

Review

Exploring the Frontier of Integrated Photonic Logic Gates: Breakthrough Designs and Promising Applications

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Abstract

The increasing demand for high-speed, energy-efficient computing has propelled the development of integrated photonic logic gates, which utilize the speed of light to surpass the limitations of traditional electronic circuits. These gates enable ultrafast, parallel data processing with minimal power consumption, making them ideal for next-generation computing, telecommunications, and quantum applications. Recent advancements in nanofabrication, nonlinear optics, and phase-change materials have facilitated the seamless integration of all-optical logic gates onto compact photonic chips, significantly enhancing performance and scalability. This paper explores the latest breakthroughs in photonic logic gate design, key material innovations, and their transformative applications. While challenges such as fabrication precision and electronic–photonic integration remain, integrated photonic logic gates hold immense promise for revolutionizing optical computing, artificial intelligence, and secure communication.



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1. Introduction

With the rapid growth of data generation, the need for faster and more energy-efficient computing technologies has become more critical than ever [1,2]. While conventional electronic logic circuits remain widely used, they are fundamentally limited by resistive losses and signal propagation delays, restricting their speed and efficiency. Integrated photonic logic gates (LGs) have emerged as a transformative solution, utilizing the speed of light to enable ultrafast, low-power computation [3,4]. This transition from traditional optical LG architectures to integrated photonic platforms has been driven by advancements in nanofabrication, nonlinear optics, and electro-optic (EO) materials, allowing for the development of high-speed, miniaturized, and scalable photonic circuits [5,6].

Over the last few decades, all-optical LGs have undergone significant evolution. Early designs relied on bulky optical components, limiting their practical applications. However, breakthroughs in silicon (Si) photonics and novel phase-change materials (PCMs) have facilitated the integration of photonic logic elements onto a single chip, vastly improving their efficiency and scalability [7,8]. Key materials such as Ge₂Sb₂Te₅ (GST) [9] and lithium niobate (LiNbO₃) [10] have enabled reconfigurable, high-contrast optical switching, further

enhancing the performance and flexibility of photonic logic operations [11,12]. Integrated photonic LGs hold tremendous potential across various domains, including high-speed data processing [13], artificial intelligence (AI) acceleration [14], secure communication [15], and quantum computing [16,17]. By leveraging nonlinear optical effects, waveguide (WG) engineering, and nanophotonic resonators, these devices offer the possibility of massively parallel and ultrafast computations [18,19]. Despite these advantages, challenges such as material limitations, integration complexities, and fabrication precision must still be addressed. Continued research and technological innovations will be essential to unlocking the full potential of photonic computing.

All-optical LGs offer a promising solution to surpass the speed constraints imposed by traditional electronic logic circuits [5]. These gates can perform essential logical functions such as AND, OR, XOR, NAND, NOR, and XNOR using only light signals. Serving as the core building blocks, they play a crucial role in developing future ultrafast optical computing systems and advanced, high-capacity optical communication networks. Their ability to process data at the speed of light positions them at the forefront of next-generation information technologies. While early implementations of all-optical LGs often relied on bulky setups with discrete optical components, advances in nanofabrication and photonics have led to a more compact and scalable solution—integrated photonic LGs [6]. These integrated devices bring the functionality of all-optical logic onto a single photonic chip, using WGs, micro-resonators, and interferometers to manipulate light in confined structures [20]. By harnessing nonlinear effects within these miniaturized platforms, integrated photonic LGs enable ultrafast, energy-efficient, and highly parallel operations, paving the way for next-generation optical computing, high-speed data processing, and quantum information technologies [7,8].

Their ability to leverage parallelism allows for highly efficient computation, while the potential for nonvolatile operation could transform memory and storage systems. However, these benefits come with challenges. The fabrication of photonic circuits is complex and costly, requiring precise manufacturing and specialized materials. Additionally, integrating photonic components with existing electronic systems remains a significant hurdle, as the two operate on different principles [12]. Photonic components, though compact, still occupy considerable space in integrated circuits, and current materials face limitations in terms of efficiency, especially for nonlinear optical operations. Furthermore, designing and optimizing photonic circuits requires specialized knowledge of both optics and electronics, making the process more intricate than traditional electronic circuit design [21]. Despite these drawbacks, integrated photonic LGs represent a promising future for high-performance, energy-efficient computing. The pros and cons of integrated photonic LGs are summarized in Figure 1.

Recent advances in unconventional computing have drawn inspiration from nanoscale systems such as molecular LGs and probabilistic bits (p-bits), which offer alternative approaches to information processing beyond deterministic digital logic [22,23]. Molecular logic gates operate through chemical or optical inputs at the molecular level, enabling compact, parallelizable logic functions [24]. Similarly, p-bits introduce stochastic behavior into computation, fluctuating between binary states with tunable probabilities, and have shown promise for optimization, neuromorphic, and quantum-inspired architectures [25,26]. These paradigms provide conceptual frameworks for developing integrated photonic logic systems that leverage nonlinear optical effects, noise, and dynamic material responses to achieve compact, energy-efficient, and potentially adaptive computing architectures.

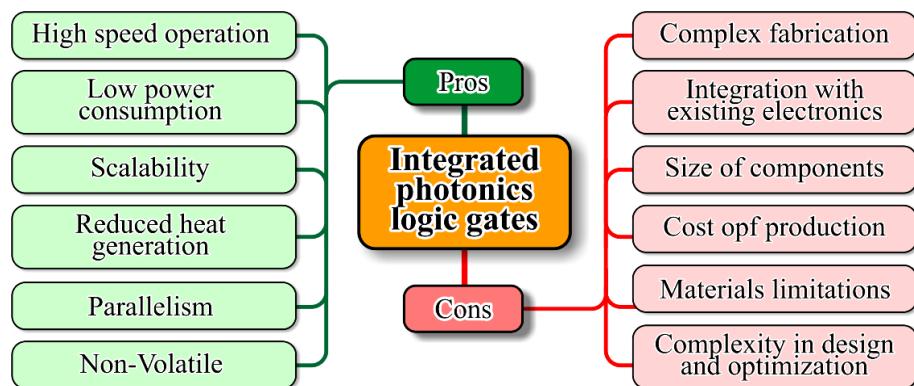


Figure 1. Pros and cons of integrated photonic LGs.

Photonic crystals (PhCs), discovered and demonstrated as a promising platform, offer a path to achieving full optical information processing and computing [18,19,27]. PhCs are particularly valued for their ability to manipulate electromagnetic waves, their compact design, low power consumption, and superior light confinement, which have enabled diverse applications in areas such as telecommunications, signal processing, biophotonics, and computing [28–33]. Beyond PhCs, several other photonic structures play a crucial role in the design and implementation of photonic LGs. Si photonic WGs are widely used due to their compatibility with CMOS fabrication, enabling the integration of high-speed, low-loss optical circuits on Si chips [34]. Microring resonators (MRRs) are another key structure, leveraging resonance effects to perform logic operations through nonlinear interactions and EO tuning [35–37]. Plasmonic WGs, which exploit surface plasmon polaritons (SPPs) at metal–dielectric interfaces, offer extreme miniaturization and ultrafast switching, making them promising for nanoscale photonic logic [38–40]. Additionally, Mach–Zehnder interferometers (MZIs) are extensively employed in photonic LGs, where phase modulation and constructive or destructive interference enable logic operations such as XOR and AND [41–43]. These diverse photonic architectures, each with unique advantages, contribute to developing ultrafast, energy-efficient optical computing systems beyond conventional electronic LGs.

This review uniquely contributes to the current body of literature by providing a comprehensive, up-to-date synthesis of recent advances in integrated photonic LG technologies. Unlike prior reviews that often focused on individual materials or specific architectures, this work systematically examines and compares nonlinear, electro-optic, and phase-change materials, detailing their suitability for photonic LGs. Furthermore, it highlights novel device designs, inverse-design methodologies, and reconfigurable platforms that enable high-speed, energy-efficient logic operations. By mapping these innovations to cutting-edge applications such as quantum computing, AI hardware acceleration, and secure communication, this review bridges the gap between foundational photonic logic principles and real-world deployment strategies, offering a forward-looking perspective that is currently lacking in existing publications.

2. Types and Characteristics of LGs

LGs are the essential building blocks of digital electronic systems, performing fundamental logical operations on one or more binary inputs to generate a single binary output [44]. These gates form the core of digital computation, with seven primary types, each playing a crucial role in different circuits [25]. The AND gate delivers a high output (1) only when all inputs are high, making it indispensable in applications where multiple conditions must be simultaneously satisfied [45]. The OR gate, on the other hand, produces a high output if at least one input is high, functioning as the digital equivalent of addition.

The NOT gate, also known as an inverter, takes a single input and outputs its opposite logic state, switching 1 to 0 or 0 to 1 [46]. In addition to these basic gates, more complex gates arise from their combinations. The NAND gate, an inverted version of the AND gate, outputs low (0) only when all inputs are high and is widely used in memory storage and processor design [47]. The NOR gate, the complement of the OR gate, outputs high only when all inputs are low, making it valuable in control logic. The XOR (exclusive OR) gate produces a high output when the number of high inputs is odd, proving essential for arithmetic operations, digital adders, and error detection systems. Finally, the XNOR (exclusive NOR) gate, the inverted form of XOR, outputs high when the number of high inputs is even, making it ideal for parity checks and digital comparisons [48]. Together, these gates form the backbone of digital logic, enabling the complex decision-making, control, and computational functions found in modern computers, mobile devices, and countless other electronic systems [49] (Table 1).

Table 1. LGs: Functions, characteristics, and applications.

| LG | Logic Function | Key Characteristics | Applications |
|------|---|---|---|
| AND | Outputs high (1) only when all inputs are high (1) | Conditional logic, reliability, simple binary multiplication | Used in decision-making circuits, digital security systems, and arithmetic units |
| OR | Outputs high (1) if at least one input is high (1) | Logical addition, inclusive operation, easy to implement | Used in alarm systems, enabling conditions, and simple control logic |
| NOT | Inverts input signal (0 to 1 or 1 to 0) | Single input, inversion property, essential in combinational circuits | Used in digital signal processing, toggling outputs, and creating control signals |
| NAND | Outputs low (0) only when all inputs are high (1) | Universal gate, can form any logic function, efficient for large circuits | Used in memory storage (flash, RAM), microprocessors, and control logic |
| NOR | Outputs high (1) only when all inputs are low (0) | Another universal gate, reliable for minimal logic designs | Used in latch circuits, digital timers, and control systems |
| XOR | Outputs high (1) when an odd number of inputs are high | Parity-based function, selective switching, is essential in arithmetic | Used in arithmetic circuits, binary adders, parity checkers, and encryption |
| XNOR | Outputs high (1) when an even number of inputs are high | Equality detection, complementary to XOR, checks signal match | Used in parity generators, digital comparators, and data verification systems |

3. Materials for Photonic LGs

The performance and functionality of integrated photonic LGs are significantly influenced by the choice of material used for their construction. Different materials offer unique characteristics that cater to specific requirements, such as speed, energy efficiency, and scalability. In the following sections, we explore three key types of materials commonly used in the design of photonic LGs: nonlinear materials, EO materials, and optical phase-change materials (O-PCMs). Each of these materials brings distinct advantages and challenges, which are crucial in determining their suitability for various all-optical logic operations. Table 2 presents a comprehensive overview of various nonlinear, EO, and phase-change materials that are commonly employed in integrated photonics for implementing LGs. These materials are selected based on their unique optical properties, such as nonlinear refractive index, EO coefficients, and phase-change characteristics. The table highlights their transparency ranges, key properties, and notable characteristics, providing insight into their suitability for all-optical logic operations, reconfigurable photonic devices, and efficient signal processing.

Moreover, noble metal nanostructures (e.g., Au, Ag) and carbon-based materials (e.g., graphene, CNTs) play a significant role in integrated photonic LGs due to their strong nonlinear optical responses and ultrafast dynamics [13,38,50]. Noble metals offer plasmonic enhancement, enabling low-threshold switching, while graphene and carbon nanotubes provide broadband absorption and fast carrier recovery, essential for high-speed logic operations [51]. Their compatibility with existing photonic platforms supports compact and efficient device integration.

Table 2. Nonlinear, EO, and phase-change materials for integrated photonic LGs: properties and characteristics.

| Material | Type | Key Properties and Characteristics | Response Time | χ^2 (pm/V) | χ^3 (esu) |
|---|-----------|--|---------------|-------------------|-------------------------------|
| Silicon Nitride (Si_3N_4) [52,53] | Nonlinear | $n_2: \sim 10^{-16} \text{ cm}^2/\text{W}$; Visible to MIR; Negligible two-photon absorption in telecom bands | ~ps | (centrosymmetric) | $\sim 1 \times 10^{-14}$ |
| Liquid Crystals [54,55] | Nonlinear | $n_2: \text{up to } 10^{-4} \text{ cm}^2/\text{W}$; Visible to NIR; Exceptionally large optical nonlinearity | ms–μs | (centrosymmetric) | $\sim 10^{-7}$ to 10^{-6} |
| Phthalocyanines (e.g., CuPc) [56,57] | Nonlinear | $n_2: \sim 10^{-5} \text{ cm}^2/\text{W}$; Visible; High third-order nonlinearity for optical switching | ns–ps | (centrosymmetric) | $\sim 10^{-8}$ to 10^{-7} |
| Lithium Niobate (LiNbO_3) [58] | EOs | $r_{33}: \sim 30 \text{ pm/V}$; $0.4\text{--}5 \mu\text{m}$; Strong Pockels effect | ~ps | ~30 | $\sim 10^{-14}$ to 10^{-13} |
| Barium Titanate (BaTiO_3) [59] | EOs | $r_{33}: \sim 100 \text{ pm/V}$; $0.4\text{--}5 \mu\text{m}$; Very high EO coefficient | ~ps | ~100–160 | $\sim 10^{-12}$ |
| $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) [60,61] | O-PCM | Large Δn ; $1\text{--}18.5 \mu\text{m}$; Fast phase change for nonvolatile switching | ~ns | (centrosymmetric) | $\sim 10^{-11}$ to 10^{-10} |
| $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ (GSST) [62,63] | O-PCM | $\Delta n \sim 2.0$; $1\text{--}18.5 \mu\text{m}$; Better transparency and loss profile | ~ns | (centrosymmetric) | $\sim 10^{-11}$ to 10^{-10} |
| Vanadium Dioxide (VO_2) [64] | O-PCM | Transition at $\sim 68^\circ\text{C}$; Visible to MIR; Ultrafast switching via insulator–metal transition | ~fs–ps | (centrosymmetric) | $\sim 10^{-11}$ |

3.1. Nonlinear Materials

Nonlinear materials are essential in integrated photonic LGs because they enable the manipulation of light in ways that linear materials cannot [65,66]. These materials respond to optical signals in a nonlinear fashion, meaning their properties change depending on the intensity of the light passing through them. This nonlinearity allows for key optical operations, such as AND, OR, and XOR, which are critical for LGs [67]. Effects like second-harmonic generation, self-phase modulation, and four-wave mixing are utilized to perform these operations within photonic circuits. Materials commonly used in integrated photonics include Si [68], silicon nitride [52], lithium niobate [69], and indium phosphide [70], which exhibit strong nonlinear properties. By using these nonlinear materials, photonic LGs can operate at the speed of light, offering significant advantages over traditional electronic LGs in terms of speed, integration density, and energy efficiency, paving the way for faster and more powerful optical computing systems.

Recently, a novel flip-flop concept governed by the nonlinear optical behavior of dynamically distributed nanostructures within a liquid medium was proposed [71]. The active component, silver-decorated carbon nanotubes were dispersed in ethanol to form a responsive nanofluid. Functionally, the system operates as a probabilistic NAND latch. Its optical properties were investigated through two-wave mixing experiments using nanosec-

ond laser pulses at a 532 nm wavelength. The underlying mechanism relies on Brownian motion, which modulates the nonlinear transmittance of the dispersed nanostructures and enables probabilistic bit behavior. The system's output states were influenced by irradiance-dependent nonlinear absorption and further shaped by the interplay between current optical inputs and previous output states through feedback mechanisms. The observed optical response emerged from a probabilistic process, driven by spatial variations in nanoparticle concentration. Key system parameters were identified through a stability assessment of the nanofluid. Overall, the findings underscore the potential of nanohybrid fluids in implementing probabilistic logic, supporting quantum-level switching, and enabling next-generation optical sensing platforms [71].

Ghadi et al. introduced the design and simulation of all-optical LGs using Kerr nonlinear circular resonators to improve the performance of optical CPUs [72]. Their simulations, conducted with the two-dimensional finite-difference time-domain (FDTD) technique, featured simple plasmonic structures where switching states depended on the intensity and positioning of pump, signal, and monitor beams. Additionally, they accounted for manufacturing tolerances by simulating fabrication errors for each gate type. The reported transmission rate variations for AND, NOR, OR, and NOT gates were 42%, 95%, 55%, and 92%, respectively, with an extremely fast response time of around 50 femtoseconds. Key advantages of their design included support for multiple logic functions, high transmission performance, resilience to production variations, and compact size, making them a promising solution for future photonic computing systems [72].

In another study, Sharifi et al. proposed a new nonlinear photonic crystal (PhC) structure to implement all-optical LGs [73]. Their design featured a nonlinear directional coupler with integrated junctions. The base configuration enabled XOR and OR operations, and further structural adjustments allowed for additional gates like XNOR, NOR, and AND. Si nanocrystals formed the nonlinear rods, providing the necessary phase modulation for switching. Performance assessment was conducted through FDTD and plane-wave expansion (PWE) simulations, demonstrating operational speeds beyond 1 Tbit/s with uniform input–output signals and switching power needs of around 3W [73]. Furthermore, two-dimensional lithium niobate PhC circuits incorporating microcavities enabled the realization of all-optical AND, XOR, and NOT gates, along with a half-adder circuit [74]. These devices exhibited an extinction ratio of up to 23 dB, thanks to the efficient switching characteristics of two-missing-hole microcavities. Such devices highlight the potential for sophisticated optical computing components within lithium niobate-based photonic platforms [74].

Jandieri et al. introduced an innovative approach for constructing scalable all-optical LGs focusing on NOT, AND, and NAND gates by utilizing bandgap solitons within coupled photonic crystal WGs [8]. The design was based on a planar photonic crystal (PhC) structure composed of a hexagonal array of air holes in crystalline silicon (c-Si), serving as the nonlinear medium (Figure 2a). The gates operated fully in the time domain, allowing temporal solitons to maintain their pulse shapes throughout each logic process. This inherent stability made it possible to cascade multiple gates seamlessly, eliminating the need for intermediate signal amplification. Consequently, the output from one LG could be fed directly into the next, enabling the development of advanced multi-input all-optical logic circuits. Since NOT, AND, and NAND gates are the fundamental elements for constructing all other logic functions, this method provides a flexible and efficient route toward high-speed all-optical digital processing systems [8].

The realization of a NAND gate was accomplished by combining an AND gate and a NOT gate in a series configuration. Figure 2b–e illustrate the structure and operation of the proposed all-optical NAND LG on a single enlarged photonic crystal (PhC) chip. The

output signals retrieved through comprehensive computational electromagnetic analysis, depicted in Figure 2e, confirm the successful functionality of the proposed NAND gate design. A critical aspect of this design is the “bridge” section, which ensured seamless transfer of the temporal soliton pulse from the AND gate to the NOT gate. To minimize power loss at port 1 and port 3, specific air holes were removed in the bridge area to enable smooth pulse propagation. The optimal length of this bridge section has been determined to be approximately six times the lattice period of the PhC [8].

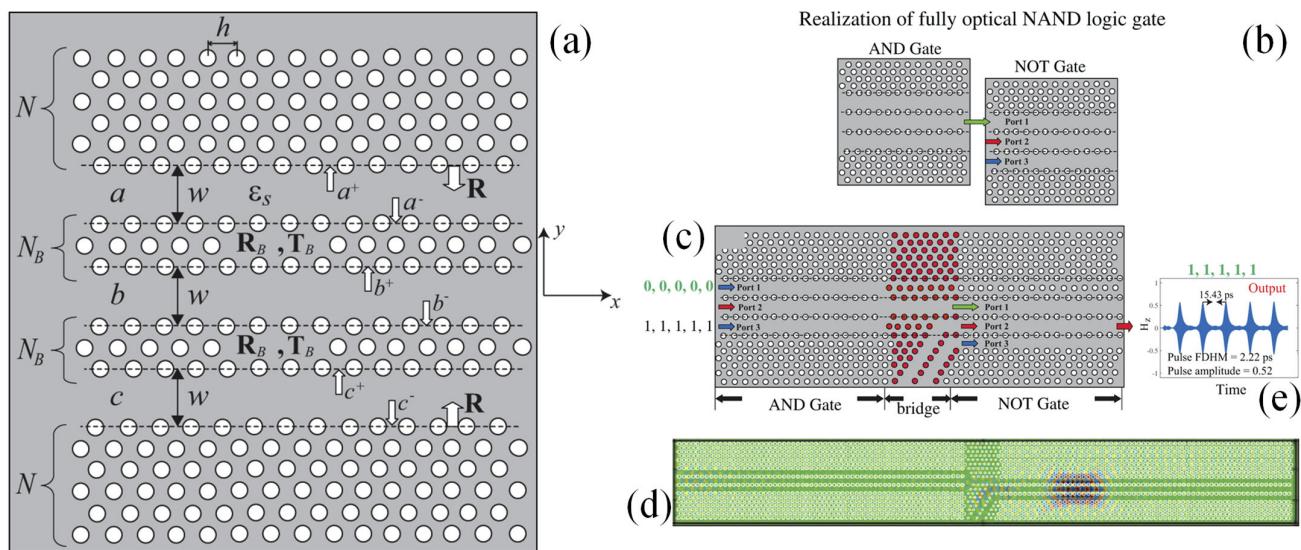


Figure 2. (a) A schematic representation showing three identical symmetric coupled photonic crystal waveguides (C-PhCWs) with guiding channels of equal width, separated by barrier layers consisting of two photonic crystals, each with a specific number of layers. These PhCs feature a hexagonal lattice of circular air holes arranged periodically along the axis with a defined period. (b) Conceptual design of an all-optical NAND gate formed by connecting an AND gate in series with a NOT gate. (c) Integration of the NAND gate layout onto a single expanded PhC chip. (d) simulated magnetic field patterns illustrating signal pulse propagation within the NAND gate. (e) magnetic field distribution corresponding to the output signal detected at port 2 [8].

Additionally, to avoid significant attenuation of the output signal from port 2 of the AND gate while passing through the bridge, further geometric adjustments are necessary. FDTD simulations showed that decreasing the radii of the air holes in the bridge region to 0.18 effectively supports stable soliton propagation. This adjustment allowed the output pulse to traverse the bridge without substantial distortion, even after experiencing some power loss from back-reflections. Nevertheless, despite these modifications, some reduction in signal amplitude at port 2 remained due to residual reflections, which are accounted for in the FDTD simulation of the entire NAND gate system. However, thanks to the inherent digitalization feature of the device, it was possible to fine-tune the input conditions of the NOT gate to ensure proper NAND gate functionality. Further optimization of the bridge region, such as careful adjustments of air-hole radii and positions, reduced back-reflections even more. Another promising approach was the integration of a tilted PhC WG section serving as a “wave dump,” which would direct reflected pulses from the NOT gate out into free space. This strategy helped protect the nonlinear operation of the AND gate by preventing back-reflected signals from triggering unintended soliton formation. Continued refinement of WG bends and coupling into free space remains essential for achieving stable, high-performance all-optical logic operations [8].

Recently, nanoscale all-optical LG devices have attracted considerable interest due to their promising use in optical computing and interconnection systems. Yang et al. reported the development of integrated nanoscale all-optical XNOR, XOR, and NAND gates by leveraging plasmon-induced transparency in plasmonic circuits with on-chip tunability [75]. By adding an organic composite layer, they significantly boosted the system's nonlinearity, taking advantage of resonant excitation, slow-light effects, and strong field confinement within the plasmonic nanocavity. This innovation reduced the required excitation power to just 200 μ W, about a thousand times lower than previous designs. Additionally, the device size was compressed to under 600 nm, improving prior benchmarks by an order of magnitude. The contrast ratio (CR) between logic states "1" and "0" reached an impressive 29 dB, among the highest ever documented. These achievements pave the way for integrated platforms in nonlinear and quantum optics and open new possibilities for nanophotonic chip development based on nonlinear plasmonics [75].

To demonstrate the logic function "0 XNOR 0 = 1," the input grating was patterned only onto reference WG C, as depicted in Figure 3a. The CCD image captured under 200 μ W excitation from a 120 fs, 830 nm laser source (Figure 3b) displayed a strong scattered signal of 90 arbitrary units (au), indicating a logic "1" output, with finite element method (FEM) simulations supporting these observations in Figure 3c. For "1 XNOR 0 = 0," the input grating was placed on both reference WG C and WG A (Figure 3d). The corresponding CCD image (Figure 3e) revealed minimal scattering (0.12 au), representing a logic "0" output, confirmed by FEM results in Figure 3f [75]. Similarly, the logic operation "0 XNOR 1 = 0" was tested by etching the input grating onto WGs C and B (Figure 3g). The measured CCD image (Figure 3h) showed weak scattering, again at 0.12 au, aligning with FEM results in Figure 3i. For the case "1 XNOR 1 = 1," gratings were added to WG C and both input WGs A and B (Figure 3j). The resulting CCD image (Figure 3k) indicated a strong output signal of 113 au, with FEM simulations confirming this behavior in Figure 3l [75].

To understand the physical principles behind these operations, the researchers calculated the linear transmission spectra of a plasmonic WG side-coupled to nanocavity C1 covered with MEH-PPV:IR140. The results (Figure 3m–p) demonstrated that when light propagated only through reference WG C, the spectrum shifted to 830 nm, resulting in high transmission. However, when the signal passed through WG C and either WG A or B, the transmission minimum also moved to 830 nm, causing reduced transmission (Figure 3q). In contrast, when passing through WG C and both A and B, the spectrum again aligned with 830 nm, restoring high transmission levels [75].

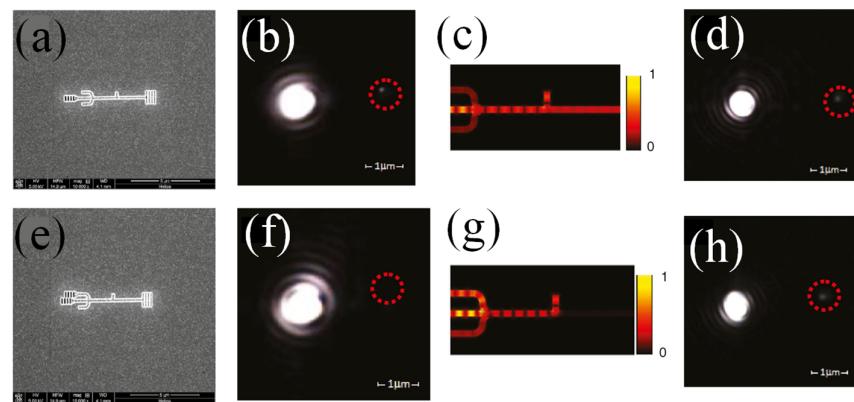


Figure 3. Cont.

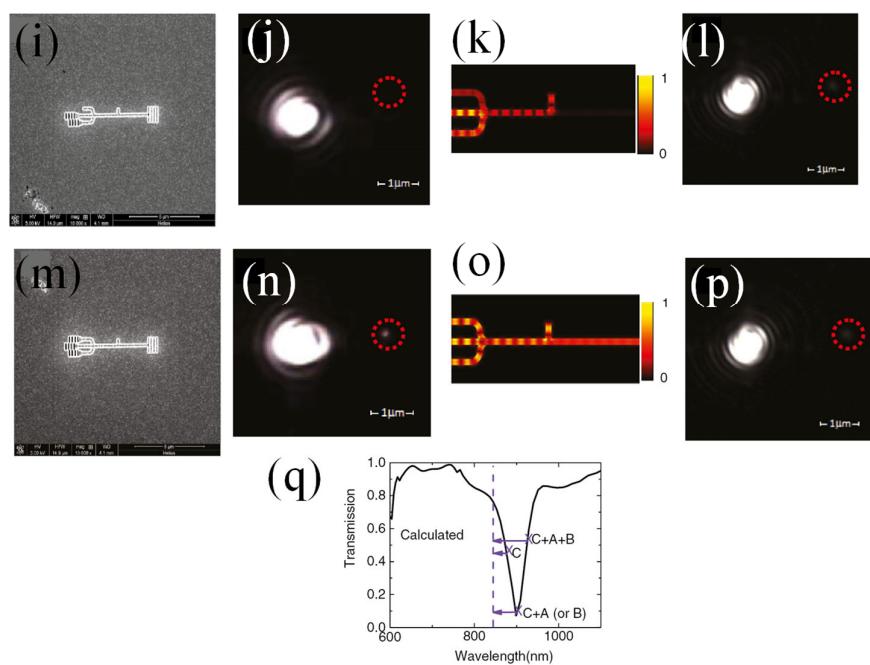


Figure 3. XNOR gate logic operation in a series of images and calculated results. For the case of “0 XNOR 0 = 1,” the SEM image of the plasmonic sample without the MEH-PPV:IR140 cover layer is shown in (a), followed by the CCD image under 830 nm, 120 fs laser excitation in (b), the calculated results in (c), and the CCD image of the control sample in (d). Similarly, for “1 XNOR 0 = 0,” the SEM image of the plasmonic sample without the MEH-PPV:IR140 cover layer is shown in (e), with the corresponding CCD image under 830 nm, 120 fs laser excitation in (f), the calculated results in (g), and the CCD image of the control sample in (h). In the case of “0 XNOR 1 = 0,” the SEM image of the plasmonic sample is shown in (i), along with the CCD image under the same excitation conditions in (j), the calculated results in (k), and the CCD image of the control sample in (l). Lastly, for “1 XNOR 1 = 1,” the SEM image of the plasmonic sample is shown in (m), with the CCD image under 830 nm, 120 fs laser excitation in (n), the calculated results in (o), and the CCD image of the control sample in (p). The decoupling grating position is indicated by a red dashed circle. Additionally, the calculated linear transmission spectrum of a plasmonic WG side-coupled to plasmonic nanocavity C1, with the MEH-PPV:IR140 cover layer, is shown in (q) under various excitation conditions. The crosses mark the shift to the 830 nm position [75].

3.2. EO Materials

EO materials are key to the development of advanced LGs for optical computing [76]. These materials change their optical properties, such as refractive index, when subjected to an electric field, enabling them to modulate light in response to electrical signals [77]. This unique property makes EO materials ideal for creating high-speed, energy-efficient LGs that can outperform traditional electronic ones [78]. By using light instead of electrical currents, optical LGs can achieve faster data processing with lower power consumption, leading to more efficient computing systems. Common EO materials, like lithium niobate (LiNbO_3), indium phosphide (InP), and Si photonics, integrate well with existing semiconductor technologies while offering the benefits of optical data transmission [79].

Das et al. presented a new EO reconfigurable gate that can switch between OR and Ex-OR operations [80]. The design incorporated two MRRs positioned in parallel in the upper and lower arms of an MZI structure, with a tunable phase shifter placed in the lower arm that can be controlled externally. When the phase of the tunable phase shifter was set to 0, the gate operated as an OR gate, and when the phase was adjusted to a specific value, it switched to an Ex-OR gate. The MRRs used EO modulation through carrier injection, with voltages of 2 V and -1.85 V representing logic 1 and logic 0, respectively. The performance of the Ex-OR gate was also analyzed for deviations in the phase shift from

the ideal value. The extinction ratio achieved was 17 dB for Ex-OR operation and 7.58 dB for OR operation. To validate the circuit's functionality, time-domain simulations at a data rate of 10 Gbps and a wavelength of 1550 nm were performed, using two electrical bit streams as inputs [80]. Furthermore, Das et al. presented a design of NOT, OR, and AND LGs using a 2:1 Multiplexer (MUX) based on a titanium-diffused lithium niobate EO Mach–Zehnder interferometer (MZI) [81]. The rising demand for terahertz-speed computation and efficient interconnects drives the shift toward optical integrated circuits over CMOS technology. Shannon decomposition and reduced binary decision diagram (RBDD) mapping were applied to optimize MUX-based logic circuits. The designs were simulated using the beam propagation method (BPM) via OPTIBPM. Fabricated on 33 mm × 100 μm wafers, the proposed circuits offer high-speed response suitable for communication systems and industrial applications. Key parameters—0.0012 dB insertion loss, 28.97 dB extinction ratio, and 29.5 dB CR—met acceptable standards [81].

Yadav et al. explored optical switching within the MZI structure driven by the EO effect [82]. By exploiting this phenomenon, a phase difference was introduced between optical signals traversing the two arms of the MZI structure. Such EO-based switching mechanisms are applicable in implementing various digital logic operations. A thorough analysis of the EO effect was presented, including a detailed mathematical model that outlined the devices and operational parameters necessary for calculating normalized output power at the MZI structure's ports. The proposed MZI design leveraged the EO effect to create efficient optical switching and sensing systems. This approach offered significant advantages, including the ability to transmit signals over long distances with minimal power loss and immunity to electromagnetic interference. Additionally, optical WGs provided a considerably larger transmission bandwidth compared to traditional communication channels. Utilizing an infrared laser light source further enhanced the capacity for long-distance transmission [82].

Graphene's plasmonic modes can be effectively controlled via an external gate voltage, making it an ideal material for designing EO graphene plasmonic LGs at mid-infrared wavelengths. Ooi et al. showed that these devices surpass traditional optical LGs by exhibiting cut-off states and interferometric effects [83]. Furthermore, six fundamental LGs (NOR, AND, NAND, OR, XNOR, XOR) were demonstrated to not only achieve an ultracompact size, smaller than the 10 μm operating wavelength, but also exhibit a high minimum extinction ratio of 15 dB. These graphene plasmonic LGs offer significant potential as building blocks for future nanoscale mid-infrared photonic integrated circuits [83].

A recent development in integrated photonic devices has introduced innovative solutions for optical computing and data storage, supporting the advancement of photonic systems beyond traditional von Neumann architectures [84]. This work presented hybrid nonvolatile EO plasmonic switches alongside novel designs for both combinational and sequential logic circuits (Figure 4a). The switches were engineered using plasmonic WGs combined with a thin PCM layer. By toggling the PCM between amorphous and crystalline phases, the optical losses in the WG were able to be effectively modulated. The electric field distributions for both material states are illustrated in Figure 4b,c. Phase transitions in the PCM were initiated through electrical threshold switching or thermal conduction, utilizing either external heaters or heat generated from the plasmonic WG metal itself. The proposed framework successfully implemented basic LGs, a half-adder, and sequential logic circuits, all using these plasmonic switches as active elements. The resulting designs exhibited compact structures, low power consumption, rapid switching speeds, and extinction ratios exceeding 20 dB, merging photonics, plasmonics, and electronics on a single platform to enable high-speed optical logic [84].

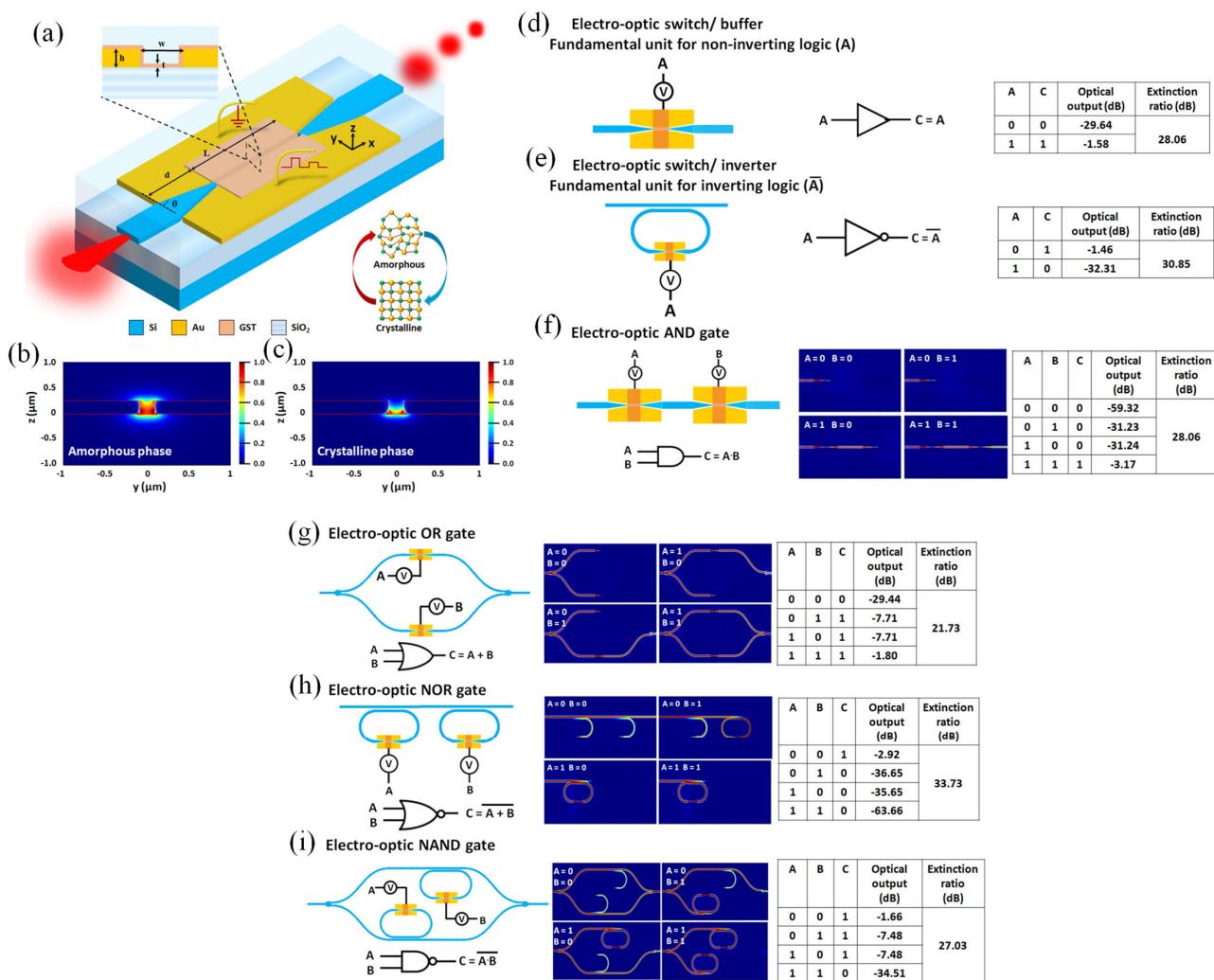


Figure 4. (a) Schematic of the proposed broadband nonvolatile hybrid EO plasmonic switch. The inset displays the cross-sectional view of the plasmonic slot WG with a thin GST layer. Mode profiles of the PCM-coated plasmonic slot WG at a telecom wavelength of 1550 nm are presented for the (b) amorphous phase and (c) crystalline phase of GST. The mode profiles were calculated for TE-polarized light. Configurations, graphical representations, and truth tables for the following EO logic units: (d) non-inverting logic unit, (e) inverting logic unit, (f) AND gate, (g) OR gate, (h) NAND gate, and (i) NOR gate [84].

Figure 4d–i depict the configurations of key non-inverting and inverting logic elements (Figure 4a,b) and six fundamental LGs—AND, OR, NAND, NOR, XOR, and XNOR—using the hybrid nonvolatile EO plasmonic switch as the main component. The EO AND gate (Figure 4f) was realized by placing two plasmonic switches in series. If either input or both are at logic “0,” the output remains low due to the crystalline state. High output transmission is achieved only when both inputs are at logic “1,” with the switches in their amorphous phase. This configuration produced an extinction ratio of 28.06 dB. The OR gate (Figure 4g) was constructed with two parallel switches, incorporating an input splitter and an output combiner. When either input is logic “1,” the output signal is strong. The extinction ratio reached 21.73 dB, although higher insertion losses were observed due to signal splitting. Finally, Figure 4h,i display the NAND and NOR gate designs, built by connecting inverting logic units in parallel and series, respectively. These designs highlighted the potential of EO plasmonic switches for creating compact, low-power, and high-performance all-optical logic systems [84].

3.3. Optical Phase-Change Materials (O-PCMs)

Optical phase-change materials (O-PCMs) are gaining attention in the development of advanced LGs due to their ability to undergo reversible transitions between different phases, which alter their optical properties [63,85,86]. These materials can switch between amorphous and crystalline states in response to external stimuli, such as heat or light. When used in LGs, O-PCMs exploit these phase transitions to control light transmission, reflection, or absorption, enabling the material to perform binary operations. In their amorphous state, O-PCMs typically have high optical absorption and low transparency, while in their crystalline state, they exhibit high transparency and low absorption [87]. This change in optical characteristics can be used to represent binary states, such as "0" and "1," in a similar way to how traditional LGs operate with electrical signals. The phase change is initiated by applying a pulse of light or heat, which makes the material transition between states, allowing for ultrafast switching speeds [63].

The main advantage of O-PCM-based LGs is their potential for high-speed operation with low power consumption, as they rely on light rather than electrical signals [88]. Additionally, O-PCMs can be integrated with photonic circuits, enabling faster data processing and more efficient communication compared to traditional electronic LGs [89]. As research into O-PCMs progresses, these materials hold promise for revolutionizing LG technology, especially in areas requiring high-speed data processing and low-energy consumption, such as optical computing and photonic integrated circuits [84].

Zhang et al. presented a design of highly compact, reconfigurable, and nonvolatile photonic LGs, each measuring just $2.4\text{ }\mu\text{m} \times 2.4\text{ }\mu\text{m}$, achieved through an inverse-design strategy that incorporated two states of PCMs [7]. The gate architecture consisted of four ports: two for input, one for output, and one for control. This design facilitated the implementation of four logic operations—OR, NOT, AND, and XOR—within a single device. Simulations using 3D-FDTD methods showed that these gates function effectively across a 35 nm wavelength range around 1550 nm, with CR of 7.64 dB for OR, 6.1 dB for NOT, 3.3 dB for AND, and 18.92 dB for XOR. The compact nature of the devices resulted in a transmission propagation delay (TPD) of less than 1 ps, making them suitable for high-speed data processing. Additionally, the analysis of manufacturing tolerances revealed that these structures maintained excellent performance despite fabrication deviations [7]. Figure 5a presents a schematic representation of the LG.

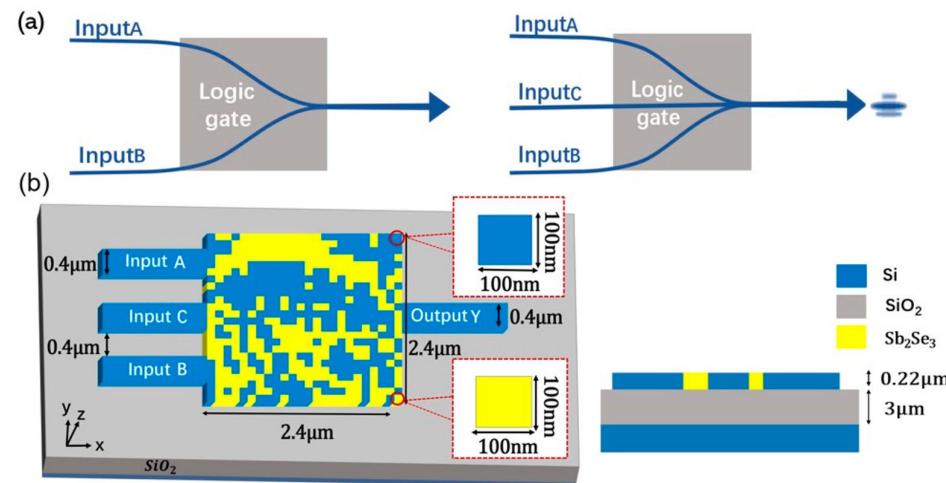


Figure 5. Cont.

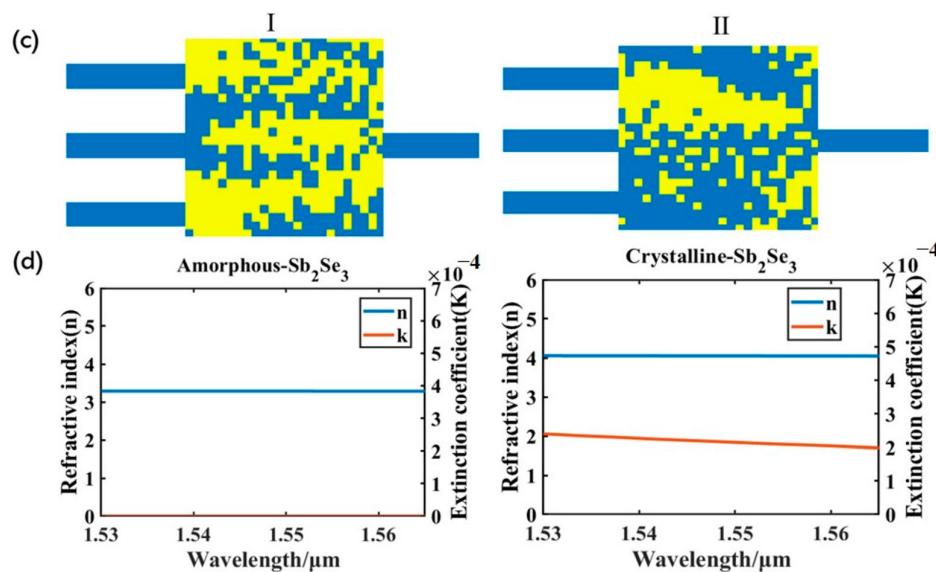


Figure 5. Design of photonic LGs. (a) Visual representation of the photonic LG. (b) Diagram illustrating the structural parameters, where a TE mode wave in the C-band is transmitted from the left input WGs to the right output WG through an optimized region. (c) Schematic depiction of structures I and II. (d) Refractive index and extinction coefficient curves of Sb₂Se₃ for wavelengths ranging from 1530 nm to 1565 nm, highlighting differences between the crystalline and amorphous states [7].

To establish a condition where WGs A and B receive no light input while the output WG produces light, a control WG C with a continuous light source input was incorporated during the design process. The structural configuration of the LG is depicted in Figure 5b. Figure 5c illustrates two distinct structures, labeled I and II, both designed using the DBS method and following the design framework outlined in Figure 5b [7]. The device employed a standard silicon-on-insulator (SOI) platform, consisting of a 220 nm-thick Si layer over a 3 μm-thick SiO₂ layer. The layout included three input WGs and one output WG, all with a width of 400 nm and separated by a 400 nm gap. The central design area measured 2.4 μm × 2.4 μm and was divided into a 24 × 24-pixel grid, where each pixel was sized at 100 nm × 100 nm. The pixel states were defined by either Si or antimony selenide (Sb₂Se₃), with blue cells representing Si and yellow cells indicating Sb₂Se₃. Switching between the crystalline and amorphous phases of Sb₂Se₃ enabled the realization of different LG functionalities. In structure I, the device operated as a NOT gate when Sb₂Se₃ was crystalline and as an OR gate when Sb₂Se₃ was amorphous. In structure II, it functioned as an XOR gate with crystalline Sb₂Se₃ and as an AND gate with amorphous Sb₂Se₃. Figure 5d presents the extinction coefficient and refractive index curves of Sb₂Se₃ within the C-band, demonstrating its remarkably low loss at a wavelength of 1550 nm in both phases, along with a pronounced contrast between the refractive indices of the two states [7].

To better understand the performance and suitability of various photonic LGs, it is important to consider the materials used to construct them. Nonlinear materials, EO materials, and O-PCMs each offer unique advantages and challenges that influence the design and operation of these gates. Table 3 summarizes the key characteristics, best-suited LGs, advantages, and challenges associated with each material type, providing a clear comparison to guide the selection of materials for different photonic logic applications.

Table 3. Comparison of photonic LG suitability based on nonlinear materials, EO materials, and O-PCMs with respect to their key characteristics.

| Material Type | Key Characteristics | Best-Suited Photonic LGs | Advantages | Challenges | Logic Fingerprint |
|-----------------------------------|--|--|---|--|---|
| Nonlinear Materials [19,75,90,91] | High third-order nonlinearity, ultrafast response, supports soliton propagation, intensity-dependent refractive index change | AND, OR, NAND, NOR, XOR, NOT (especially soliton-based and threshold-driven) | All-optical ultrafast operation; time-domain stability | High power consumption; optical losses; fabrication precision | Threshold output based on intensity; logic encoded in soliton formation (e.g., output “1” only above intensity threshold) |
| EO Materials [5,92] | Pockels effect: refractive index changes under applied voltage; fast and tunable response | Reconfigurable AND, OR, XOR, NOT (electrically controlled) | Fast switching; low losses; reconfigurable | Needs electrical input; integration complexity; not purely optical | Externally tunable transmission/reflection states mapped to logic (e.g., applied voltage sets logic “1” or “0”) |
| PCMs [93–95] | Reversible switching between amorphous and crystalline states with high optical contrast | Memory-assisted AND, OR, NOT (nonvolatile gates) | Nonvolatile optical logic; memory functionality; low static power | Slower speed; endurance limits; thermal issues | State-dependent output (e.g., “1” = crystalline, “0” = amorphous); persistent logic state without input |

Having explored the diverse materials and architectures that underpin integrated photonic LGs, it becomes clear that material choice and design intricacies are key enablers of device performance. However, the ultimate measure of these innovations lies in their real-world impact. The following sections examine how integrated photonic LGs are being applied across transformative fields from optical computing and high-speed data processing to quantum communication and AI hardware acceleration. These applications not only highlight the technological potential of photonic LGs but also underscore the growing demand for faster, more secure, and more energy-efficient information processing systems.

4. Challenges in System Architecture, Programming, and Performance Metrics

While integrated photonic LGs demonstrate remarkable speed and energy efficiency, their adoption into large-scale computing platforms requires addressing key architectural and performance considerations [96–98]. One of the foremost challenges is programmability [99]. Unlike conventional electronic logic gates, which can be dynamically reprogrammed via software or electronic control signals, photonic LGs are inherently passive and require material-level or structural adaptations to alter their behavior [100,101]. Nonetheless, significant progress has been made through the use of EO materials, which allow for real-time modulation of optical signals using external voltages [102]. Structures such as tunable MZIs and MRRs have been used to implement reconfigurable gates [37,79,103]. Additionally, PCMs like GST and GSST have enabled nonvolatile optical switching, allowing a single device to be reconfigured between logic states (e.g., OR to XOR) by thermally or optically induced phase transitions [7]. These mechanisms offer pathways toward programmable optical processors with minimal energy requirements.

At the system architecture level, integrating photonic LGs into functional computing platforms introduces several engineering hurdles. One major issue is interfacing with electronic systems, as photonic and electronic domains operate under different signal protocols and timescales. Ensuring efficient optical-to-electronic (and vice versa) conversion without introducing significant latency remains a persistent challenge [104]. Another concern is ther-

mal management, especially for dense photonic circuits where localized heating from active switching elements (e.g., PCMs or plasmonic hotspots) can lead to cross talk or degradation of performance [105,106]. Furthermore, cascability and synchronization are critical for implementing multi-stage logic circuits that are not trivial in photonic systems operating at femtosecond or picosecond speeds [107,108]. Accurate timing control and phase coherence must be maintained, which requires advanced design strategies. Finally, fabrication precision is crucial, particularly for photonic crystal or plasmonic structures, where deviations in the order of tens of nanometers can dramatically affect optical resonance and switching behavior [109].

To facilitate a more systematic comparison between integrated photonic LGs and traditional CMOS-based systems, key quantitative performance metrics are outlined in Table 4. These include gate density, energy consumption per bit, switching speed, bandwidth, and extinction ratios. Photonic LGs, particularly those utilizing plasmonic and photonic crystal structures, have achieved densities in the range of $\sim 10^4\text{--}10^5$ gates per mm^2 and exhibit switching times as low as 50 femtoseconds [110,111]. Power consumption varies by architecture and material, with some plasmonic implementations requiring as little as 200 μW per gate and certain PCM-based systems operating at sub-nanowatt levels in static states [112,113]. The bandwidth advantage of photonic systems is also notable, with some designs achieving data rates exceeding 1 terabit per second. Although CMOS logic maintains superior integration density and manufacturing maturity, photonic LGs offer compelling trade-offs in speed, energy-delay product, and potential for massively parallel computation.

Table 4. Comparative performance metrics of integrated photonic LGs vs. CMOS logic.

| Parameter | Photonic LGs (Typical) | CMOS Logic (Typical) |
|---------------------------|--|---|
| Gate Density | $\sim 10^4\text{--}10^5$ gates/ mm^2 (plasmonic, PhC) [7] | $\sim 10^7\text{--}10^8$ gates/ mm^2 |
| Power per Bit | $\sim 200 \mu\text{W}/\text{gate}$ (plasmonic), sub-nW (PCM) [75] | 10–100 pJ/bit |
| Speed/Switching Time | 50 fs–10 ps [114,115] | $\sim 10\text{--}100$ ps |
| Bandwidth | >1 Tbps [73] | $\sim 10\text{--}100$ Gbps |
| Footprint per Gate | 0.5–2.4 μm^2 (with optimized layouts) [7] | $<1 \mu\text{m}^2$ |
| Insertion Loss/Extinction | Up to 28 dB CR (e.g., EO and PCM gates) [84] | N/A (not optical) |

5. Applications of Integrated Photonic LGs

Recent advancements in integrated photonic LG designs and material innovations have opened the door to a variety of impactful applications. These devices are no longer confined to theoretical models or experimental setups: instead, they are driving innovation across fields such as high-speed data processing, data center optimization, quantum communication, and AI hardware acceleration. In the following sections, we examine how integrated photonic LGs are being applied to meet the growing demands for faster, more efficient, and more secure computing and communication systems.

5.1. Optical Phase-Change Materials (O-PCMs)

Optical computing and high-speed data processing harness the power of photons rather than electrons to achieve extraordinary processing speeds and energy efficiency [3,5,116]. By leveraging the unique properties of light, such as high bandwidth and parallelism, optical computing enables faster data transmission and processing compared to traditional electronic systems [117]. This breakthrough technology holds immense potential across various fields, including AI, big-data analytics, telecommunications, and cryptography, where real-time analysis and rapid processing are critical [118]. Additionally, its ability to reduce energy consumption and minimize heat generation makes it a more

sustainable alternative to conventional computing [34]. As data processing demands continue to escalate, optical computing could transform industries by providing faster, more efficient, and highly scalable solutions [4,13,119,120].

Shahi et al. introduced optimized all-optical NOT and XOR LGs based on interference effects in two-dimensional PhC structures [121]. Designed for next-generation photonic integrated circuits (PICs), these gates feature carefully refined output WGs to enhance performance. The proposed devices demonstrated a fast response time of 0.15 ps, a CR of 32.88 dB, and a data rate of 6.67 Tbit/s, all within a compact footprint of $83.55\text{ }\mu\text{m}^2$. To further demonstrate scalability, a 4×2 optical encoder was developed using the same design principles, achieving a 26.54 dB CR in just $133.67\text{ }\mu\text{m}^2$ of space. The photonic bandgap was determined through the plane-wave expansion method, while device performance was verified via finite-difference time-domain simulations. These results confirmed the potential of the proposed designs for compact, high-speed optical computing applications [121].

Traditional neural network computing on integrated circuits faces challenges in energy efficiency and speed. Optical interconnections, particularly using graphene, offer a promising alternative due to their compact size and strong surface plasmon confinement [122]. Zhu et al. proposed a graphene-based one-bit optical numerical comparator built on a $0.4\text{ }\mu\text{m}^2$ dielectric layer with Y-shaped graphene nanoribbons [123]. Switching was controlled by tuning graphene's chemical potential via external voltage. Finite-difference time-domain simulations at $9.55\text{ }\mu\text{m}$ TM mode showed a minimum extinction ratio of 31.12 dB and amplitude modulation of 0.77 dB. The design outperformed existing comparators in size, loss, and stability. Process variation analysis confirmed its reliability for high-speed, integrated photonic computing in neural networks [123].

An advanced design method has been employed to create ultracompact Si-based all-optical LGs (OR, XOR, NOR, AND, and NAND) with footprints as small as $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$ (Figure 6a–d) [124]. This approach integrated the method of moving asymptotes (MMA) with the finite element method (FEM) to achieve highly optimized structures. The substrate was divided into numerous small regions, with the refractive index of each region fine-tuned according to the desired performance goals. While this optimization process initially resulted in gradient-index distributions that are impractical to fabricate, a binary reconstruction technique was applied to transform these gradients into binary structures. This involved eliminating intermediate refractive index values, smoothing the structure's boundaries, and refilling the areas with Si or air, resulting in a physically realizable design. Simulations confirmed the high performance of these devices, showing strong CR for each LG: OR and XOR gates achieve between 23.50 dB and 25.50 dB, NOR gates between 6.33 dB and 7.91 dB, AND gates between 4.44 dB and 6.13 dB, and NAND gates between 8.85 dB and 10.07 dB. Additionally, these LGs demonstrated significantly broader bandwidths nearly ten times wider than traditional designs without sacrificing overall performance. The OR and XOR gates operated effectively across wavelengths from 800 nm to 1600 nm, NOR gates from 850 nm to 1350 nm, AND gates from 1000 nm to 1240 nm and 1310 nm to 1400 nm, and NAND gates from 1360 nm to 1530 nm. This design methodology not only enabled compact, high-performance photonic logic devices but also holds great promise for future applications in optical computing and signal processing [124].

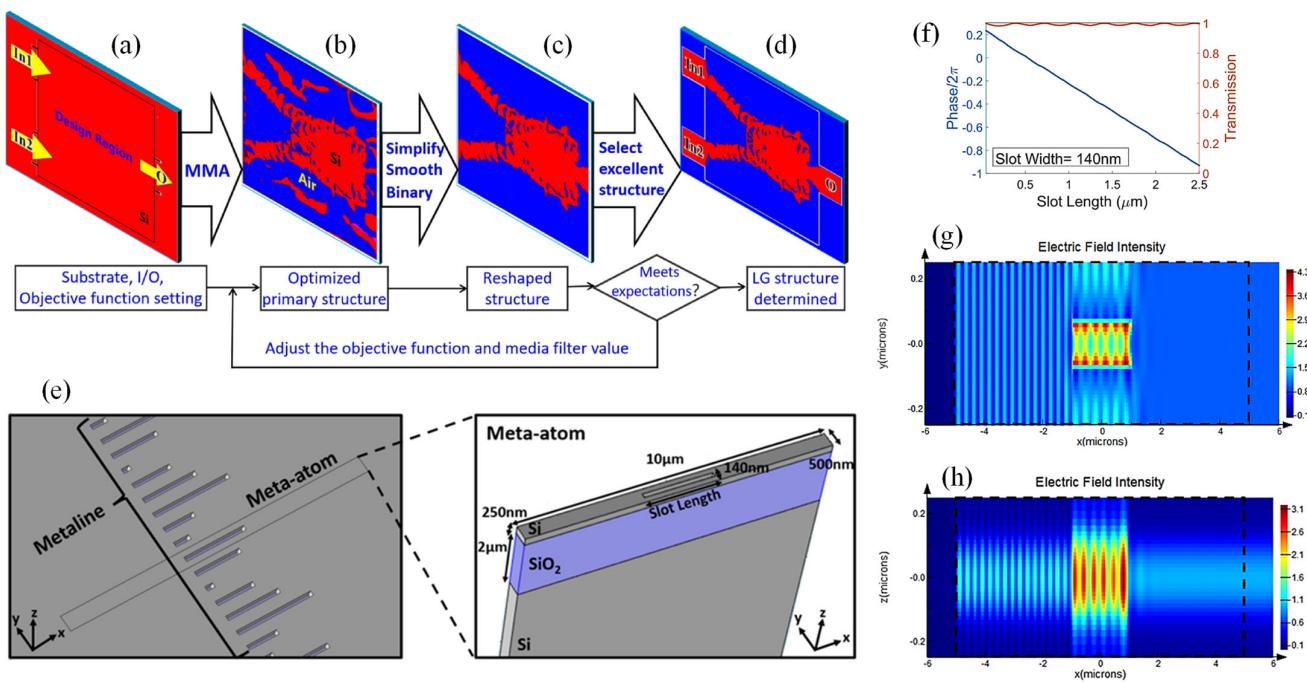


Figure 6. Design process for Si-based AO-LGs with a $2 \mu\text{m} \times 2 \mu\text{m}$ footprint: (a) initial substrate, (b) optimized structure, (c) reshaped configuration, (d) final design [124]. (e) Diagram of a metaline with meta-atoms, each containing a subwavelength slot whose length is a learnable parameter [125]. (f) Varying the slot length from 100 nm to 2.3 μm while keeping the width at 140 nm and height at 250 nm allows continuous phase tuning from 0 to 2π with amplitude above 0.96. (g) Electric field intensity in the x-y plane of a meta-atom with a 2 μm slot at the Si slab's mid-plane ($z = 0$). (h) Electric field intensity in the x-z plane across the slot's mid-plane ($y = 0$) [125].

In [125], a versatile optical LG built on an on-chip diffractive optical neural network capable of executing fundamental logic functions like AND, NOT, and OR at a wavelength of 1.55 μm was proposed. It also demonstrated consistent performance across seven distinct wavelengths within a 60 nm bandwidth, enabling efficient parallel processing through wavelength-division multiplexing. The design focused on simplicity, seamless integration, minimal loss, energy efficiency, and broad operational bandwidth. The proposed optical architecture used an SOI platform consisting of metalines made up of meta-atoms arranged in series (Figure 6e). Each meta-atom, represented by a subwavelength slot, served as a weight element connecting layers through in-plane-wave diffraction and interference. By adjusting slot width, length, and height, precise control over transmitted amplitude and phase delay was achieved.

The SOI platform featured a 250 nm Si top layer and a 2 μm buried oxide layer, with metalines spaced at a 500 nm lattice constant. Slots were 140 nm wide, 250 nm high and their lengths ranged from 100 nm to 2.3 μm , allowing continuous phase tuning from 0 to 2π with a transmission amplitude above 0.96 (Figure 6f). The design wavelength was 1.55 μm . Simulation results, obtained using Lumerical FDTD, were derived by placing FDTD ports 10 μm apart along the x-axis, using the fundamental TE mode for excitation. Electric field intensity profiles illustrated TE wave transmission through a 2 μm -long slot (Figure 6g,h). This innovative approach offered a promising solution for creating high-speed on-chip nanophotonic processors, essential for the next generation of optical computing technologies.

While optical computing and high-speed data processing showcase the ability of photonic LGs to handle large volumes of data with unparalleled speed and efficiency, their integration into large-scale network infrastructures is equally significant. In modern data

centers and optical networks, photonic LGs are driving innovations in traffic routing, signal switching, and bandwidth management—all critical for sustaining the ever-increasing global data demand.

5.2. Data Center Optimization and Optical Network Management

Modern data centers and telecommunication infrastructures are experiencing an exponential surge in data traffic [126,127]. Integrated photonic LGs help address this demand by enabling optical signal processing for switching, routing, and traffic management directly on photonic chips [128]. By eliminating the need for optical-to-electrical conversions, they reduce latency and power consumption in high-speed optical networks [129]. This leads to faster, more energy-efficient data transfer across cloud platforms, hyperscale data centers, and global internet backbones [20,130].

Dong et al. proposed a novel design framework for multi-character LGs using the method of moving asymptotes (MMA) to optimize basic logic units, which were then combined into complex gate structures [131]. This approach enabled the fabrication of three-character AND and OR gates ($2 \mu\text{m} \times 3 \mu\text{m}$) and four-character counterparts ($2 \mu\text{m} \times 4 \mu\text{m}$). The three-character AND gate exhibited a maximum CR of 19.411 across 950–1600 nm, while the OR gate reached 12.551 across 1200–1600 nm. Similarly, the four-character AND and OR gates achieved a CR of 9.269 (950–1550 nm) and 17.754 (1000–1600 nm), respectively. Unlike conventional binary gates, these multi-character LGs generate logic outputs directly without control ports, simplifying architecture and enhancing system performance. This methodology presents a promising direction for future photonic logic devices [131].

A new optical LG platform has been created using silicon nitride WGs embedded in polymer and controlled by thermal electrodes. This platform enabled the parallel execution of AND and OR logic operations on two-bit input signals (A and B). The binary input currents were applied to a subset of electrodes, while others acted as adjustable weights, influencing the light interference through the thermo-optic effect to determine whether the gate performs AND or OR operations [99]. The resulting logic outputs were converted into optical intensity variations at the output WGs. Simulations showed a nonlinear response of the light intensity to the applied currents, providing the ability to manipulate the optical field precisely. After fabricating the chip and integrating the system, 65,536 experiments were run automatically. The resulting data were processed by a sorting algorithm to identify the valid configurations from over 283 million possible input–weight–output combinations, ensuring they met the required truth table. The results for AND and OR gates in four distinct operation scenarios with varying contrast were presented. This simple, yet effective platform is cost-efficient and holds promise for applications in on-chip photonic computing and optical signal switching [99].

Figure 7a shows the architecture of the FPWE LG. Input signals A and B, each with two bits of logic (represented by two electrodes), were selected from the electrode matrix E. These signals are in the electronic domain as currents: low for logic “0” and high for logic “1.” The logic output C is determined by the optical intensity variations at the WG output O, resulting from multimode interference. The electrode sets for A [$E_{a1}, E_{a2}, E_{a3}, E_{a4}$] and B [$E_{b1}, E_{b2}, E_{b3}, E_{b4}$] can be chosen freely, but A and B must be independent (“ $A \cap B = \emptyset$ ”). The remaining electrodes in E form the weight matrix W, with current through them adjusted to achieve the desired truth table for AND or OR operations [99].

Figure 7b depicts the chip design. The MMI size is $7 \text{ mm} \times 110 \mu\text{m}$, with input and output WGs symmetrically placed around it. Eleven input WGs are positioned on the left, and any can serve as the carrier light injection port. These WGs are connected to taper structures to improve coupling with the multimode WG, with a $4 \mu\text{m}$ gap. Two output WGs can be chosen for the optical output C, and output tapers are placed with a $28 \mu\text{m}$ gap.

A network of 4×7 thermal electrodes, each with two $150 \mu\text{m} \times 150 \mu\text{m}$ pads, is arranged along the WG. Electrodes are labeled by row and column, with 1 mm gaps between columns in the x-direction. Each column contains 4 electrodes measuring $150 \mu\text{m} \times 8 \mu\text{m}$. The redundant WG ports and electrodes allow flexibility in designing different logic and switching devices with varying input–weight–output configurations [99].

The functional layout of the FPWE system is presented in Figure 7c, with Figure 7d capturing the system during active operation. Electrical signals are routed from the primary circuit board to the optical chip through an integrated adapter within the optoelectronic (O/E) subassembly. This adapter not only ensures signal transfer but also acts as a stable sub-mount, allowing for precise fiber alignment and secure wire bonding to connector pins. Due to the extremely thin electrode pads (approximately 100 nm) without any plating layer, a dedicated bonding technique using solder balls was developed to create a reliable connection between gold wires and the polymer-clad pads. The inset of Figure 7d provides a microscope image detailing this bonding process [99].

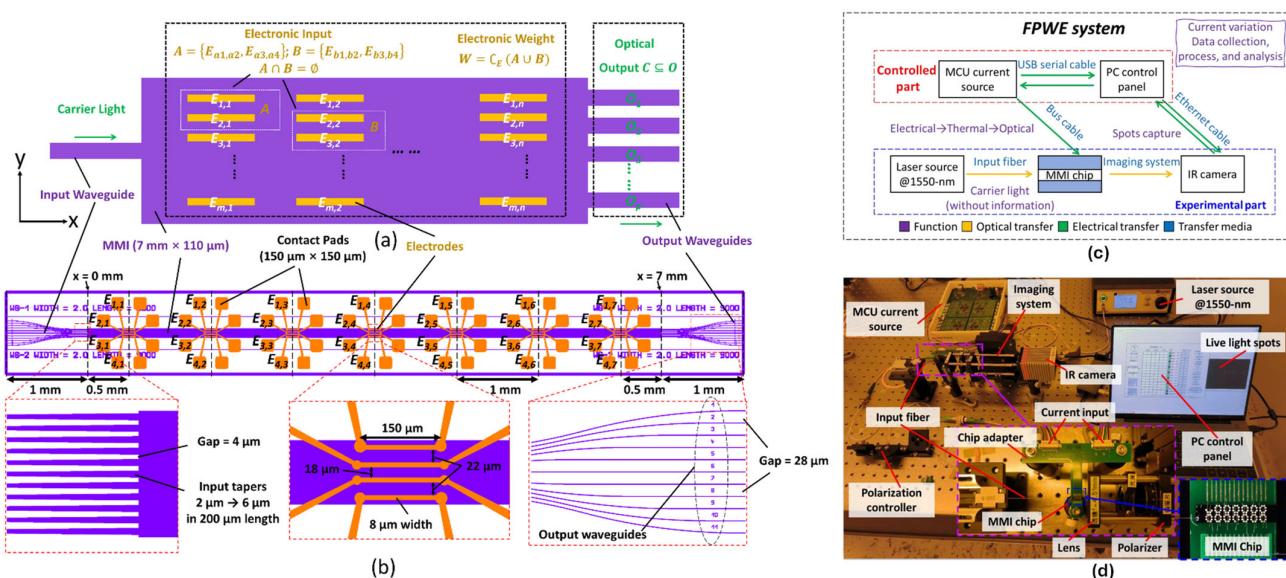


Figure 7. (a) Diagram of the FPWE functioning as a two-bit LG, featuring an optical path composed of input, multimode, and output WGs. Electronic inputs A, B, along with weight selections, are applied through the electrode network (E). The logic output (C) is represented by changes in optical intensity observed at two output ports (O). (b) The chip layout highlights the electrode network, with additional WG ports included for potential future expansion. The insets provide close-up views of the input tapers, electrode structures, and output WGs. (c) Conceptual illustration and (d) corresponding photograph of the FPWE system [99].

Beyond conventional data transfer and processing, integrated photonic LGs are also poised to revolutionize the future of secure and quantum information technologies. As the world moves toward quantum computing and ultra-secure communication, photonic devices are becoming indispensable for implementing quantum logic operations with high fidelity and scalability [120,132,133].

5.3. Quantum Information Processing and Quantum Communication

Photons stand out as ideal qubit candidates, particularly for long-range quantum information transfer, positioning them at the forefront of scalable, modular optical quantum computing that can function at room temperature. However, one of the key challenges in this field is the inherently low fidelity and probabilistic operation of two-photon quantum LGs, which imposes substantial overhead on fault-tolerant quantum systems [134,135].

While solutions like multiplexing and advanced error correction strategies help mitigate the randomness, the fidelity of these linear optical gates is fundamentally constrained by the limitations of single-photon sources. To address this, Shi et al. demonstrated a linear optical quantum LG with exceptionally high performance, achieving a truth table fidelity of 99.84(3)% and an entangling gate fidelity of 99.69(4)% using photon detection-based post-selection [136]. This success was largely attributed to a near-optimal Rydberg single-photon source, offering significant promise for scalable quantum photonic computing platforms that rely on robust single-photon and photon–photon gate operations.

In parallel, significant efforts have been directed toward implementing all-optical Boolean logic functions using quantum dot-based semiconductor optical amplifiers [137]. The researchers focused on the nonlinear behavior of these devices, incorporating factors such as carrier heating and spectral hole-burning into their rate-equation models. By utilizing the excited states of quantum dots along with the wetting layer as dual carrier reservoirs and leveraging ultrafast carrier relaxation times, the proposed setup enabled high-speed logic processing at rates up to 250 Gb/s [137].

In another advancement, De et al. introduced a novel all-optical quantum Toffoli gate design, fabricated on a two-dimensional Si–air photonic crystal platform [138]. The gate’s operation was based on carefully engineered interference effects, both constructive and destructive. The structure included an optical AND gate featuring two inputs and three outputs, as well as an optical XOR gate with two inputs and a single output. Two Y-junction power splitters were integrated into the input stage of the AND gate to manage signal distribution. Designed for operation at 1550 nm wavelength, this gate occupied a compact footprint of $50 \mu\text{m} \times 50 \mu\text{m}$ and was thoroughly analyzed through plane-wave expansion and finite-difference time-domain simulations. The simulation results validated the gate’s performance in terms of response time, CR, and logic reliability, all achieved without relying on nonlinear materials, highlighting clear advantages over prior designs [138].

He et al. recently demonstrated the development of ultracompact, universal quantum LGs on Si chips using an inverse-design approach [139]. The quantum photonic chip was fabricated on an SOI platform featuring a 220-nm-thick Si layer. As illustrated in Figure 8a, the chip architecture consists of four key functional modules arranged sequentially: (i) quantum source, (ii) state preparation, (iii) quantum gates, and (iv) state tomography. The core of this work centers on the inverse-designed quantum gates, which include a Hadamard gate, phase Z gate, and CNOT gate, shown in Figure 8b–d. Remarkably, the realized controlled-NOT and Hadamard gates are both approximately the size of a single vacuum wavelength, making them the most compact optical quantum gates reported so far. Furthermore, these fundamental gates were integrated into a quantum circuit capable of executing arbitrary quantum operations, with the overall footprint significantly smaller by several orders of magnitude than previously demonstrated quantum photonic circuits [139].

The experimental setup designed to evaluate quantum gate performance is outlined in Figure 8e. Two continuous-wave pump lasers, each operating at 35 mW and frequencies of $\omega_1 = 194.9 \text{ THz}$ and $\omega_3 = 195.3 \text{ THz}$, were combined and introduced into the photonic chip. Before coupling, their polarization states were carefully adjusted using polarization controllers and the beams were directed into the chip through a one-dimensional transverse electric grating coupler. As depicted in Figure 8a, these pump signals (marked by red and yellow arrows) entered the first module, where a multimode interference (MMI) coupler divided them into upper and lower Si WGs. Inside these 6 mm-long WGs, spontaneous four-wave mixing (SFWM) generated new photon pairs at a central frequency of $\omega_2 = 195.1 \text{ THz}$ (equivalent to a wavelength of 1536.61 nm). The phase relationship

between the two paths was controlled using phase shifters, producing an antibunched photon state after recombination at the second MMI [139].

The second module consisted of two MZIs paired with four phase shifters, enabling the creation of arbitrary single-qubit states encoded in optical paths. These generated qubits were then transmitted to the third module, which contained inverse-designed quantum LGs for experimental verification. The fourth module performed quantum-state tomography, employing MZIs and additional phase shifters to project and measure the output quantum states accurately. After processing, photons exited the chip via one-dimensional grating couplers and were directed into optical fibers for detection using superconducting nanowire single-photon detectors (SNSPDs).

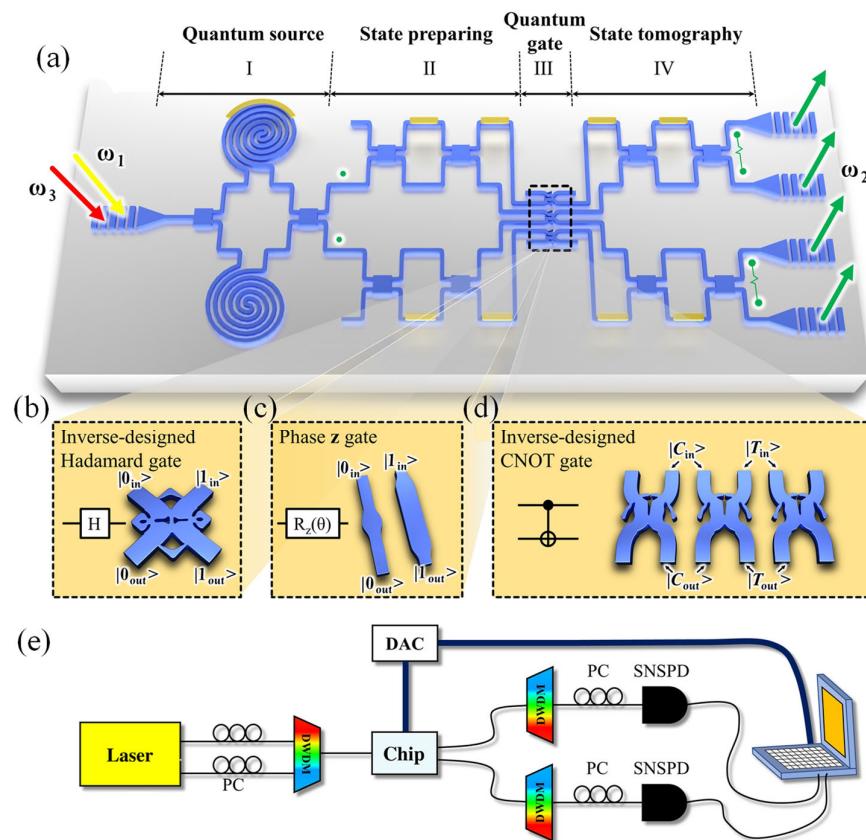


Figure 8. The inverse-designed ultracompact quantum LGs: (a) schematic of the photonic chip for measuring the quantum gates, (b) design of the Hadamard gate, (c) design of the phase Z gate, (d) design of the CNOT gate, (e) diagram of the experimental setup, featuring components such as the polarization controller (PC), digital-to-analogue converter (DAC), and superconducting nanowire single-photon detector (SNSPD) [139].

To ensure clean signal detection, two cascaded dense wavelength-division multiplexers (DWDMs) filtered out any residual pump photons. The chip also featured nine thermal electrodes, each controlled via a digital-to-analogue converter system, allowing precise phase tuning. Performance evaluation of the quantum gates was conducted by analyzing two-photon coincidence counts. This experimental demonstration represents a key step toward developing large-scale, integrated quantum photonic circuits with on-chip photon sources, paving the way for future advancements in quantum information processing technologies [139].

The synergy between photonics and quantum systems represents one frontier, but equally exciting developments are occurring in the field of neuromorphic computing and AI hardware acceleration. Here, integrated photonic LGs mimic neural structures to enable

high-speed, low-power computation tailored for machine learning and advanced pattern recognition. Section 5.4. explores how these devices are paving the way for intelligent, energy-efficient photonic processors.

5.4. Neuromorphic and AI Hardware Acceleration

AI refers to technologies that enable machines to perform tasks typically associated with human intelligence [140]. By analyzing large datasets, AI systems can carry out various tasks like detection, prediction, and complex modeling across multiple domains [1]. Its potential is evident in areas such as speech recognition, healthcare diagnostics, and self-driving cars, making AI a critical force in both technological progress and societal change. While conventional computing platforms like CPUs and GPUs are widely used for AI model training, the increasing demand for greater data processing power and the diminishing effectiveness of Moore's law have created a need for alternative architectures that provide faster processing with lower power consumption [141].

Application-specific integrated circuits (ASICs), such as Google's Tensor Processing Units (TPUs), have emerged as a leading solution for accelerating AI computations [142]. These chips are optimized to perform matrix–vector multiplication, a crucial operation in many machine learning algorithms, at a significantly faster rate than GPUs. Additionally, neuromorphic computing, which is inspired by the structure and function of the human brain, is attracting considerable interest. Unlike traditional von Neumann processors, which require constant data transfer between processing units and memory, neuromorphic systems allow for data to be processed directly in memory, often in parallel, and can mimic the spiking patterns of biological neurons, offering a more efficient approach for specific AI tasks [143].

Photonic LGs are increasingly being integrated into neuromorphic computing systems designed to emulate the neural structures of the human brain [144,145]. Their ability to perform weighted addition and thresholding operations optically makes them well suited for implementing neural network functions [146–148]. These gates can accelerate tasks such as pattern recognition, computer vision, and natural language processing, offering high-speed, energy-efficient alternatives to traditional AI accelerators, especially for edge computing and low-power devices [12]. Neuromorphic computing enables the development of energy-efficient computing systems, making it ideal for high-performance applications with low power consumption, such as edge computing, IoT devices, and autonomous systems. Singh et al. presented a neuron-based FPGA implementation using Verilog HDL [149]. LGs and combinational blocks were designed using single-layer and multi-layer perceptrons with a unit-step function. The proposed design was implemented on a Nexys 4 DDR FPGA board, developed using Verilog HDL in Xilinx VIVADO, and tested with various input values. The neural-based LGs and combinational blocks exhibited behavior comparable to conventional designs. This approach enhances neuromorphic VLSI system design by offering flexibility, adaptability, and ease of modification [149].

Parandin et al. presented a novel method for developing an all-optical AND gate utilizing a two-dimensional photonic crystal platform [150]. This design was aimed at advancing optical computing technologies by supporting high-speed data processing and efficient parallel operations. The gate featured a simple structure with two input ports and one output port, where the logical states were determined by light intensity: low output power represented logic 0, while high output power signified logic 1. To optimize the photonic crystal configuration and accurately achieve the desired logic function, artificial neural networks (ANNs) were employed during the design phase. The ANNs provided a systematic approach to refining structural parameters, ensuring that the gate performed with high precision and reliability. This combination of photonic crystal technology with

ANN-based optimization demonstrated a significant step forward in the design and realization of complex all-optical logic circuits. Experimental results confirmed clear signal distinctions between logic states, verifying the successful implementation of the AND gate concept [150].

In a related study, Hamed et al. explored the use of neural networks to design all-optical three-input XOR gates [151]. Their approach employed two different neural architectures: multilayer perceptron (MLP) and radial basis function (RBF) networks. Simulation-generated datasets representing all possible input and output power levels were used for training and evaluation. The data were split into 90% for training and 10% for testing. Both network types were assessed using key performance indicators such as mean square error (MSE), relative square error (RSE), and the correlation coefficient (R^2). Visual comparisons between predicted outputs and simulation data were also provided to demonstrate model accuracy.

Additionally, the research examined the effect of varying network parameters—such as the number of hidden layers, neuron counts, training epochs, learning rates, and Gaussian spread (in the case of RBF)—on the model's predictive performance. The RBF model delivered optimal performance with a Gaussian spread of 1 and 90 hidden neurons, achieving MSE, RSE, and R^2 values of 4.0837×10^{-4} , 0.0114, and 0.9888, respectively. The MLP model performed best with two hidden layers comprising 12 and 8 neurons (in a 5–12–8–1 architecture), trained over 65 epochs. By using logsigmoid functions in the hidden layers and a pure linear function at the output, the MLP model achieved excellent accuracy, with MSE, RSE, and R^2 values of 7.5×10^{-10} , 0.000133, and 0.9999, respectively. Although both models successfully simulated the all-optical XOR gate, the MLP network demonstrated higher accuracy and stability. These results highlight the potential of neural networks as powerful tools for designing advanced optical logic devices in future integrated photonic systems [151].

In another study, optical neural network LGs were investigated using both unsupervised and supervised learning methods [146]. It introduced two optical neuron structures: self-connection and interconnection configurations. The performance of AND, OR, NAND, NOR, and XOR LGs was analyzed, with simulation results showing that the interconnection configuration achieved a lower bit error ratio (BER) than the self-connection configuration. The OR LG achieved its best performance with a BER of 6.54%, while the XOR LG reached 4.89×10^{-5} . These results demonstrated that by adjusting the parameters of couplers and phase shifters, the proposed optical structure can effectively support various LG operations [146].

Jha et al. introduced an experimental strategy for realizing all-optical, reconfigurable nonlinear activation functions on a Si photonics platform, utilizing a cavity-loaded Mach-Zehnder interferometer (MZI) [152]. This device exploited the free-carrier dispersion (FCD) effect to dynamically tune and produce various nonlinear activation profiles, including sigmoid, radial basis, clamped ReLU, and softplus, all with customizable thresholds. Benchmark testing demonstrated impressive performance, achieving 100% accuracy on the XOR problem and 94% accuracy for MNIST handwritten digit classification, both validated through activation functions obtained from experimental measurements. The setup was designed as a nonlinear computing unit for photonic neural networks, providing adaptability for a broad spectrum of neuromorphic computing applications.

The neuron architecture incorporated key components such as weighting, summation, and nonlinear activation, as outlined in Figure 9a. The proposed optical design, presented in Figure 9b, integrated an MRR into one arm of an MZI, placed after a Mach-Zehnder coupler (MZC), allowing precise control over the activation behavior. An optical micrograph of the fabricated SOI device is shown in Figure 9c [152].

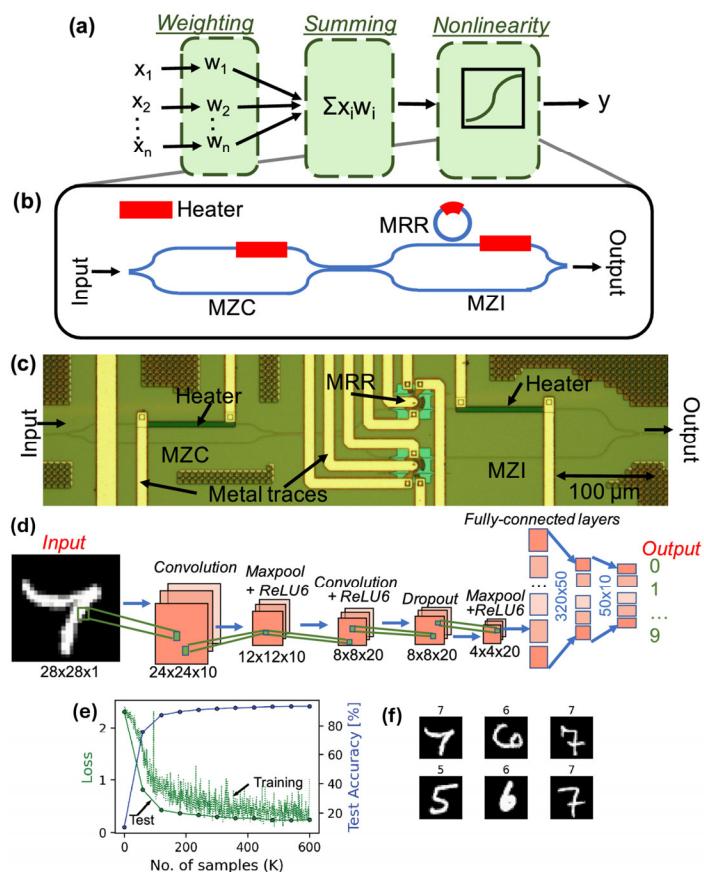


Figure 9. (a) Schematic representation of a neuron, depicting input weighting, summation, and nonlinear processing to produce an output, (b) diagram of the device, consisting of an MRR integrated into an MZI, placed after an MZC, (c) optical micrograph of the fabricated device on an SOI platform, (d) schematic of the MNIST classification network with convolutional layers, max pooling, ReLU6 activation, dropout, fully connected layers, and softmax output [0–9], (e) negative log-likelihood loss and test accuracy plotted against sample count, with each point representing an epoch, (f) Sample input images with predicted labels [152].

For evaluating the device in a practical machine learning scenario, a multi-class classification model was built for MNIST digit recognition, illustrated in Figure 9d [152]. The network employed an experimentally derived clamped ReLU, represented in training as a ReLU6 function. The MNIST dataset was split into training and testing sets with batch sizes of 64 and 1000, respectively. Training utilized stochastic gradient descent with a learning rate of 0.001 and a momentum factor of 0.5. Each input image was processed as a two-dimensional tensor normalized to the dataset's global mean (0.1307) and standard deviation (0.3081). The neural network pipeline consisted of convolutional layers, max-pooling layers, the experimental ReLU6 activation, followed by fully connected layers, and finally, a softmax output. Figure 9e tracks the negative log-likelihood loss during both training and testing phases, showing convergence within 10 epochs and achieving a final test accuracy of 94%. Additionally, Figure 9f showcases examples of input digits along with their accurately predicted classifications. Beyond classification tasks, these adaptable nonlinear optical activation functions hold potential for various artificial neural network applications [152].

Finally, security and privacy are critical in today's interconnected digital landscape. Integrated photonic LGs are not only advancing computational power but also enhancing secure communication protocols and cryptographic systems. The subsequent section

discusses their pivotal role in developing robust encryption, secure data transmission, and advanced cryptographic technologies.

5.5. Secure Communication and Cryptographic Systems

The inherent speed and interference immunity of photonic LGs make them well suited for secure communication protocols and cryptographic applications. On-chip photonic logic elements can perform complex encryption and decryption functions rapidly, enabling secure data transmission in military, financial, and critical infrastructure sectors [153]. Additionally, they play an essential role in optical steganography and secure multi-party computations, where privacy and data protection are paramount. A high-speed encryption and decryption scheme capable of operating at 160 Gb/s was introduced for secure optical network communication [153]. The design utilized XOR logic circuits based on semiconductor optical amplifiers (SOAs), integrated with a delay interferometer to overcome the limitations imposed by the slow carrier recovery of SOAs—a challenge that becomes more pronounced at elevated data rates. The performance of the proposed system was thoroughly assessed by analyzing key parameters, including the extinction ratio and quality factor. The findings indicated that this approach is not only practical but also ensures robust security at ultrahigh data transmission speeds.

Rachana et al. introduced a compact three-input AND LG designed using a two-dimensional PhC with a T-shaped WG structure, consisting of Si rods in an air medium [154]. The AND gate played a critical role in functions such as pattern recognition, error detection and correction, code conversion, secure data encryption and decryption, and arithmetic processing. The device's performance was evaluated through FDTD simulations at an operating wavelength of 1.55 μm . The simulation results revealed a strong CR of 24.533 dB, with the lowest CR recorded at 8.6 dB. The proposed structure achieved transmission efficiency ranging between 19.6% and 142%, along with an ultrafast response time of 26 femtoseconds, an insertion loss of 1.52 dB, and supports data rates up to 38.4 Tbps. These characteristics demonstrated the potential of the proposed design for high-speed and space-efficient optical signal processing applications [154].

Optoelectronic LGs (OELGs) hold significant potential as foundational elements for future logic architectures, with applications spanning LiDAR systems, advanced machine vision, and high-speed video processing. Achieving on-chip OELG operation at telecom wavelengths is critical for compatibility with Si-based optoelectronic platforms. Despite this need, current devices are generally limited to linear logic operations in the ultraviolet or visible ranges, and there remains a lack of versatile, high-performance OELGs capable of supporting multiple logic functions at telecom frequencies. He et al. presented a novel approach that integrated black phosphorus with Si WGs, enabling optoelectronic logic processing at a wavelength of 1550 nm [20]. By controlling optical inputs through multiple WGs and detecting electronic outputs, both linear logic functions—including AND, OR, NOT, NAND, and NOR—and more complex nonlinear operations such as XOR and XNOR were successfully realized. The devices demonstrated a responsivity of up to 0.35 A/W and operated with a 3 dB bandwidth of 230 MHz. In addition, composite logic operations were introduced by combining a photovoltaic OR gate with a voltage-controlled AND gate, allowing for multi-layer logic computing in the form of $(A + B)C$. These OELGs were further utilized to perform advanced functions such as symbol classification, edge detection, image fusion, and secure data processing. These findings open new pathways toward integrating multifunctional optoelectronic logic elements in next-generation computing systems [20].

LGs, including XNOR, NAND, and NOR, were realized by sequentially applying different input signal combinations (IN-00, IN-01, IN-10, IN-11), as demonstrated in Figure 10a–c. In addition, OELGs were employed to demonstrate a physical-layer en-

cription and decryption approach, illustrated in Figure 10d [20]. The XNOR gate was integral to comparison and decision circuits, supporting both address detection and secure data transmission. In this system, the text “UCAS” was first converted into ASCII format and used as one of the input signals (IN2), while the second input (IN1) functioned as a key. Passing these signals through the XNOR gate produced an encrypted output (Figure 10d(i)), which was then decrypted by feeding the encrypted signal back into the same gate (Figure 10d(ii)). This process demonstrated a low bit error rate, ranging between 10^{-7} and 10^{-8} .

One notable aspect of this system was its ability to operate effectively under free-space illumination. The XNOR function was successfully validated by focusing a light spot through an objective lens onto the device. Moreover, the WG chip design proved to be versatile and compatible with various 2D semiconductors. For example, an Au–InSe–Au device was integrated into the setup, enabling the execution of multiple logic operations, including OR, AND, and XNOR [20].

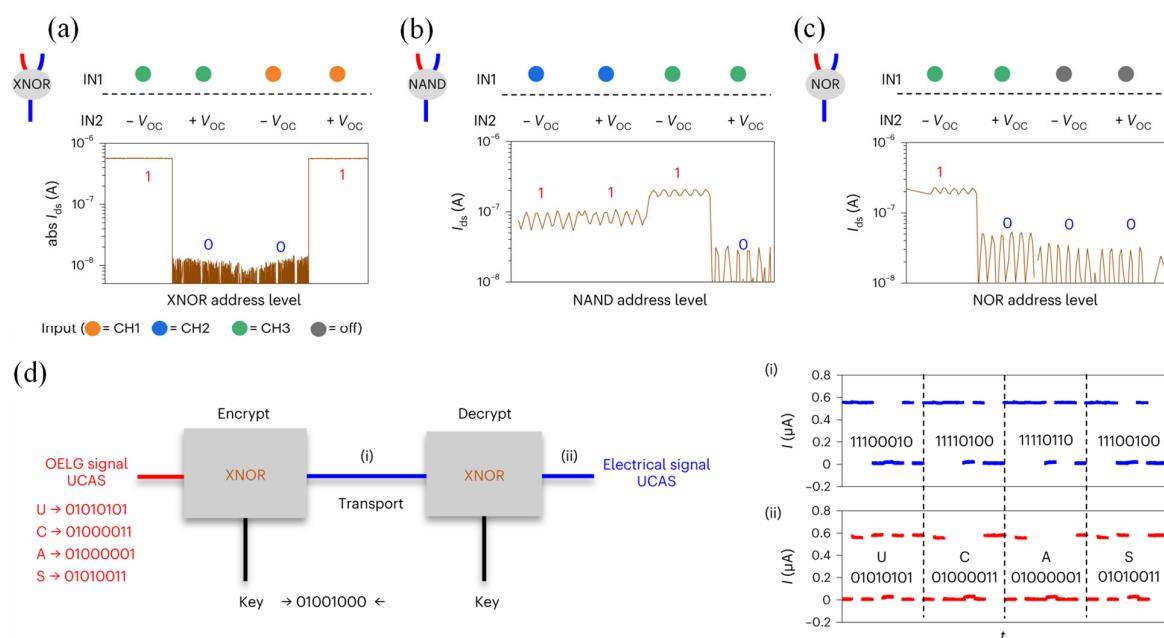


Figure 10. Experimental analysis of OELGs performing XNOR, NAND, and NOR logic operations within the telecom band. (a–c) Output current for the four possible input states of the XNOR (a), NAND (b), and NOR (c) gates. (d) Schematic on the left demonstrates the application of XNOR gates for signal encryption and decryption, while the experimental results on the right show the encrypted signal (i) and the decrypted signal (ii). Panel (t) represents the time axis [20].

6. Roadmap for Integrated Photonic LGs

The development of integrated photonic LGs has progressed through several key technological eras, each marked by distinct innovations in materials, architectures, and integration methods [155]. In the earliest stages, optical LGs were implemented using discrete, bulky components such as lenses, mirrors, and beam splitters [65,156,157]. These setups, though conceptually groundbreaking, were impractical for scalable applications due to size, alignment sensitivity, and energy inefficiency.

With the advent of silicon photonics in the early 2000s, a new phase of integration began. The compatibility of silicon with standard CMOS fabrication processes made it possible to realize compact, chip-scale photonic circuits. This milestone enabled early demonstrations of waveguide-based LGs that used interferometers and microring resonators [6,20,35]. However, limitations in nonlinear optical response and switching speed restricted their practical deployment.

The 2010s saw a significant leap forward, fueled by the emergence of advanced materials and fabrication techniques. Nonlinear materials such as silicon nitride and chalcogenide glasses, along with electro-optic materials like lithium niobate and indium phosphide, enabled higher-speed and lower-power photonic operations [52,58,70]. The introduction of O-PCMs, such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST), marked a turning point by allowing nonvolatile, reconfigurable photonic logic with high contrast and small footprints [60,61,84]. These materials also enable memory-assisted logic, an essential requirement for building optical computing platforms.

In the early 2020s, integrated photonic LGs began to evolve beyond proof-of-concept devices. The incorporation of inverse-design methodologies, machine learning optimization, and hybrid platforms (combining photonic and plasmonic elements) allowed researchers to drastically reduce device sizes, enhance transmission contrast ratios, and improve tolerance to fabrication variations [75,84,124]. LGs with footprints below $2.5 \mu\text{m}^2$ and extinction ratios exceeding 20 dB are now achievable. Concurrently, photonic LGs have begun to find meaningful applications in quantum computing, neuromorphic processors, AI accelerators, and secure communication systems [14,132,152].

Looking ahead to the next decade (2025–2035), the roadmap for integrated photonic LGs points toward several transformative goals. Monolithic integration of photonic and electronic circuits is expected to overcome current interfacing limitations and enable truly hybrid computation platforms [20,84]. Continued development of ultrafast, energy-efficient O-PCMs will likely yield high-performance photonic memories with sub-nanosecond switching speeds and improved endurance [60,61,87]. Advances in low-loss plasmonic structures and topological photonics may further enhance LG performance while reducing footprint and cross talk [38,39].

Additionally, the adoption of AI-assisted design workflows promises to revolutionize photonic circuit design by enabling automated, optimized architectures tailored for specific computational tasks [124,152]. As quantum technologies mature, photonic LGs capable of operating with single photons or entangled states will become essential components in scalable, room-temperature quantum logic platforms [136,139]. Together, these developments outline a clear trajectory toward the realization of practical, programmable, and massively parallel photonic computing systems that extend well beyond the limitations of traditional electronics.

7. Challenges and Prospects

Integrated photonic LGs, which utilize light rather than electrons to perform logical operations, face several significant challenges that limit their widespread implementation. One of the most critical issues is material limitations [158,159]. Photonic LGs rely on nonlinear optical effects to enable switching and logic operations, but most photonic materials used (like Si) exhibit relatively weak nonlinearities at low power levels. This often necessitates high optical power to achieve sufficient switching contrast, which contradicts the low-power advantage of photonics [160–162]. Additionally, scalability and integration present major obstacles. While integrated photonic devices have been demonstrated on small scales, building large-scale logic circuits requires precise alignment, low-loss WGs, and reliable interconnects, all of which increase fabrication complexity and costs [163]. Moreover, device footprint and miniaturization pose challenges due to the diffraction limit of light and the difficulty of compactly integrating multiple functional photonic elements on a single chip [164].

Another major challenge lies in thermal management and stability [165]. Photonic devices are sensitive to temperature variations, which can cause shifts in resonance wavelengths and degrade performance, especially in densely packed circuits [166]. Furthermore,

signal synchronization and coherence management are complex compared to electronic circuits. Optical signals propagate at the speed of light and lack inherent mechanisms for storage and synchronization, making it difficult to design photonic logic circuits that require sequential operations or feedback. Finally, compatibility with electronic control systems remains a hurdle. Although photonic logic offers speed and bandwidth advantages, it still requires efficient EO interfaces to communicate with traditional electronics, and these interfaces can introduce significant latency and power overhead [167].

Despite these challenges, the potential for integrated photonic LGs is promising, especially in areas where electronic circuits approach their fundamental speed and power limits [168–170]. The most compelling advantage is their potential to enable ultrafast processing speeds operating at frequencies far beyond those achievable by traditional transistors, thanks to the speed of light and the absence of parasitic capacitances. This capability opens new possibilities for real-time signal processing in applications such as optical communications, data centers, and high-performance computing [118,125]. Furthermore, photonic LGs have the potential for massive parallelism [99]: light waves of different frequencies (wavelengths) can propagate simultaneously without interference (wavelength-division multiplexing) [171], allowing for multiple operations to be performed in parallel within the same physical infrastructure.

In terms of materials, the development of new nonlinear materials and platforms such as Si–organic hybrids [172], III–V semiconductors [173], and two-dimensional materials like graphene [174] offer opportunities for stronger optical nonlinearities at lower power thresholds. Additionally, quantum photonics represents a transformative future direction, where photonic LGs could become fundamental building blocks for quantum information processing, leveraging photon entanglement and superposition. Another promising area is the potential for integration with neuromorphic computing architectures [175], where photonic circuits can mimic neural networks to perform analogue computation at ultrafast speeds with low energy consumption [145]. Overall, with advances in fabrication techniques, design methodologies, and hybrid integration technologies [176,177], integrated photonic LGs could play a vital role in next-generation computing systems that demand high bandwidth, low latency, and minimal energy consumption.

8. Concluding Remarks

This review highlighted the significant advancements in integrated photonic LGs, emphasizing their potential to revolutionize high-speed, energy-efficient computing, and optical signal processing. Through a detailed exploration of design methodologies, material innovations, and fabrication techniques, we have illustrated how key technologies such as photonic LGs leveraging EO materials, nonlinear optics, and optical phase-change materials are driving the evolution of integrated photonic circuits.

Despite the remarkable progress in this field, several challenges remain. The complexity of fabrication, the difficulty of integrating photonic and electronic systems, and the efficiency limitations of current materials present ongoing hurdles. Additionally, the miniaturization of photonic logic devices while maintaining high-speed, low-power operation requires further research and innovation. Addressing these issues will demand continued advancements in nanofabrication techniques, the discovery of new materials with enhanced optical properties, and the development of optimized circuit architectures.

Integrated photonic LGs are expected to play a transformative role in next-generation computing, optical communication networks, and AI acceleration. Their ultrafast operation and low energy consumption position them as a viable alternative to traditional electronic processors in specialized applications. Furthermore, the integration of photonics with emerging technologies, such as quantum computing and neuromorphic engineering,

presents exciting opportunities for future advancements. In conclusion, the evolution of integrated photonic LGs is paving the way for the next generation of computing and information processing. Overcoming current challenges will require interdisciplinary collaboration between optics, materials science, and semiconductor engineering. With sustained research and technological breakthroughs, photonic computing has the potential to redefine the landscape of digital processing, offering unprecedented speed, efficiency, and scalability.

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