All Optical Scalable Logic Gates Using Si$_3$N$_4$ Microring Resonators

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Abstract— In this paper microring resonator based logic gates are discussed that operate on same input and output wavelength. Same input and output wavelength allows the cascaded operation of the developed logic gates and thus can be utilized for developing photonic integrated circuits. Logic operations such as AND, OR, NOR, XOR and XNOR are successfully demonstrated. Optical Kerr effect is utilized for operation and structures are numerically simulated using coupled mode equations. Output power levels of around 0.18 W and 0.05 W are achieved for high and low power logic respectively. The proposed structures perform well for data rate under 1 Gbps and are analysed to determine the acceptable input range for high and low power logic respectively. The cascaded operation of proposed logic gates is also demonstrated.

Index Terms—All optical devices, Logic devices, Nonlinear optics, Optical Kerr effect, Resonators

I. INTRODUCTION

MICRORING resonator is a fundamental photonic device whose intrinsic properties makes it an obvious choice as an optical filter. A simple ring resonator is a circular waveguide that operates on the principle of total internal reflection and interference. To couple light from outside world to the ring, bus waveguides are employed and hence a ring resonator can be used in certain configurations such as an all pass filter and an add drop filter [1].

Microring ring resonators are useful for the development of photonic integrated circuits because of their compact and planar structure. An additional advantage is the absence of back reflections which are major concern in Fabry Perot type cavities such as photonic crystals. As a result, microring cavities have been extensively utilized for the development of optical switches [2], all optical diode [3] with a special focus on optical logic gates. A microring resonator based all optical AND gate is reported in [4,5] that uses four wave mixing for operation. Two photon absorption based all optical

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AND/NAND logic gates using semiconductor microring resonators is described in [6]. Silicon microring resonator utilizing free-carrier dispersion effect to demonstrate AND/NAND operation is given in [7]. Thermo-optic effect in silicon microring resonator is used in [8,9] to demonstrate XOR and XNOR operation.

Previously proposed systems are all optical as they operate using light signals but have a limitation of different input and output wavelengths. This results in non-scalability of these systems. All optical logic gates having same input and output wavelengths is reported in [10] but that have a limitation of low output power. There is huge contrast between input and output power so those structures also cannot be used for developing highly scalable photonic integrated circuits. The output power level of the NAND gate described in [10] is enhanced in [11] which can be used to develop other logic gates as well.

In this paper, new structures based on microring resonators for all optical logic gates operating on single wavelength are proposed, that have considerably high output power, thus facilitating their cascaded operation. All logic gates described in this paper use optical Kerr effect for operation. The third order nonlinear effect is dominant at high optical intensities and has been utilized for optical switching purposes in silica micro cavity [12]. All the structures are numerically simulated using coupled mode equations defined for ring waveguides [13, 14]. CMT is powerful for calculating complicated photonic systems, when we already know the basic property of single cavity (i.e. Q and coupling etc.) .

The paper is organized as follows. Section II describes the design parameters and principle of operation. Structures of various logic gates are describes in Section III. Section IV describes the input power analysis and the speed analysis of the proposed gates. In Section V, we have demonstrated cascaded operation of proposed logic gates. Section VI concludes the paper. The mathematical equations used to numerically model the structures are discussed in the appendix A.

II. DESIGNS PARAMETERS

In this section we will discuss design parameters for logic gate structures of AND, OR, NOR, XOR and XNOR operation. We have used Si$_3$N$_4$ material in our work. It is chosen because it has high energy band gap of around 5 eV that allows Kerr effect to dominate over other third order nonlinear effects such as two photon absorption etc. Si$_3$N$_4$ has

a refractive index of 1.98. The nonlinear refractive index of the material is 2.4×10^{-15} cm^2/W [15]. The microring has a radius and width of 20 μm and 900 nm respectively. The bus waveguides have a length, width and height of 100 μm, 900 nm and 644 nm respectively. The mode volume is 1.45×10^2 μm^3. The unloaded Q factor of the cavity is taken to be 10^6. High Q value allows sufficient time for the mode amplitude to build up in the cavity and larger duration for light matter interaction.

The operation of the logic gates described in this paper is based on resonance shift of the cavity induced by the change in refractive index due to cross phase modulation arising due to Kerr effect. The change in refractive index for λ_1 is given by

$$\Delta n_{Kerr} = \frac{2n_2c}{nV}\left(U_{\lambda_1} + 2U_{\lambda_2}\right) \qquad (1)$$

where n is the refractive index of the material, n_2 is nonlinear refractive index, V is mode volume and U is the energy of mode in the cavity. Δn_{Kerr} for λ_2 can be obtained by switching $U_{\lambda1}$ and $U_{\lambda2}$ in equation (1).

As the refractive index increases, the resonance shifts towards higher side

$$\delta\lambda = \frac{\Delta n_{Kerr}}{n}\lambda_{res} \qquad (2)$$

where $\delta\lambda$ is the resonance shift and λ_{res} is the resonant wavelength.

Cavity has two resonances at 1550 and 1580 nm. We have used two different wavelengths in our system which are slightly detuned from resonance and are at 1580.01 nm (λ_1) and 1550.02 nm (λ_2) respectively. The logical inputs and the output of the gates are at λ_1. The signal at λ_2 is termed as drive signal and it is used to modulate logical inputs inside the cavities. Apart from that, we have used additional λ_1 signal at C4 of each logic gates that replaces λ_2 signal. Since it is not logical input we have addressed this signal also as drive signal. When the inputs (either the logical inputs or the drive) are applied, the refractive index of the cavity increases, which causes the cavity resonance to shift. If the resonance shift matches to the detuning of either logical input or drive signal, the respective signal gets coupled to the ring from bus waveguide and vice versa. The coupling also depends on the gap distance between bus waveguide and cavity and it must be adjusted accordingly.

For τ_{coup} = 150 ps, the resonance shift and output power obtained at the transmit port of a cavity is given in Table I.

In the proposed logic gates, to get high power at output the drive signal power is increased or decreased from 250 mW and the variation in power is compensated by adjusting τ_{coup} values to achieve desired resonant shifts. Table I is an indicator of how the cavity behaves when different input combinations are applied. Based on this principle of operation the authors have designed structures to carry out AND, OR, NOR, XOR and XNOR logic operations. All the gates described in this work are composed of five microring cavities.

TABLE I
Input power, cavity resonance shifts and output power

Signal Input 1 at λ_1 (mW)	Signal Input 2 at λ_1 (mW)	Drive Input at λ_2 (mW)	$\delta\lambda_1$ (nm)	$\delta\lambda_2$ (nm)	Signal Output at λ_1 (mW)	Drive Output at λ_2 (mW)
0(L)	0(L)	0(L)	0	0	0(L)	0(L)
0(L)	0(L)	250(H)	0.008	0.004	0(L)	190(H)
0(L)	250(H)	0(L)	0.014	0.027	40(L)	0(L)
0(L)	250(H)	250(H)	0.035	0.0205	220(H)	10(L)
250(H)	0(L)	0(L)	0.014	0.027	40(L)	0(L)
250(H)	0(L)	250(H)	0.035	0.0205	220(H)	10(L)
250(H)	250(H)	0(L)	0.023	0.045	230(H)	0(L)
250(H)	250(H)	250(H)	0.025	0.041	230(H)	210(H)

III. ALL OPTICAL LOGIC GATES

A. AND Gate

In AND operation when both the inputs are high, only then the output is high else the output is low. Fig. 1 (a) shows the logic gate structure and demonstrates the operation when both inputs are high. A detailed operation is discussed in Appendix B. In this structure, cavities C1 and C2 carry out the logic operation. C3 and C5 are the filtering cavities that filter out unnecessary λ_2 signal component. C4 replaces λ_2 signal with λ_1. As we know the logic gates have two logical inputs thus input 1 at C1 and input 2 at C2 serves that purpose. The drive signals used in the gates are used to modulate the input 1 and input 2. The logic operation takes place between input 1 and input 2 at λ_1, the drive signal just facilitates the operation. The window dimension in the figures of logic gate structures indicate the dimensions or the footprints of the logic gates i.e. how much area they will cover on chip. Fig. 1(b) shows the output of AND gate. The input combination used for all the gates described in this paper is 1100 and 0110, hence the output of AND operation is 0100.

It must be noted that cavity C3 in AND gate is used as a filtering cavity to smoothen the output obtained from C2. The logic gates may function without C3 as well but the output may not be that smooth so we have used an additional filtering cavity to filter λ_2 component. It is particularly necessary if we want to use this system for tandem connection.

The time taken for the signal to couple from bus waveguide to ring (τ_{coup}) is set in the simulation work for all the cavities. τ_{coup} gives the decay rate of power from bus waveguide to cavity and vice versa. We have utilized trial and error method to set τ_{coup} values. The fundamental idea used was how we want the cavity to behave. If we wanted strong coupling, we set low τ_{coup} values, and if we wanted less coupling we set high τ_{coup} values.

The values of τ_{coup} for AND structure are 70, 40, 170, 150 and 150 ps respectively. Input signal powers are fixed at 0.25 W. The drive signals at λ_1 and λ_2 have 0.30 and 0.56 W power respectively. Both input and drive signal are return to zero format with 60 % duty cycle. Output power achieved is 0.22 W for high power logic and 0.02 W for low power logic respectively.

B. OR Gate

In OR operation, the output is low only when both the inputs are low else high. Fig. 2(a) shows the structure of OR gate. Cavities C1, C2 and C3 perform the desired logic operation. C4 replaces λ_2 component with λ_1. C5 is the filtering cavity to filter out the λ_2 component at the output. The operation of OR gate can be understood on similar basis as that of AND gate. Fig. 2(a) shows the operation of OR gate when both the inputs are high. Fig. 2(b) shows the output of OR gate which is 1110.

The τ_{coup} values for the cavities in OR gate are 200, 150, 300, 150 and 150 ps respectively. The drive signal at λ_1 has power of 0.36 W. Two λ_2 drive signals are used in the structure having power of 0.25 W. Output power achieved is 0.20 W for high power logic and 0.05 W for low power logic respectively.

C. NOR Gate

NOR operation is opposite of OR operation i.e. when both the inputs are high output is low else high. Fig. 3(a) shows the structure of NOR gate. Cavities C1, C2 and C3 perform the desired logic operation. C4 replaces λ_2 component with λ_1. C5 is the filtering cavity to suppress the λ_2 component at the output. Fig. 3(a) shows the operation of NOR gate when both the inputs are high. Fig. 3(b) shows the output of NOR gate which is 0001.

The τ_{coup} values for the cavities in NOR gate are 70, 40, 200, 150 and 250 ps respectively. The drive signal at λ_1 has power of 0.42 W. λ_2 drive signals have power of 0.25 W each. Output power achieved is 0.22 W for high power logic and 0.02 W for low power logic respectively.

D. XOR Gate

In XOR operation, the output is low when both the inputs are identical i.e. both are either low or high. The output is high when the inputs are different. Fig, 4(a) shows the structure of XOR gate and Fig. 4(b) shows the output of XOR gate which is 1010.

The τ_{coup} values for the cavities in XOR gate are 150, 120, 200, 150 and 70 ps respectively. The drive signal at λ_1 has power of 0.49 W. The drive signals at λ_2 wavelength have power of 0.56 W and 0.38 W respectively. Output power achieved is 0.20 W for high power logic and 0.06 W for low power logic respectively.
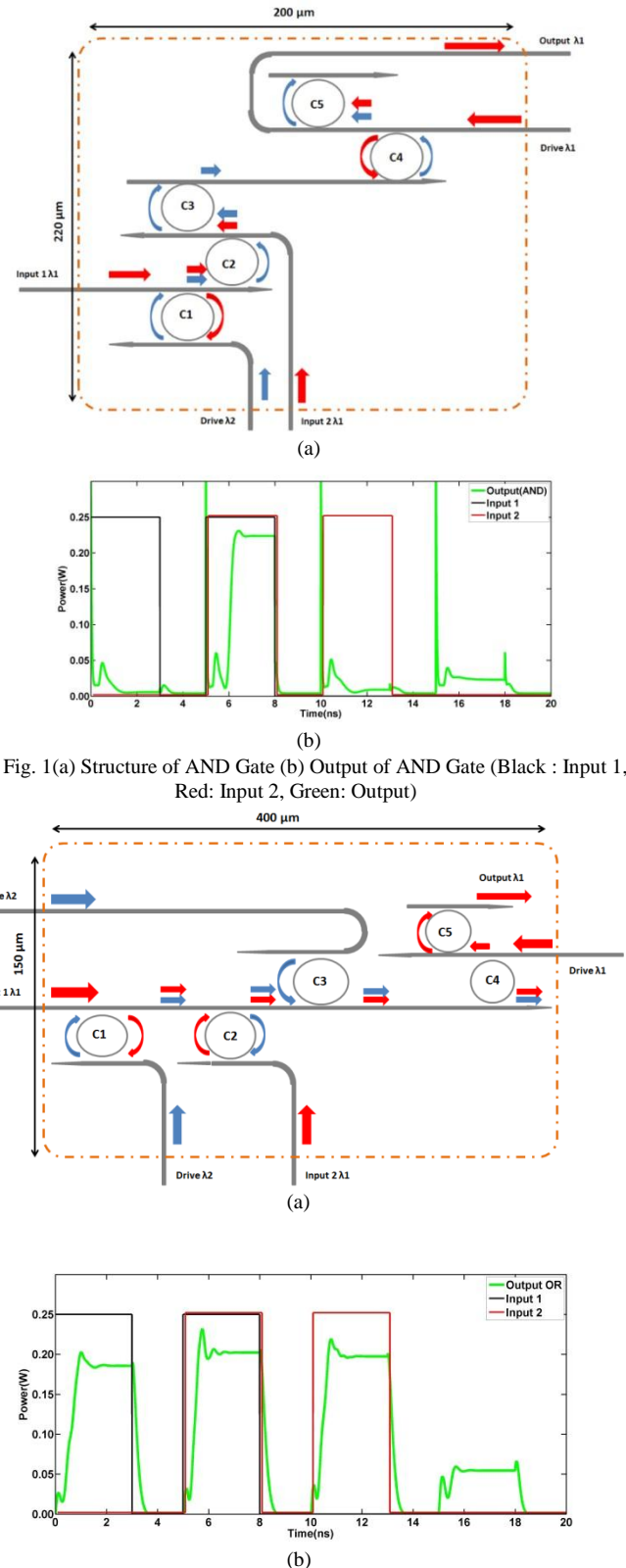
E. XNOR Gate

XNOR operation is opposite to XOR. The structure of XNOR gate is identical to NOR gate as shown in Fig. 3(a). Fig. 5 shows the output of XNOR gate which is 0101. The τ_{coup} values for the cavities in XNOR gate are 150, 100, 200, 150 and 180 ps respectively. The drive signal at λ_1 has power of 0.36 W. The drive signals at λ_2 wavelength have power of 0.56 W and 0.38 W respectively. Output power achieved is 0.24 W for high power logic and 0.02 W for low power logic respectively.

(a)

(b)

Fig. 1(a) Structure of AND Gate (b) Output of AND Gate (Black : Input 1, Red: Input 2, Green: Output)

(a)

(b)

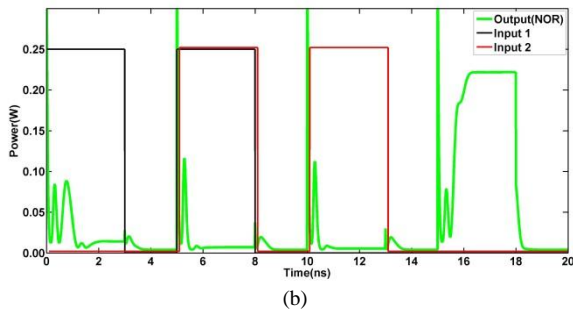Fig. 2(a) Structure of OR Gate (b) Output of OR Gate (Black : Input 1, Red: Input 2, Green: Output)
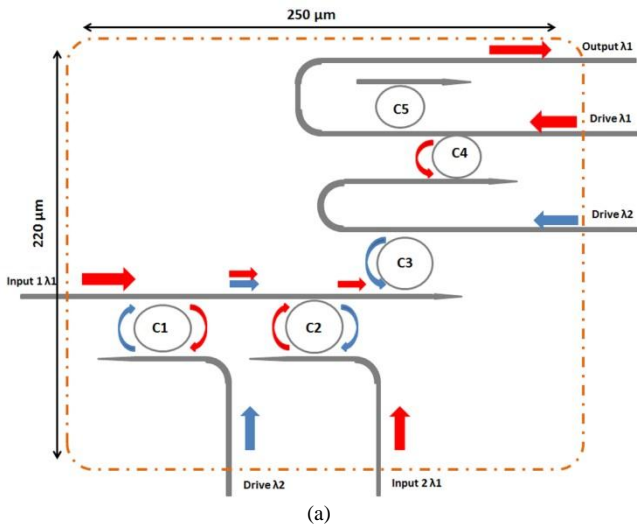
(a)

(b)

Fig. 3(a) Structure of NOR Gate (b) Output of NOR Gate (Black : Input 1, Red: Input 2, Green: Output)
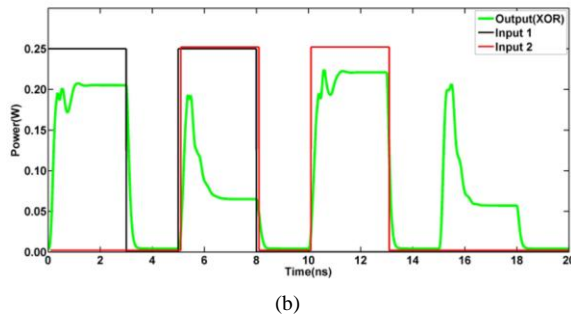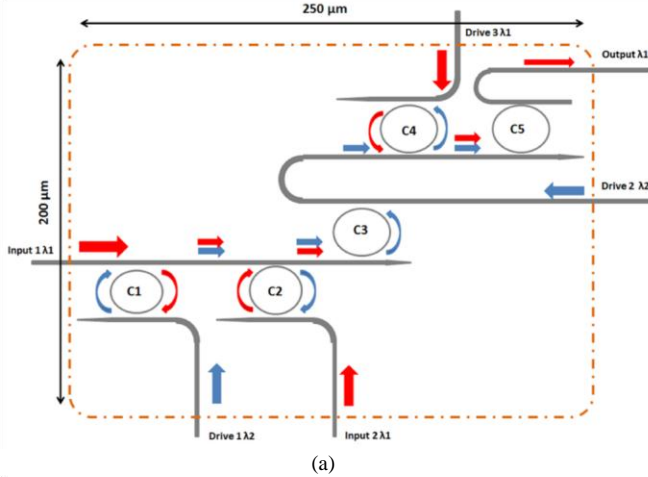

(a)

(b)

Fig. 4(a) Structure of XOR Gate (b) Output of XOR Gate (Black : Input1, Red: Input 2, Green: Output)
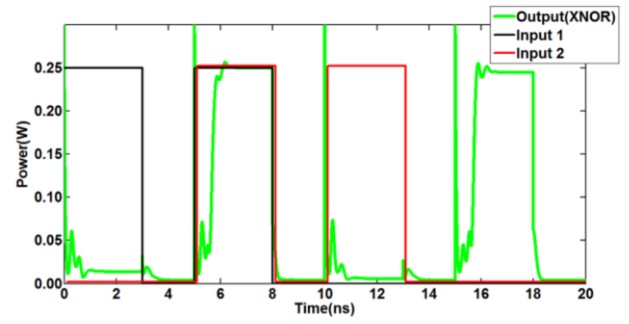

Fig. 5. Output of XNOR Gate (Black : Input 1, Red: Input 2, Green: Output)

IV. ANALYSIS OF DESIGNED GATES

Logic gates proposed in this paper were analyzed for input power range that can be accepted for high and low power logic respectively. The input power was varied from 0 to 360 mW and the change in output power was recorded. For AND gate, input power less than 25 mW can be taken as low power logic and input power greater than 200 mW can be taken as high power logic. Input power between 160-200 mW follows logic operation but suffers from low output duty cycle.

For OR gate, input power less than 40 mW can be taken as low power logic subjected that output power less than 60 mW corresponds to low power logic. Input power greater than 200 mW can be taken as high power logic to get sufficient output power for high power logic. For NOR gate, input power less than 8 mW can be taken as low power logic and input power greater than 122.5 mW can be taken as high power logic. This is depicted in Fig. 6 (a), (b) and (c) respectively.
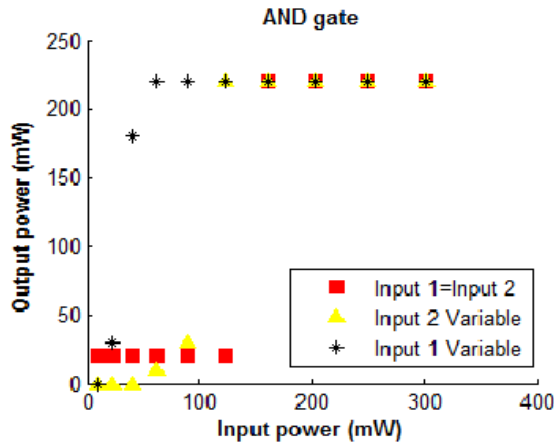
When we performed input power analysis for XOR and XNOR logic gates, we found that XOR structure can carry out AND, OR and XOR operations at different input power ranges. XOR logic gate can be used as AND gate for input powers lying between 22.5 mW and 62.5 mW. OR operation is achieved when input is between 90 mW and 160 mW. Above 200 mW, the structure performs XOR operation. Similar behavior is shown by the XNOR gate structure. When input power is between 40 mW and 90 mW, the structure behaves as NAND gate. When both inputs lie between 122.5 mW and 144 mW, NOR operation is obtained and when input is above 160 mW, XNOR operation is achieved.

We have also carried out the speed analysis of the proposed structures to determine the data rate which can be supported by the logic gates. Fig. 7(a) to 7(e) shows a graph between time taken by the output to reach stability and the input power for AND, OR, NOR, XOR and XNOR gate respectively.
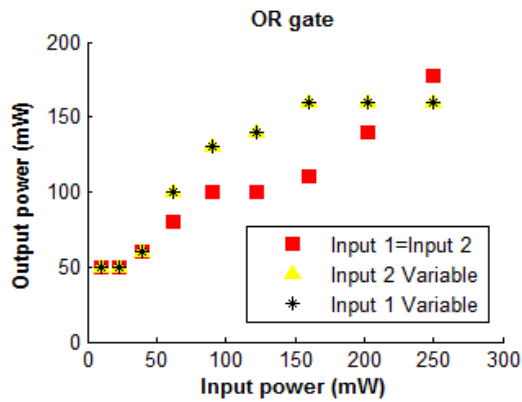
From Fig. 7(a) we see that, for AND gate, as we increase the input power, the time required for stability of output decreases and thus the gate can be operated at high data rate. For the proposed system operating at 250 mW input power, time taken for output stabilization is 1.2 ns thus the AND gate can operate at around 0.8 Gbps data rate. In OR, NOR, XOR and XNOR gates, the time required for stabilization of output is different for low to high transition and high to low transition as shown in Fig. 7(b) to 7(e). For OR gate, time required for output stabilization at operating input power of 250 mW is 1.1

ns, thus OR gate can operate at a data rate of 0.9 Gbps. Time required for output stabilization of NOR, XOR and XNOR gate is 1.2 ns, 1.3 ns and 1.2 ns respectively at 250 mW input power. Hence the date rate supported is 0.8 Gbps, 0.7 Gbps and 0.8 Gbps respectively.
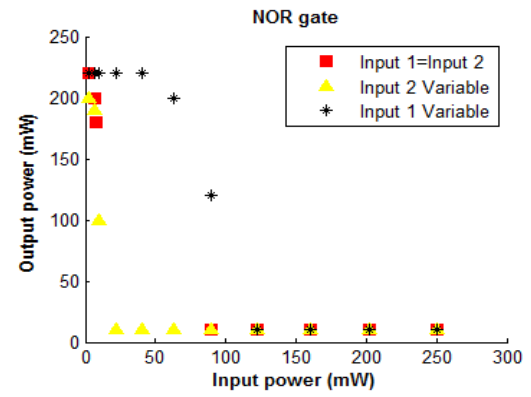
Although the speed of such system is ultimately determined by the photon lifetime of the cavities, it is much more complex. When the nonlinear cavity is pumped with a CW input, the transmittance usually exhibits an oscillation, whose period is much longer than the photon lifetime. The period of this transient behavior becomes shorter when the pump becomes strong. In our system, the loaded photon lifetime is about 150 ps, and therefore the system has the potential to operate at a maximum speed of >5GHz, but we scarify low-power operation. If we would like to further enhance the speed, we need to decrease the Q. But this also increases the operating power. Hence there are always a trade-off between operating speed and operating power.
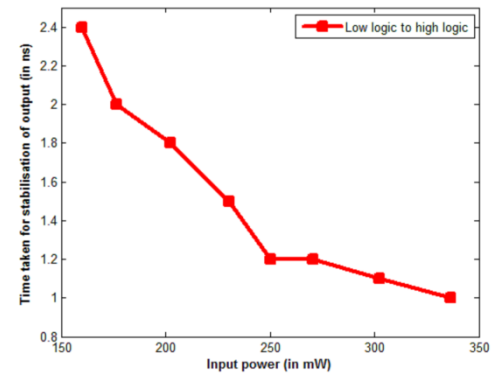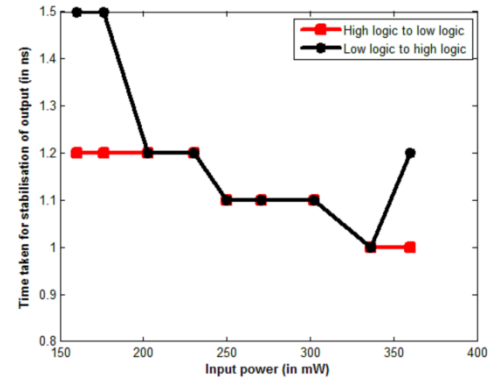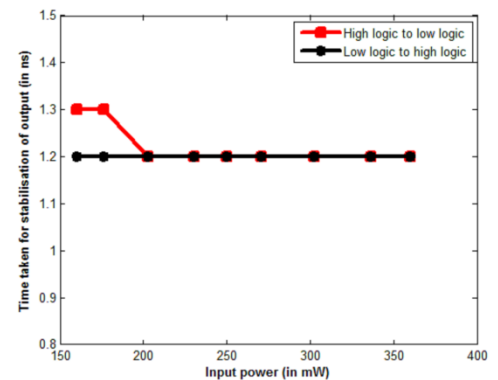

(a)

(b)

(c)

Fig. 6. Input power analysis for (a) AND gate (b) OR gate (c) NOR gate; Red square: Input 1 and Input 2 varied simultaneously, Yellow triangle: Input 2 is varied, input 1 is fixed at 250 mW, Black star: Input 1 is varied, input 2 is fixed at 250 mW
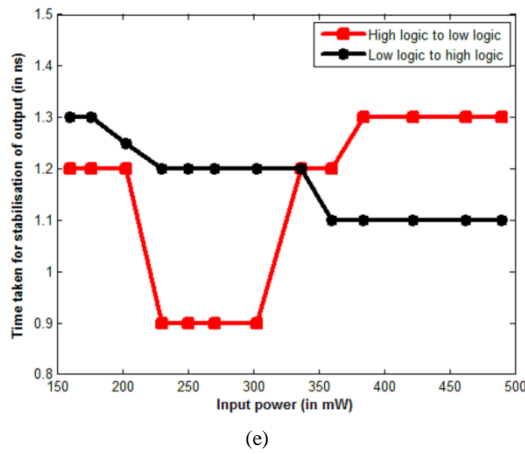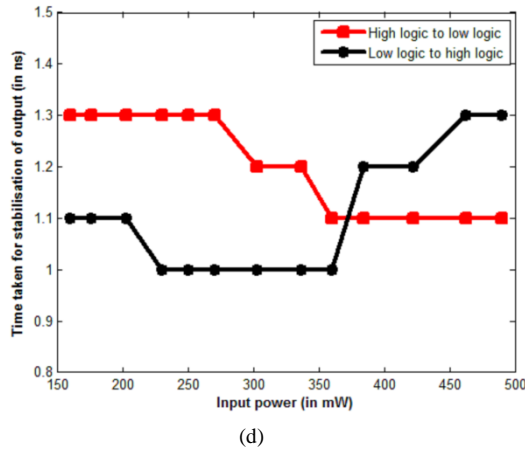

(a)

(b)

(c)

(d)

(e)

Fig. 7. Speed analysis of (a) AND gate (b) OR gate (c) NOR gate (d) XOR gate and (e) XNOR gate; Red line: Time taken for stabilisation of output when changing from 1 to 0, Black line: Time taken for stabilisation of output when changing from 0 to 1

V. CASCADED OPERATION

Logic gates proposed in this work have a very important advantage over other previously proposed architectures of operating on same input and output wavelength. This allows their cascaded operation i.e. the output of one logic gate can be fed to the input of following logic gate. In this section we have utilized the AND and NOR gate discussed previously to develop a NAND gate. Input1 and input 2 are given to the AND gate whose output is fed to the NOR gate. NOR gate is used in the configuration of an inverter. Thus it inverts the AND output and output of NAND operation is achieved.

Fig. 8(a) and 8(b) shows the schematic and output. Inputs are 1100 and 0110. Thus AND output is 0100 and final output is 1011 which corresponds to NAND operation. Output power of around 0.15 W is achieved for high power logic.

For the cascaded operation, pulse width is increased from 5 ns to 7 ns as the transients per cavity tend to accumulate and thus the output switching duration increases.
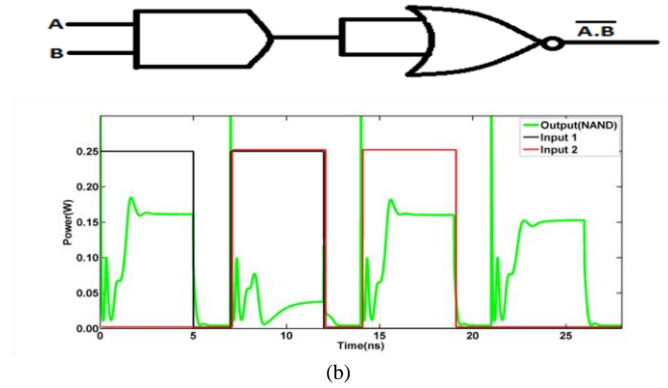

(b)

Fig. 8(a) AND gate cascaded with NOR gate (b) NAND output

CONCLUSION

In this paper, all optical logic gates based on Si_3N_4 platform are proposed. Si_3N_4 offers a very high band gap that facilitates Kerr nonlinearity and also suppresses other third nonlinear effects. It also has a very high nonlinear refractive index thus making it a potential candidate for our work. We have successfully demonstrated AND, OR, NOR, XOR and XNOR logic operations using five microring cavities. The developed structures are all optical since they use only light signal for operation. Major features of the proposed logic gates are their operating wavelengths and output power. High power at the output and same input and output wavelength facilitates the cascaded operation of the gates and thus can be utilized to develop scalable photonic integrated circuits in future. The input power in our work is 250 mW which can be significantly reduced using carrier plasma dispersion effect as demonstrated in [10].

The logic gates discussed in the paper operates on return to zero input. 60% duty cycle is chosen because it gives sufficient time to the cavity for relaxation and to return to original state for the next input. Other kind of input formats such as non-return to zero needs to be examined on developed structures.

It must be noted that in Kerr effect, at high input intensities, coupling between the ring and the waveguide reduces. In [16], the effect of nonlinear coupling is depicted for chalcogenide material in which the lateral coupling between the ring waveguides vanishes at 1.6 W/μm^2. Since this is very large value and the light intensities used in our work are not that much high we have assumed that the coupling efficiency does not change very abruptly. Besides we have used an air cladding in our structures and thus there is an air gap between the waveguide and the cavity. Therefore we can assume that coupling efficiency would not change very much even at higher power levels. Effect of nonlinear coupling needs to be investigated on the proposed logic gate structures.

APPENDIX A

A. Coupling coefficient between straight waveguide and ring waveguide

$$\kappa(s) = \frac{\omega \varepsilon_0 \cos\left(\frac{k_x w}{2}\right)(n^2 - n_0^2)}{2P(k_x^2 + \alpha^2)} \times \sqrt{\frac{\pi R}{\alpha}} \, exp\left(-\alpha\left(s + \frac{w}{2}\right)\right) \times$$
$$\left[\alpha \cos\left(\frac{k_x w}{2}\right)\sinh\left(\frac{\alpha w}{2}\right) + k_x \sin\left(\frac{k_x w}{2}\right)\cosh\left(\frac{\alpha w}{2}\right)\right] \quad (3)$$

where ω is the angular frequency of input light, k_x is transverse propagation constant, α is evanescent field decay constant in the cladding, w is waveguide width, n is refractive index of the waveguide, n_0 is refractive index of cladding i.e. air in this work, R is radius of cavity, s is gap distance between bus waveguide and ring waveguide, P is mode power given by

$$P = \frac{\beta}{2\omega\mu_0}\left(\frac{w}{2} + \frac{1}{\alpha}\right) \quad (4)$$

where β is the propagation constant. k_x and α are calculated as

$$k_x = \sqrt{n^2 k^2 - \beta^2} \quad (5)$$
$$\alpha = \sqrt{\beta^2 - n_0^2 k^2} \quad (6)$$

where k is the wave vector in vacuum.

B. Coupled mode analysis

The structures discussed in this paper are numerically simulated using coupled mode theory equations defined for ring waveguide. The coupled mode equations discussed in this work are taken from [14] with a slight modification. In [14] the input signal is given only from one port so the decay rate is τ where

$$\frac{1}{\tau} = \frac{1}{\tau_{loss}} + \frac{2}{\tau_{coup}} \quad (7)$$

In our work the input signal is given from both input as well as add port. Hence the decay rate is 2τ. Thus the time rate of change of ring energy is given by

$$\frac{da}{dt} = \left(j\omega_{res} - \frac{1}{2\tau}\right)a - exp(j\theta)\mu s_i \quad (8)$$

where ω_{res} is resonant angular frequency of the cavity.

Following the steps as given in [14] we get

$$\mu = \sqrt{\frac{1}{\tau_{coup}}} \quad (9)$$

Thus we get the equation

$$\frac{da}{dt} = \left(j\omega_{res} - \frac{1}{2}\left(\frac{1}{\tau_{loss}} + \frac{2}{\tau_{coup}}\right)\right)a - exp(j\theta)\sqrt{\frac{1}{\tau_{coup}}}s_i \quad (10)$$

where a is mode amplitude, τ_{loss} is photon lifetime in cavity, τ_{coup} is coupling to the waveguide, s_i is the input wave, d is length of bus waveguide and θ is relative phase between the mode amplitude in the cavity and the waveguide given as

$$\theta = 4\pi^2 nR\left(\frac{1}{\lambda_{res}} - \frac{1}{\lambda}\right) \quad (11)$$

λ_{res} and λ are resonant and input wavelength respectively.

The output at the transmit port according to [14] is
$$s_t = s_i - j\mu a \quad (12)$$
where $-j$ phase factor gives the relative phase between waveguide and the ring mode. In our work it is replaced by $exp(-j\theta)$. We have also introduced an additional term $exp(-j\beta d)$

that represents the phase shift experienced by signal between input and transmit port because of finite length d of the bus waveguide. Thus the equation becomes

$$s_t = \exp(-j\beta d)\left(s_i - \exp(-j\theta)\sqrt{\frac{1}{\tau_{coup}}}a\right) \quad (13)$$

Similarly the drop port output is given by [14]
$$|s_d|^2 = |s_i|^2 - |s_t|^2 \quad (14)$$

Putting s_t in the equation we get

$$|s_d| = \sqrt{\frac{1}{\tau_{coup}}}a \quad (15)$$

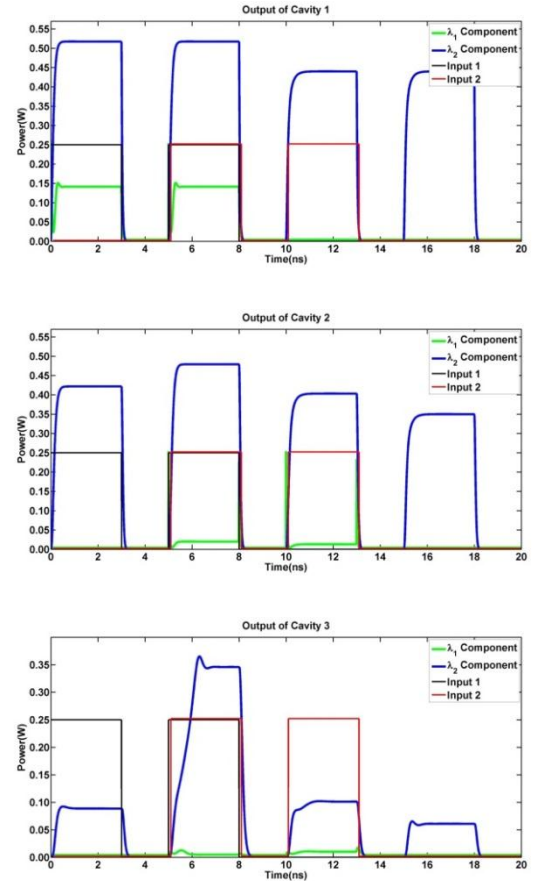Adding the phase shift due to bus waveguide

$$s_d = \exp(-j\beta d)\sqrt{\frac{1}{\tau_{coup}}}a \quad (16)$$

The coupled mode equations are simulated for each cavity separately with s_i changing for each cavity i.e. for cavity 1, where external inputs are applied, we have taken external inputs as s_i. For subsequent cavities, the outputs of previous cavities are taken as s_i.

APPENDIX B

AND Gate Operation

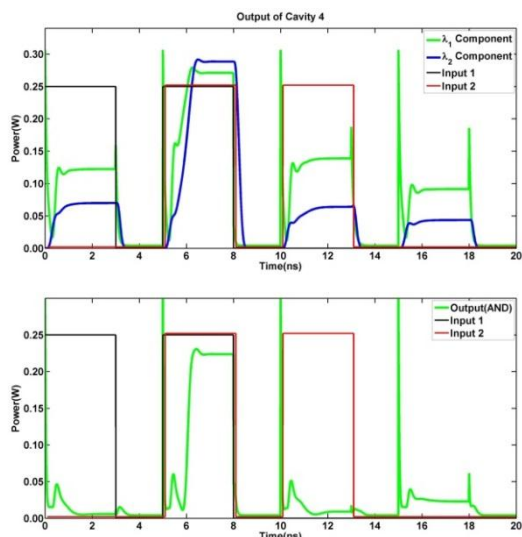Cavity wise operation of AND gate is given below in Fig. 9

Fig. 9. Cavity wise operation of AND Gate

It should be noted that Table I is not directly applicable here for cavity C1 and C2 because the power of drive signal at λ_2 is very high. Due to its high power and small gap distance for cavity C1 and C2, a part of λ_2 signal leaks into the cavity even when the cavity is off resonance. From cavity C3 onwards the principle of operation as described in Table I is closely followed.

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