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Photonic crystal integrated logic gates and circuits

LUIS PEDRAZA CABALLERO,[1,5] MICHELLE L. POVINELLI,[2] JHONATTAN C. RAMIREZ,[3] PAULO S. S. GUIMARÃES,[4] AND OMAR P. VILELA NETO[1,6]

[1]Department of Computer Science, Universidade Federal de Minas Gerais, Belo Horizonte 31270-901, Brazil
[2]Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, USA
[3]Department of Electronic Engineering, Universidade Federal de Minas Gerais, Belo Horizonte 31270-901, Brazil
[4]Department of Physics, Universidade Federal de Minas Gerais, Belo Horizonte 31270-901, Brazil
[5]lpedraza@dcc.ufmg.br
[6]omar@dcc.ufmg.br

Abstract: This paper presents and demonstrates the three logic processing levels based on complementary photonic crystal logic devices through photonic integrated circuit modeling. We accomplished a set of logic circuits including AND, OR, NAND, NOR, XOR, FAN-OUT, HALF ADDER, and FULL ADDER based on photonic crystal slab platforms. Furthermore, we achieved efficient all-optical logic circuits with contrast ratios as high as 5.5 dB, demonstrated in our simulation results, guaranteeing well-defined output power values for logic representations; a clock-rate up to 2 GHz; and an operating wavelength at $\lambda \approx 1550$ nm. Thus, we can now switch up for high computing abstraction levels to build photonic integrated circuits rather than isolated gates or devices.

1. Introduction

The physical limitation of conventional CMOS transistors miniaturization and the consequent downfall of Moore's Law have motivated an ongoing pursuit for emerging technologies to aid the development of computational systems able to support the demands of deep learning, big data, internet-of-things (IoT), autonomous driving, datacenters, cryptocurrencies, wearable systems, neuromorphic computing, and many other applications [1–5]. Low power consumption, high speed of data processing, and low energy dissipation are the main desirable features for the new generation of computers [6,7].

Photonics is an emerging technology capable of fulfilling digital electronics gaps and achieving the desired features mentioned before. Since its discovery and demonstration, Photonic Crystals (PhCs) appear as a promising platform to realize the fully optical processing information and computing [8–11]. The PhC ability to control electromagnetic waves, compactness, low power consumption and exceptional confinement of light has opened a large variety of applications for telecommunications, signal processing, biophotonics, and computing [12–16].

Within the domain of logic devices and circuits, some advances have been achieved based on different approaches. Examples of that are: logic gates based on self-collimation effects, multi-mode interference, waveguide interference paths, ring resonator, four-wave mixing, temporal solitons and nonlinear effects [17–32]. Despite the technological advances achieved in this area of knowledge, limitations to creating logical systems are evidenced due to the inability to concatenate gates to project circuits. The main obstacles identified are unequal input and output wavelengths, different power values to represent the same logic state, high input powers to achieve

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nonlinear effects, and weak output response [7,31,33]. We recently proposed Complementary Photonic Crystal Integrated Logic (CPCL) switches, aiming to cascade devices and build circuits [33]. This is a fundamental step towards the development of a completely photonic logic.

Considering the above, we applied the CPCL to address and demonstrate how PhC logic gates and circuits can be implemented by the adjacent connection of the proposed Switches N and P. Furthermore, our work solves some of the aforementioned drawbacks allowing us to project PhC universal integrated logic circuits rather than isolated devices or components. It means that we can now design any computational circuit for a wide range of applications by applying a similar methodology to the well-known and mature CMOS technology. This is a key point towards the realization of all-optical systems switching up from isolated components to circuits and reaching high computing abstraction levels. Thus, we perform reliable Finite-Difference Time-Domain (FDTD) simulations through the Lumerical FDTD Simulation tool to prove a complete set of logic gates and circuits including AND, OR, NAND, NOR, XOR, FAN-OUT, HALF-ADDER, and FULL-ADDER components. Furthermore, these PhC gates and circuits operate with the same input and output wavelength, have well-defined output power values to represent the logic states 0 and 1, and exhibit an ON-OFF contrast ratio higher than 5.50 dB. So, we ensure that our circuits achieve the main features to obtain practical devices for fabrication, enabling large-scale circuit integration [7]. In accordance with what was previously described, the results presented in this work open up new possibilities for future research on PhC logic circuits and systems.

This manuscript is organized as follows: In Section 2 we present the study of the input and output power values for the CPCL. In Section 3 we address how CPCL is used to model PhC logic gates and circuits and provide numerical simulations to demonstrate it. Section 4 discuss the main results of this work and compare them with the most recent advances in this field. Finally, Section 5 gathers the main conclusions.

2. Photonic crystal switches N and P

We previously proposed the Complementary Photonic Crystal Logic Devices (CPCL) [33], where the efficient operation of the Switch N (SwN) and Switch P (SwP) were demonstrated. These devices are PhC equivalents to the NMOS and PMOS transistor of the CMOS technology.

As a rule of thumb, our adopted PhC configuration is composed of a triangular lattice of holes embedded in a dielectric heterostructure substrate of GaAs/AlGaAs with effective refractive index n_{eff} = 2.87. The heterostructure consists of a 500 nm GaAs core with 180 nm of $Al_{0.25}Ga_{0.75}As$ cladding on top and downsides, and a 1500 nm buffer of $Al_{0.6}Ga_{0.4}As$. Its n_{eff} was theoretically derived by performing an extensive modal analysis which ensures single-mode propagation and strong confinement of the fundamental TE00 mode. The radius of holes and the lattice constant are 130 nm and 420 nm, respectively. The aforementioned configuration obtained for the PhCs guarantees a photonic bandgap between 1290 nm to 1670 nm. The complete design of the slab heterostructure is detailed in Ref. [33].

The SwN is composed of four terminals, called Input (In), Control (C), Output (O), and Drain (D). Its logic Output will have the same Input value if the Control is 1. Otherwise, it will be 0, as shown in Figure 1(a). We proved the operation of our PhC integrated SwN at ω_{op} = 193.45 THz of input and output operating frequency by setting up output power values greater than 50 mW and lower than 10 mW as logic 1 and 0, respectively [33]. On the other hand, the SwP is exactly the opposite of the SwN. Specifically, its logic Output will be the same as the Input if the Control is 0. Otherwise, it will be 0, as illustrated in Figure 1(b). The output power values obtained to represent the logic 1 and 0 were greater than 42 mW and lower than 12 mW, respectively [33].

Here we introduce a wide study of the switches output power responses to better describe the systems and achieve a proper setup for each PhC integrated gate and circuit. Therefore, we perform a set of simulations consisting of all the setups for the Input and Control sources from 0 to 80 mW with power steps of 5 mW.

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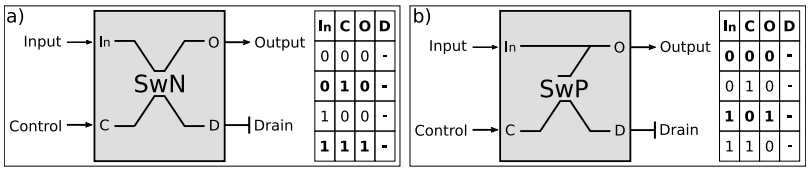

Fig. 1. Schematic representations of the CPCL Devices and the truth table for the logic outputs of both a) SwN and b) SwP.

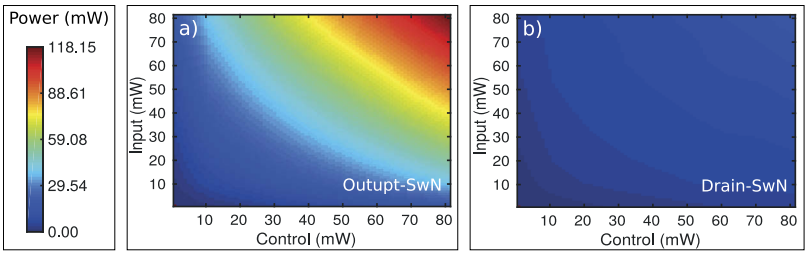

Fig. 2. Normalized SwN power response as a function of the Input (from 0 mW to 80 mW) and Control (from 0 mW to 80 mW) for the a) Output. The lateral color bar illustrates the maximum and minimum power values obtained at the Output of the SwN when the input setups SwN(80,80) and SwN(0,0) are carried out, respectively. b) Normalized power response to the maximum SwN Output value at the SwN Drain.

Figure 2 shows the output power response as a function of each Input and Control combination for both the Output and Drain of SwN. We can observe in Figure 2(a) that the greater the Input and Control, the greater the power value at the Output of SwN, reaching a power value of about 118 mW for the SwN(80,80) input setup. This result shows that the SwN operates as an optical amplifier since we can modulate the power at the Control to achieve the desired power value to represent a specific logic state. Figures 2(b) also shows an increase in the Drain value, but it is much smaller and can be neglected since it is not used in the logic datapath.

In the same direction, Figure 3(a) illustrates how the SwP output power changes as a function of the applied Input and Control signals. To represent the PMOS transistor, the Output is on only when the input is on, but the Control is off. Thus, for this instance, when the input setup SwP(80,0) is performed, the SwP Output achieves its maximum value, i.e., 63 mW. However,

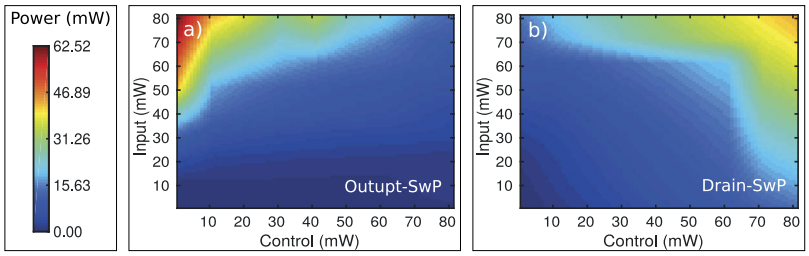

Fig. 3. Normalized SwP power response as a function of the Input (from 0 mW to 80 mW) and Control (from 0 mW to 80 mW) for the a) Output. The lateral color bar illustrates the maximum and minimum power values obtained at the Output of SwP when the input setups SwP(80,0) and SwP(0,0) are carried out, respectively. b) Normalized power response to the maximum SwP Output value at the SwP Drain.

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once the Control signal increases, the Output is turned off, decaying to a value of about 12 mW when the input setup SwP(80,80) is carried out. This fact demonstrates the ability of the SwP to operate as a signal reducer by applying the correct power signal at the Control source. Finally, Figure 3(b) shows the Drain power, which is also neglected in the circuits.

3. Modeling of the integrated logic gates and circuits

For the design of the gates and circuits applying the switches, we adopt the Finite-Difference Time-Domain (FDTD) method using the Lumerical FDTD Solution Tool to demonstrate the correct operation of the PhC circuits, thus ensuring accurate and reliable numerical simulations. First, we set the simulation Courant stability condition in 0.7 with a time step of 0.04 fs and space step of 0.02 μm. The Perfectly Matched Layer (PML) has a thickness of the order of the operating wavelength, i.e., about 1550 nm. Then, we divide the simulation space into three sections: Input (IS), PhC Processing Logic Unit (PPLUS), and Output (OS), as graphically described in Figure 4.

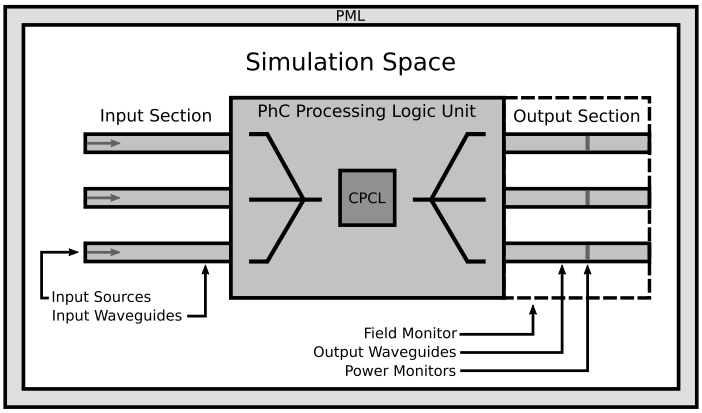

Fig. 4. Sketch of a typical simulation space of a PhC integrated circuit. It is divided in three sections: Input (IS), PhC Processing Logic Unit (PPLUS) and Output (OS).

In the IS, we place all input sources and input waveguides. So, to represent logic 1, we use a 50 mW Gaussian pulse centered at 193.41 THz (1550 nm) and a full-width of 0.24 THz. On the other hand, the absence of a light signal means logic 0. It is important to clarify that we define an Adapted Source Power (ASP), which is an adjustable reference signal to modulate the optical power levels into the system, maintaining the expected performance at the output. Its power value is derived empirically, and we will detail it below for each circuit. The PPLUS is the core of the circuit and where the logic takes place. In this sense, we string the Switches N and P to obtain the desired logic function at the output of our system. Finally, in the OS, we place the output waveguides and the field and power monitors. These monitors collect the field profile in the frequency domain from simulation results across some spatial region within the simulation in the FDTD. Essentially, the E (Electric field), H (Magnetic field), P (Poynting vector) and T (Transmission) as a function of frequency are calculated by applying a Fourier transform on the simulation time collected data. Here, we capture the intensity distribution at the steady-state at ω_{op} = 193.45 THz. In addition, we compute the power value at the output waveguides. Aiming to optimize the computational resources, the monitoring of the intensity distribution system will be carried out in OS. Later, we analyze the performance of our system, transforming the power response into a logic response. So, we define a high logic threshold (P_1) and power values to represent logic 1. In contrast, power values below the lower threshold (P_0) will represent the

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logic 0. Then, we proceed to calculate the ON-OFF contrast ratio (CR) of the device, as follow:

$$CR = 10Log_{10}(P_1/P_0)\ dB. \tag{1}$$

Following, we present the AND, OR, NAND, NOR, and XOR logic gates, plus the wire split FAN-OUT and the Half Adder and Full Adder circuits. It is important to highlight that all these logic gates and circuits are composed exclusively of switches N and P, our basic devices.

3.1. AND

A Switch N by itself can already be used as an AND gate. However, as one of the main goals of this work is to study cascaded switches, we designed a logic circuit based on two PhC SwNs connected in series. The resulting system has three inputs and three outputs terminals, as represented in Figure 5(a). In this, the ASP represents a fixed input with logic value 1. The resulting logic function for the Output (O) can be described as follow:

$$O = SwN(A, SwN(B, ASP)), \tag{2}$$

where A and B are the logic inputs. Thus, the logic output terminal of this circuit will be 1 only when the outputs of the two SwNs are 1. Otherwise, it will be 0. This system is equivalent to the AND logic function, O = A·B.

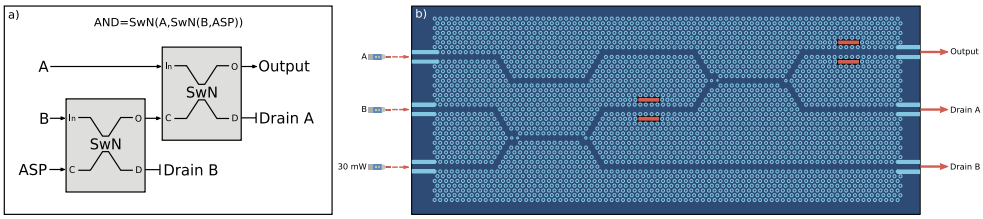

Fig. 5. PhC integrated AND circuit. a) Diagram of the AND circuit based on CPCL. b) Simulated structure of the PhC integrated AND circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

Figure 5(b) shows the schematic representation of the designed PhC integrated AND circuit. It has a footprint area of 37.38 $\mu m \times 16.00\ \mu m$. At this point, we set the ASP at 30 mW, which is a suitable value to achieve the desired logic states at the output. Figures 6(a-d) illustrate the OS normalized intensity distribution of the optical propagating mode of the PhC integrated AND circuit at the steady-state for the complete set of input combinations. The normalization rule consists of scaling the intensity by a factor $\delta = 1/max(A_h)$, where $max(A_h)$ is the maximum value of the intensity distribution with the higher output power. For this instance, $max(A_h)$ is obtained when the logic operation AND(1,1) = 1 is carried out. With this information, we can set power values greater than 50 mW and lower than 12 mW as logic 1 and 0, respectively. These values mean a CR of 6.19 dB for this gate. It also presents a clock rate of 12.5 GHz since it reaches the steady-state at 80 ps. The Drain outputs are disregarded. Thus, we demonstrate the correct operation of the PhC integrated AND gate.

3.2. OR

Our OR logic gate is based on a parallel arrangement of two SwNs, as represented in Figure 7(a). The logic output for this circuit is:

$$O = J(SwN(A, ASP), SwN(B, ASP)), \tag{3}$$

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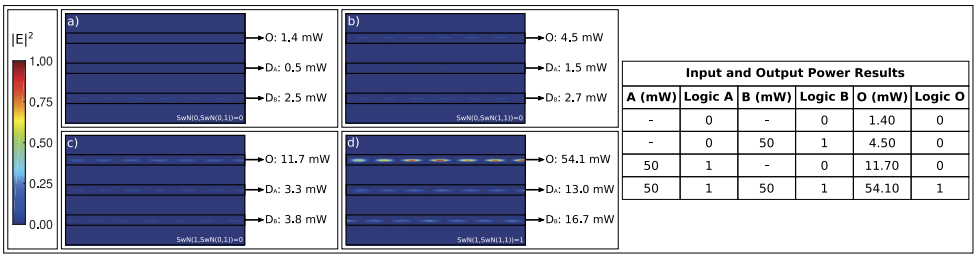

Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
-	0	-	0	1.40	0
-	0	50	1	4.50	0
50	1	-	0	11.70	0
50	1	50	1	54.10	1

Fig. 6. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) AND(0,0), b) AND(0,1), c) AND(1,0) and d) AND(1,1). The right-side table summarizes the input and output power results.

where A and B are logic inputs, while J represents the function of a PhC Y-junction. For this kind of PhC device, we found that the output power response is about 84% of the total input power applied. Thus, the logic output terminal (O) of the circuit will be 1 if any output of the SwNs is 1. Similarly, it will be 0 only when both of the SwNs outputs are 0. It is the equivalent circuit to the OR logic function, i.e., O=A+B.

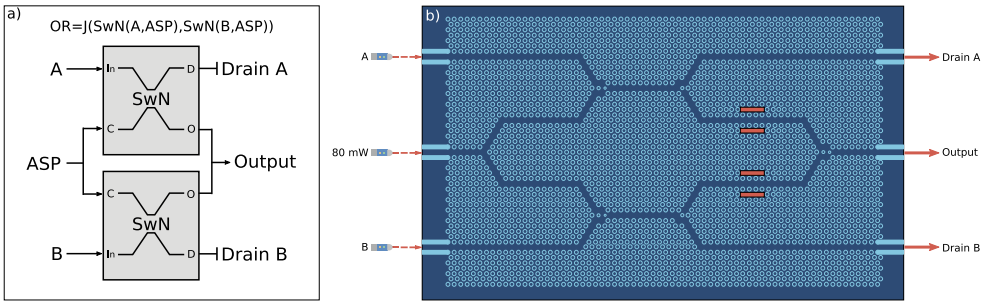

Fig. 7. PhC integrated OR circuit. a) Diagram of the OR circuit based on CPCL. b) Simulated structure of the PhC integrated OR circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

Figure 7(b) illustrates the design of the PhC structure equivalent to the OR circuit, with a footprint of 31.50 $\mu m \times 20.36\ \mu m$. Since the ASP path is split to both SwNs, we set its power at 80 mW. It is important to note that our PhC splitter divides the input power into two branches with about 43% each. Figures 8(a-d) show the OS normalized intensity distribution of the optical propagating mode for our OR circuit at the steady-state for the complete set of input combinations. So, we can appreciate that power values greater than 44 mW and lower than 6 mW represent logic 1 and 0, respectively. These values show a CR of 8.65 dB for this circuit. It also exhibits a clock rate of 12.5 GHz.

3.3. NAND

Aiming to obtain an all-optical NAND logic gate, we connect a SwN to a SwP, as can be seen in Figure 9(a), and whose logic output behavior can be described by (4).

$$O = SwP(ASP, SwN(A, B)). \tag{4}$$

The output of the PhC integrated NAND gate will be 0 when the output of SwN is 1; otherwise, it will be 1. Thus, it is analogous to the NAND logic function, represented by O = ¬(A·B). The

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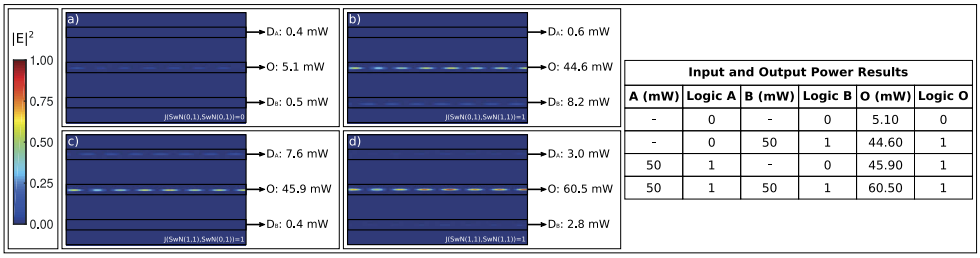


Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
-	0	-	0	5.10	0
-	0	50	1	44.60	1
50	1	-	0	45.90	1
50	1	50	1	60.50	1

Fig. 8. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) OR(0,0), b) OR(0,1), c) OR(1,0) and d) OR(1,1). The right-side table summarizes the input and output power results.

designed PhC structure for this circuit has a footprint area of 37.50 $\mu m \times 18.91$ μm, and its representative scheme can be seen in Figure 9(b). For this instance, we set the power value of the ASP at 70 mW. Figures 10(a-d) show the OS normalized intensity distribution of the optical propagating mode of the PhC integrated NAND circuit at the steady-state for the complete set of input combinations. Thus, power values greater than 45 mW and lower than 12 mW stand for logic 1 and 0, respectively. These values mean a CR of 5.74 dB for this circuit. It also presents a clock rate of 12.5 GHz, reaching its steady-state at 80 ps.

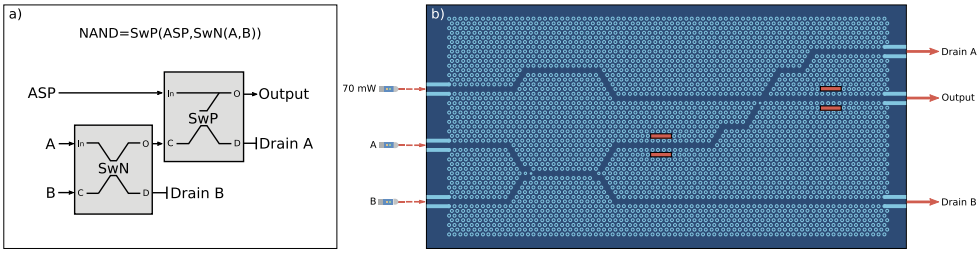
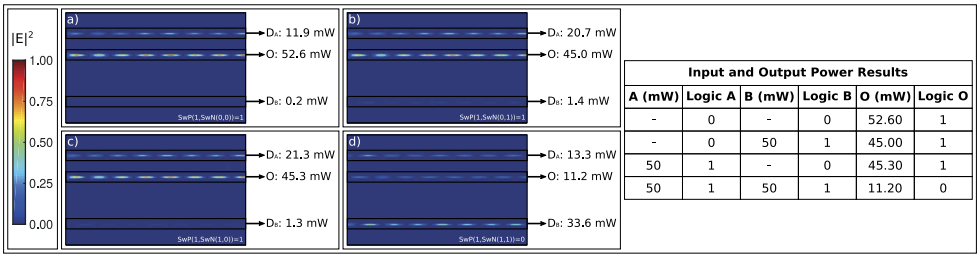


Fig. 9. PhC integrated NAND circuit. a) Diagram of the NAND circuit based on CPCL. b) Simulated structure of the PhC integrated NAND circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
-	0	-	0	52.60	1
-	0	50	1	45.00	1
50	1	-	0	45.30	1
50	1	50	1	11.20	0

Fig. 10. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) NAND(0,0), b) NAND(0,1), c) NAND(1,0) and d) NAND(1,1). The right-side table summarizes the input and output power results.

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3.4. NOR

Towards the realization of the PhC NOR logic gate, we connect two SwPs in series, as illustrated in Figure 11(a). The resulting system leads to a logic output described by the following equation:

$$O = SwP(SwP(ASP, A), B). \tag{5}$$

Thus, we obtain an equivalent to the NOR logic function, O = ¬(A+B), since the circuit output will be 1 only if both SwPs outputs are 1. Otherwise, it will be 0.

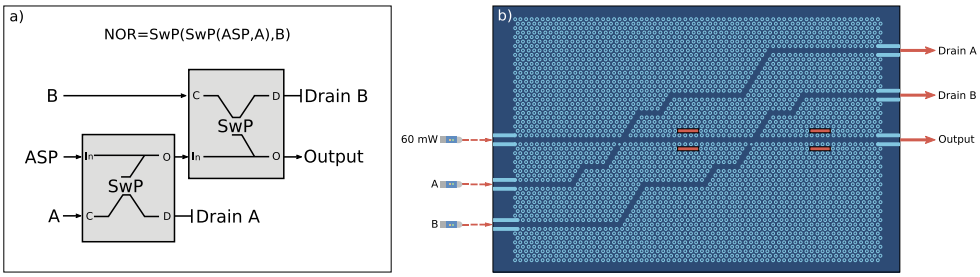
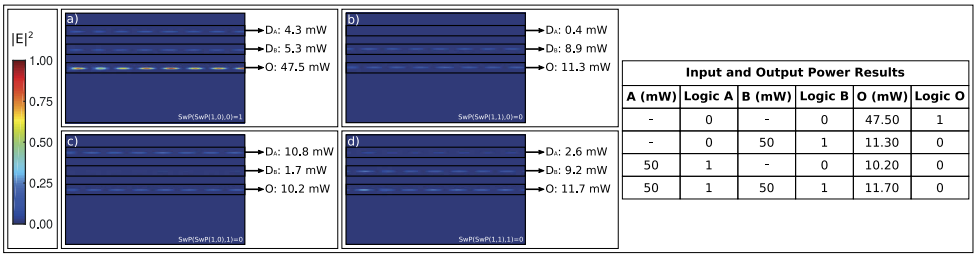


Fig. 11. PhC integrated NOR circuit. a) Diagram of the NOR circuit based on CPCL. b) Simulated structure of the PhC integrated NOR circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

Figure 11(b) shows the designed structure for the PhC integrated NOR circuit, which has a footprint of 31.08 $\mu m \times 21.82\ \mu m$. In this case, we set the ASP at 60 mW. Figures 12(a-d) show the OS normalized intensity distribution of the optical propagating mode of the PhC integrated NOR circuit at the steady-state for its input combinations. Power values greater than 47 mW and lower than 12 mW indicate logic 1 and 0, respectively. These values show a CR of 5.92 dB. This circuit also exhibits a clock rate of 12.5 GHz.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
-	0	-	0	47.50	1
-	0	50	1	11.30	0
50	1	-	0	10.20	0
50	1	50	1	11.70	0

Fig. 12. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) NOR(0,0), b) NOR(0,1), c) NOR(1,0) and d) NOR(1,1). The right-side table summarizes the input and output power results.

3.5. XOR

We achieve a PhC XOR logic gate by connecting two SwPs in parallel. The description of the logic output for our XOR circuit is given by:

$$O = J(SwP(A, B), SwP(B, A)), \tag{6}$$

where the logic output will be 1 if any output of the SwPs is 1, otherwise it will be 0. It is the equivalent circuit to the XOR logic function, i.e., O = A⊕B. It is important to note that the inputs

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signals swap for each SwP. Indeed, input A serves as the Input for the first SwP and the Control for the second SwP. In the opposite direction, input B operates as the Control for the first SwP and as the Input for the second SwP. This fact implies that an intersection path occurs between the input signals generating interference between the PhC waveguides. The correct operation and the performance of the PhC XOR circuit can be affected due to the 2D nature of our structure and mainly by the absence of a cross information device that avoids the previously mentioned interference signals. Thus, we adopt a simplified dual-rail strategy consisting of replicating the input signals to prevent the undesired interference and intersection between the input sources. Figure 13(a) shows the diagram of the final setup to achieve the PhC integrated XOR circuit.

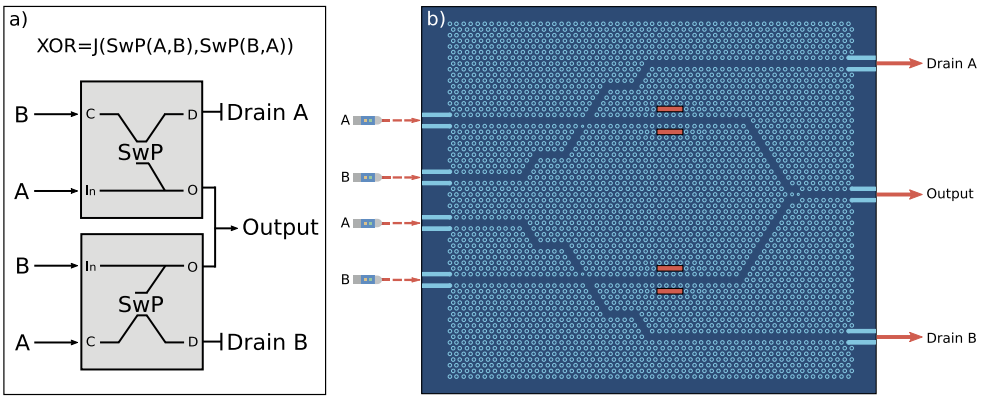
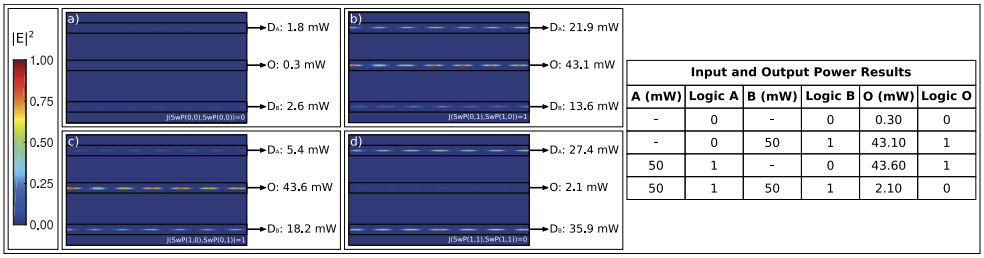


Fig. 13. PhC integrated XOR circuit. a) Diagram of the XOR circuit based on CPCL. b) Simulated structure of the PhC integrated XOR circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

Figure 13(b) illustrates the simulated structure for the PhC integrated XOR circuit, which has a footprint of 27.30 $\mu m \times 24.73\ \mu m$. Furthermore, Figures 14(a-d) show the OS normalized intensity distribution of the optical propagating mode at the steady-state for the complete set of input combinations of this circuit. Accordingly, we set power values up to 43 mW and down to 3 mW to represent logic 1 and 0, respectively. These values mean a CR of 11.56 dB for this circuit. It also presents a clock rate of 12.5 GHz.



Input and Output Power Results					
A (mW)	Logic A	B (mW)	Logic B	O (mW)	Logic O
-	0	-	0	0.30	0
-	0	50	1	43.10	1
50	1	-	0	43.60	1
50	1	50	1	2.10	0

Fig. 14. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) XOR(0,0), b) XOR(0,1), c) XOR(1,0) and d) XOR(1,1). The right-side table summarizes the input and output power results.

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3.6. FAN-OUT

In this section, we implemented a circuit to split a signal in two without losing value. This is a fundamental device to drive logic gates connections in a circuit. It was designed based on two SwNs, as can be seen in Figure 15(a), where the logic functions for each output (O1, O2) are described as follow:

$$O1 = SwN(ASP, In), \tag{7}$$

$$O2 = SwN(ASP, In). \tag{8}$$

Since the ASP will always be high, the output O1 and O2 will be 1 if the Input (In) is 1. Otherwise, they will be 0.

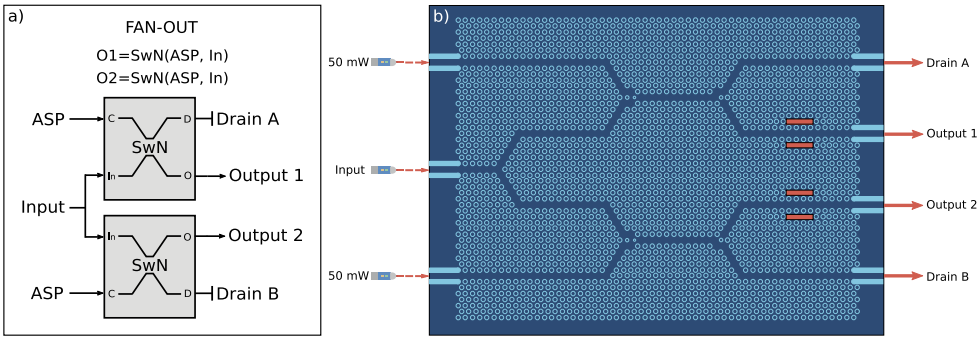
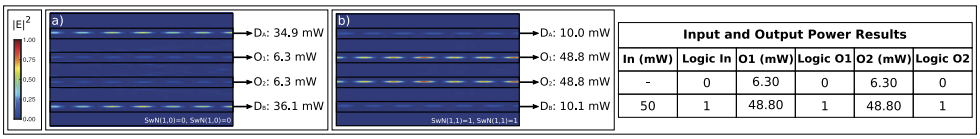


Fig. 15. PhC integrated FAN-OUT circuit. a) Diagram of the FAN-OUT circuit based on CPCL. b) Simulated structure of the PhC integrated FAN-OUT circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

Our simulated structure for the PhC integrated FAN-OUT circuit is illustrated in Figure 15(b). It has a footprint area of 26.46 $\mu m \times 20.36\ \mu m$. To achieve the desired power representations for logic 1 and 0 at the outputs, we set the ASP as 50 mW, which is enough power amount. Overall, Figure 16(a) and 16(b) show the OS normalized intensity distribution of the optical propagating mode at the steady-state for the complete set of input combinations. So, we define power values greater than 48 mW and lower than 7 mW as logic values 1 and 0, respectively. These values show a CR of 8.36 dB. This circuit has a clock rate of 12.5 GHz.



Input and Output Power Results					
In (mW)	Logic In	O1 (mW)	Logic O1	O2 (mW)	Logic O2
-	0	6.30	0	6.30	0
50	1	48.80	1	48.80	1

Fig. 16. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) Fan-out(0), b) Fan-out(1). The right-side table summarizes the input and output power results.

3.7. HALF ADDER

The half-adder (HA) is a circuit that adds two single binary digits (A and B) and produces two outputs (Sum and Carry), as can be observed in Figure 17(a). The resulting Carry and Sum are generated from the AND and XOR logic operations, respectively. HAs are commonly used in

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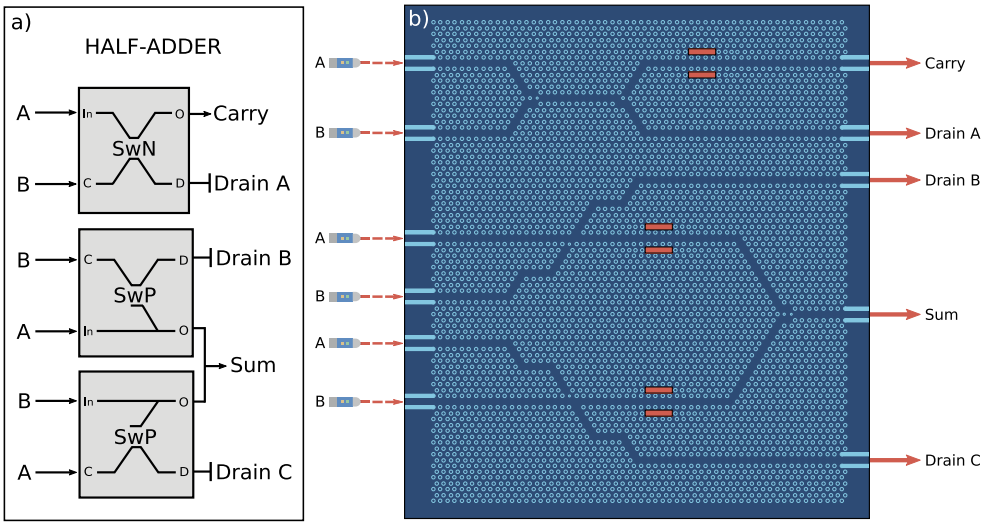
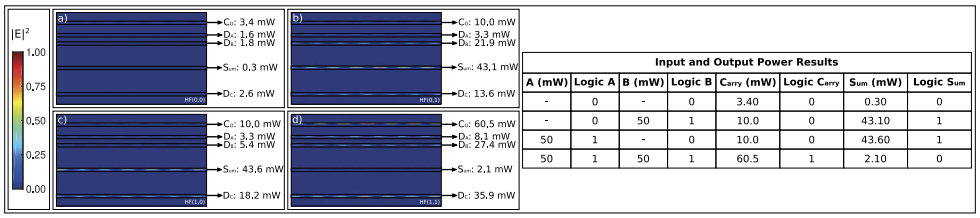


Fig. 17. PhC integrated Half-Adder (HF) circuit. a) Diagram of the HF circuit based on CPCL. b) Simulated structure of the PhC integrated HF circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

computers and microprocessors in the Arithmetic Logic Unit (ALU). As mentioned before, in Section 3.5, due to the absence of a cross-information device, we replicated the input signals.

The PhC structure for the HA circuit with a footprint of 27.30 $\mu m \times 32.00\ \mu m$ is presented in Figure 17(b). The OS normalized intensity distributions of the optical propagating mode at the steady-state for all input combinations are shown in Figures 18(a-d). Input and output power values are the same as the AND and XOR logic circuits. So, we can represent power values greater than 43 mW and lower than 12 mW as logic 1 and 0, respectively. These values indicate a CR of 5.54 dB for this circuit. The PhC integrated HA presents a clock rate of 12.5 GHz.



Input and Output Power Results

A (mW)	Logic A	B (mW)	Logic B	C_{arry} (mW)	Logic C_{arry}	S_{um} (mW)	Logic S_{um}
-	0	-	0	3.40	0	0.30	0
-	0	50	1	10.0	0	43.10	1
50	1	-	0	10.0	0	43.60	1
50	1	50	1	60.5	1	2.10	0

Fig. 18. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination a) HF(0,0), b) HF(0,1), c) HF(1,0) and d) HF(1,1). The right-side table summarizes the input and output power results.

3.8. FULL ADDER

The Full-Adder (FA) is a combinational circuit based on three inputs and two outputs, which computes the binary sum of two arbitrary numbers. It solves the limitation of the HA to handle the carry bit from the addition of two previous digits. So, we can string FAs together to create a byte-wide adder and cascade the carry bit from one FA to the next. In this work, for practical considerations and to reduce the computational cost to perform the simulations, we divided

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the PhC FA into two circuits, the CARRY, and the SUM, which are explained in the following sections.

3.8.1. CARRY

Our PhC-based Carry circuit for the FA has three logic inputs and one logic output (C_{out}), as follows:

$$C_{out} = J(SwN(A, SwN(ASP, C_{in})), SwN(B, SwN(ASP, C_{in}))), \tag{9}$$

where A, B are the two binary digits and C_{in} is the carry bit. In the Figure 19(a), it is possible to appreciate the CPCL circuit equivalents to the FA Carry circuit.

Figure 19(b) shows our designed structure for the PhC integrated FA Carry circuit, which has a footprint of 44.94 μm × 33.46 μm. For this circuit, we set the ASP as 50 mW. The OS normalized intensity distribution of the optical propagating mode for all input combinations at the steady-state of the circuit is illustrated in Figures 20(a-h). At this point, it is important to

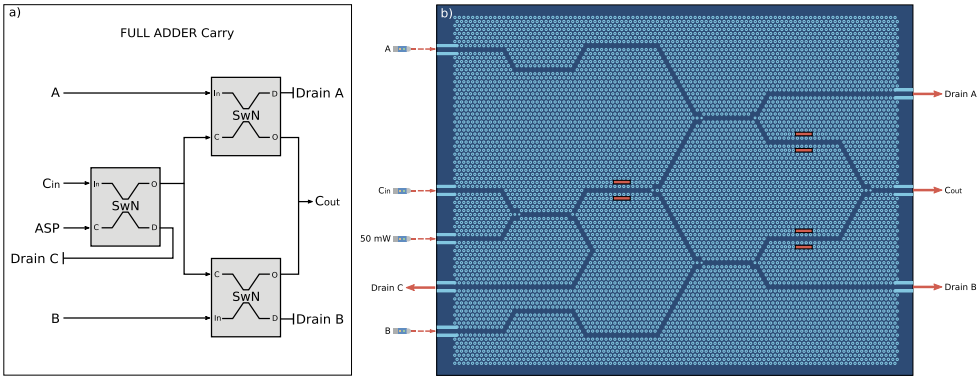
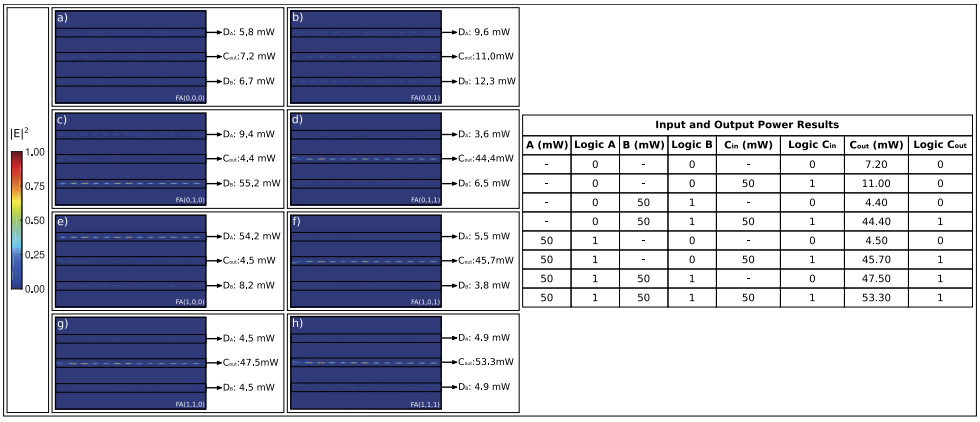


Fig. 19. PhC integrated Full-Adder (FA) Carry circuit. a) Diagram of the FA Carry circuit based on CPCL. b) Simulated structure of the PhC integrated FA Carry circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].



Input and Output Power Results

A (mW)	Logic A	B (mW)	Logic B	C_{in} (mW)	Logic C_{in}	C_{out} (mW)	Logic C_{out}
-	0	-	0	-	0	7.20	0
-	0	-	0	50	1	11.00	0
-	0	50	1	-	0	4.40	0
-	0	50	1	50	1	44.40	1
50	1	-	0	-	0	4.50	0
50	1	-	0	50	1	45.70	1
50	1	50	1	-	0	47.50	1
50	1	50	1	50	1	53.30	1

Fig. 20. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination c) FA(0,0,0), d) FA(0,0,1), e) FA(0,1,0), f) FA(0,1,1), g) FA(1,0,0), h) FA(1,0,1), i) FA(1,1,0), and j) FA(1,1,1). The right-side table summarizes the input and output power results.

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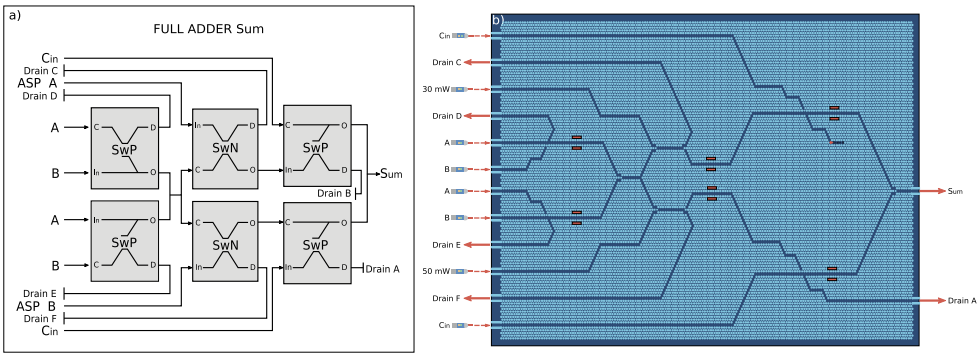


Fig. 21. PhC integrated Full-Adder (FA) Sum circuit. a) Diagram of the FA Sum circuit based on CPCL. b) Simulated structure of the PhC integrated FA Sum circuit. The red rectangles shown in the output branches of the structure represent the nonlinear optimized L3 cavities introduced in the design of the logical switches which interact with the output waveguide, as explained in reference [33].

mention that the PhC Carry circuit achieves its steady-state at 100 ps. Also, power values greater than 44 mW and lower than 12 mW stand for logic 1 and 0, respectively. These values indicate a CR of 5.64 for this circuit. The obtained clock rate for the FA Carry circuit is 10 GHz.

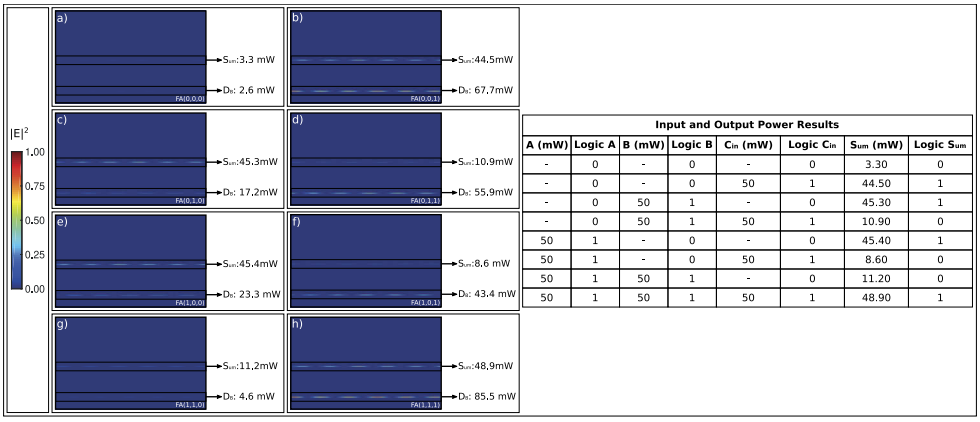
3.8.2. SUM

Here, we detail the PhC Sum circuit for the FA. It consists of three inputs and one output, named S_{um}. By using the CPCL, we can calculate its logic output through the following equation:

$$S_{um} = J(SwP(SwN(ASPA, XOR(A, B)), C_{in}), SwP(C_{in}, SwN(XOR(A, B), ASPB))) \quad (10)$$

where A, B are the two binary digits, and C_{in} is the carry bit. Figure 21(a) represents the CPCL circuit equivalents to the FA Sum circuit.

The simulated structure for the PhC integrated FA Sum circuit, which has a footprint of 74.97 μm × 45.10 μm, is illustrated in Figure 21(b). We set ASP A and B for this circuit with 30 mW



Input and Output Power Results							
A (mW)	Logic A	B (mW)	Logic B	C_{in} (mW)	Logic C_{in}	S_{um} (mW)	Logic S_{um}
-	0	-	0	-	0	3.30	0
-	0	-	0	50	1	44.50	1
-	0	50	1	-	0	45.30	1
-	0	50	1	50	1	10.90	0
50	1	-	0	-	0	45.40	1
50	1	-	0	50	1	8.60	0
50	1	50	1	-	0	11.20	0
50	1	50	1	50	1	48.90	1

Fig. 22. OS normalized intensity distribution of the optical propagating mode at the steady-state for the input combination c) FA(0,0,0), d) FA(0,0,1), e) FA(0,1,0), f) FA(0,1,1), g) FA(1,0,0), h) FA(1,0,1), i) FA(1,1,0), and j) FA(1,1,1). The right-side table summarizes the input and output power results.

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and 50 mW, respectively. So, we can appreciate in Figures 22(a-h) the OS normalized intensity distribution of the optical propagating mode for all input combinations at the steady-state. From this information, we can define power values up to 44 mW and down to 12 mW as the logic 1 and 0, respectively. These values mean a CR of 5.64 dB for this circuit, and a clock rate of 8.3 GHz is also obtained.

4. Discussion

The PhC logic devices have received great attention during the last years due to their relevance for the development of all-optical computational circuits. In this way, different strategies have been successfully applied to design logic gates on PhC platforms, including self-collimation effects, multi-mode interference, waveguide interference paths, ring resonator, four-wave mixing, temporal solitons, and nonlinear effects [17–27,29–32]. However, some limitations that restrict the technological breakthrough have been identified [31]. Following, we review and compare with our proposed devices some relevant works which implement sets of logic gates.

In Ref. [22], it is possible to appreciate all-optical OR, XOR, NOT, XNOR, and NAND logic devices, which are based on the waveguide interference paths approach. The authors reported designs for devices exhibiting a contrast ratio as high as 20 dB under a low power operation regime and a fast response time, lower than 2 ps due to the small footprint area. However, for logic gates up to three inputs, the synchronization and control of the phase difference represent a great challenge. Also, the backpropagation signal to inactive inputs and the unequal threshold values, i.e., the OR and XNOR gates, limit their application to achieve computational circuits. At the same time, the authors proposed the devices under a platform composed of rods of dielectric material in a background medium of air. Unfortunately, these kinds of structures can represent a hard challenge to accomplish their experimental demonstration.

Similarly, in Ref. [26], the authors presented an interesting design for the NOT, AND, OR, XOR, and XNOR logic gates, where the response time is of the order of a few picoseconds (a bit rate of 0.461 Tbit/s) with a low power operation due to their linear regime nature. Nevertheless, the operation of these devices is based on input phase sensitivity, which implies a phase shift to synchronize input signals, increasing the device size. In addition, the power values representing logic 1 and 0 swap for some devices. Indeed, we can observe that Output Logic 0 for their NOT gate is approximately Output Logic 1 for the OR, XOR, XNOR gates. This fact also reflects on a high variance of the device's contrast ratios. These drawbacks limit their adjacent connection to design circuits and systems.

In Ref. [29] the authors demonstrated, through topological photonic crystal cavities, the OR, AND, NOT, NOR, XOR, XNOR, and NAND logic gates. They remark that the structure designs use a linear interference approach, working with low operating power and demonstrating excellent performance even when a significant amount of disorder exists. In spite of these advantages, the issues with these PhC structures include their input phase dependence and the large footprint area of the PhC structures (up to 100 μm $\times$ 45 μm), which lead to a low clock rate.

Interesting and working designs for easily scalable all-optical NOT, AND and NAND logic gates using bandgap solitons in coupled PhC waveguides are reported in Ref. [32]. The authors reported that the logic gates topologies operate with temporal bandgap solitons having stable pulse envelopes during signal processing in the different coupled PhC waveguides. In addition, the building blocks can be cascaded using the output signal from one stage as a new input signal for the subsequent stage aiming at either different logic operators or multiple input logic gate architectures. Equally important, another advantage of this strategy is the absence of intermediate signal amplification between different coupled PhC waveguides stages or even different logic gates due to the soliton nature of the signal pulses. As an example the authors presented the NAND gate built by connecting the proposed AND and NOT gates. Nevertheless, high input power is required, increasing the energy consumption of the devices since additional source

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signals are necessary. For instance, three signal pulses were applied to achieve the single NOT gate. Also, the coupling between the PhC waveguides realized along the propagation direction within the device could lead to undesired interference effects when disorders or fluctuations are introduced at the holes close to the waveguides. Although authors accomplished a NAND gate by cascading the AND and NOT gates, it still lacks the design of advanced circuits such as the XOR, Half-Adder, or Full-Adder. In addition, it was proposed a bridge section in order to cascade the logic gates. Its design appears to be challenging to achieve for different circuits and could increase the footprint of the devices, decreasing the desired performance. On the other hand, the simulated refractive index used in the PhC structure could be hard to achieve experimentally since it does not correspond to the commonly used materials in Silicon Photonics.

In this work, we presented a complete set of PhC integrated logic gates and circuits with three Levels of Logic Processing (LLP). In this context, we refer to three LLP circuits consisting of three switches connected in a series arrangement, for instance, the FULL-ADDER Sum. On the other hand, the AND, NAND, NOR and FA-Carry are two LLP circuits, while the OR, XOR,

Table 1. Information parameters such as response time, input and output power values, and contrast ratio of PhC works in the literature within the domain of logic devices and circuits.

Ref.	Logic Gates	CR (dB)	Response Time (ps)	Output Logic 0 (mW)	Output Logic 1 (mW)
[22]	OR	-	≈2	-	$\geq 0.45P_0$
	XOR	≈20		$\leq 0.0067P_0$	$\geq 0.75P_0$
	NOT	≈20		$\leq 0.0067P_0$	$\geq 0.75P_0$
	XNOR	≈22		$\leq 0.0061P_0$	$\geq 0.85P_0$
	NAND	≈20		$\leq 0.0065P_0$	$\geq 0.75P_0$
[26]	NOT	3.74	≈2.168	$\leq 0.772P_0$	$\geq 1.326P_0$
	AND	11.47		$\leq 0.131P_0$	$\geq 1.717P_0$
	OR	12.48		$\leq 0.051P_0$	$\geq 0.717P_0$
	XOR	6.50		$\leq 0.133P_0$	$\geq 0.574P_0$
	XNOR	6.50		$\leq 0.133P_0$	$\geq 0.574P_0$
[29]	OR	54.4	-	0	$(\sqrt{2}Ee^{-i\pi/2})/2$
	AND	9.54		$(\sqrt{2}Ee^{-i\pi/2})/8$	$(3\sqrt{2}Ee^{-i\pi/2})/8$
	NOT	54.4		0	$\sqrt{2}E/2$
	NOR	9.54		$(Ee^{-i\pi/2})/4$	$(3Ee^{-i\pi/2})/4$
	XOR	54.4		0	$\sqrt{2}E/2$
	XNOR	32.6		0	$(Ee^{-i\pi/2})/2$
	NAND	31.1		0	$(Ee^{i\pi/2})/2$
[32]	NOT AND NAND	20	15.43	-	0.52A
This work	AND	6.19	80	≤12	≥50
	OR	8.65		≤6	≥44
	NAND	5.74		≤12	≥45
	NOR	5.92		≤12	≥47
	XOR	11.56	120	≤3	≥43
	FANOUT	8.36		≤7	≥48
	HA	5.54		≤12	≥43
	FA	5.64		≤12	≥44

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FAN-OUT and HALF-ADDER are one LLP. The results of our circuits have shown a CR higher than 5.50 dB, with average of 7.02 dB and confidence interval (CI) from 5.42 dB to 8.61 dB at 95% of confidence level. It demonstrates the small fluctuations of the output, and robustness of our proposed devices. These circuits also exihibit well-defined input and output power values to represent the 1 and 0 logic states, operating at the same input and output wavelength ($\lambda \approx 1550$ nm). In addition, our integrated circuits are based in the same building block devices without amplification signals between their connections (switches N and P) and have great potential for fabrication since the newest technologies for manufacturing PhC devices allow to obtain devices with an error rate below 5%, with a high rate of repeatability, and at a low production cost [34–38]. We also applied our previously proposed methodology to evaluate the effect of structural disorders on our PhC integrated circuits. Fundamentally, it consists of introducing fluctuations in specific regions in the boundary of the PhC waveguides that form the logic gate structure [25]. The results showed that our circuits can support small phase delay ($\lambda/28$) at the input sources, changes in the input power levels (±5 mW), and hole disorder effects around the cavity (±20 nm), the most sensitive region. These fluctuations result in about ±5 mW signal noise at the output for these devices. Table 1 summarizes the advantages of the devices proposed in this paper in comparison with other previously published works.

As a final consideration, we call attention to the development of a PhC cross information device that can help build improved circuits with a smaller footprint area, faster response time, and lower energy consumption. Furthermore, we expect to address a CPCL mathematical model allowing us to enhance the device design process, switching up to a high abstraction level rather than performing large FDTD simulations.

5. Conclusion

In this paper, we numerically demonstrated a complete set of PhC integrated circuits with up to two logic processing levels, based on Complementary Photonic Crystal components, including AND, OR, NOR, NAND, XOR, FAN OUT, HALF ADDER, and FULL ADDER logic devices. The proposed systems showed excellent performance for SwN and SwP acting as core hardware devices, where a contrast ratio as high as 5.5 dB was demonstrated. Furthermore, our designs were computationally guided to establish values that reliably represent logic states 1 and 0, guaranteeing an operating wavelength at $\lambda \approx 1550$ nm for input and output. Last but not least, it is imperative to emphasize that this study also contributes satisfactorily to address improvements for the current telecommunication systems, sensors, and microprocessors chips.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. H. N. Khan, D. A. Hounshell, and E. R. Fuchs, "Science and research policy at the end of moore's law," Nat. Electron. **1**(1), 14–21 (2018).
2. M. Romagnoli, V. Sorianello, M. Midrio, F. H. Koppens, C. Huyghebaert, D. Neumaier, P. Galli, W. Templ, A. D'Errico, and A. C. Ferrari, "Graphene-based integrated photonics for next-generation datacom and telecom," Nat. Rev. Mater. **3**(10), 392–414 (2018).
3. Q. Shi, B. Dong, T. He, Z. Sun, J. Zhu, Z. Zhang, and C. Lee, "Progress in wearable electronics/photonics–moving toward the era of artificial intelligence and internet of things," InfoMat **2**, 1131–1162 (2020).
4. C. E. Leiserson, N. C. Thompson, J. S. Emer, B. C. Kuszmaul, B. W. Lampson, D. Sanchez, and T. B. Schardl, "There's plenty of room at the top: What will drive computer performance after moore's law?" Science **368**(6495), eaam9744 (2020).
5. B. J. Shastri, A. N. Tait, T. F. de Lima, W. H. Pernice, H. Bhaskaran, C. D. Wright, and P. R. Prucnal, "Photonics for artificial intelligence and neuromorphic computing," Nat. Photonics **15**(2), 102–114 (2021).

Optics EXPRESS

6. P. Ye, T. Ernst, and M. V. Khare, "The last silicon transistor: Nanosheet devices could be the final evolutionary step for moore's law," IEEE Spectrum **56**(8), 30–35 (2019).
7. P. Minzioni, C. Lacava, T. Tanabe, J. Dong, X. Hu, G. Csaba, W. Porod, G. Singh, A. E. Willner, A. Almaiman, V. Torres-Company, J. Schröder, A. C. Peacock, M. J. Strain, F. Parmigiani, G. Contestabile, D. Marpaung, Z. Liu, J. E. Bowers, L. Chang, S. Fabbri, M. R. Vázquez, V. Bharadwaj, S. M. Eaton, P. Lodahl, X. Zhang, B. J. Eggleton, W. J. Munro, K. Nemoto, O. Morin, J. Laurat, and J. Nunn, "Roadmap on all-optical processing," J. Opt. **21**(6), 063001 (2019).
8. E. Yablonovitch, "Inhibited spontaneous emission in solid-state physics and electronics," Phys. Rev. Lett. **58**(20), 2059–2062 (1987).
9. S. John, "Strong localization of photons in certain disordered dielectric superlattices," Phys. Rev. Lett. **58**(23), 2486–2489 (1987).
10. E. Yablonovitch, T. Gmitter, and K.-M. Leung, "Photonic band structure: The face-centered-cubic case employing nonspherical atoms," Phys. Rev. Lett. **67**(17), 2295–2298 (1991).
11. T. F. Krauss, M. Richard, and S. Brand, "Two-dimensional photonic-bandgap structures operating at near-infrared wavelengths," Nature **383**(6602), 699–702 (1996).
12. S. E. Baker, M. D. Pocha, A. S. Chang, D. J. Sirbuly, S. Cabrini, S. D. Dhuey, T. C. Bond, and S. E. Létant, "Detection of bio-organism simulants using random binding on a defect-free photonic crystal," Appl. Phys. Lett. **97**(11), 113701 (2010).
13. D. Englund, A. Majumdar, A. Faraon, M. Toishi, N. Stoltz, P. Petroff, and J. Vučković, "Resonant excitation of a quantum dot strongly coupled to a photonic crystal nanocavity," Phys. Rev. Lett. **104**(7), 073904 (2010).
14. J. Knight, T. Birks, P. S. J. Russell, and D. Atkin, "All-silica single-mode optical fiber with photonic crystal cladding," Opt. Lett. **21**(19), 1547–1549 (1996).
15. N. Skivesen, A. Têtu, M. Kristensen, J. Kjems, L. H. Frandsen, and P. I. Borel, "Photonic-crystal waveguide biosensor," Opt. Express **15**(6), 3169–3176 (2007).
16. M. Notomi, K. Yamada, A. Shinya, J. Takahashi, C. Takahashi, and I. Yokohama, "Extremely large group-velocity dispersion of line-defect waveguides in photonic crystal slabs," Phys. Rev. Lett. **87**(25), 253902 (2001).
17. M. F. Yanik, S. Fan, M. Soljačić, and J. D. Joannopoulos, "All-optical transistor action with bistable switching in a photonic crystal cross-waveguide geometry," Opt. Lett. **28**(24), 2506–2508 (2003).
18. Y. Zhang, Y. Zhang, and B. Li, "Optical switches and logic gates based on self-collimated beams in two-dimensional photonic crystals," Opt. Express **15**(15), 9287–9292 (2007).
19. P. Andalib and N. Granpayeh, "All-optical ultracompact photonic crystal and gate based on nonlinear ring resonators," J. Opt. Soc. Am. B **26**(1), 10–16 (2009).
20. C. Husko, T. Vo, B. Corcoran, J. Li, T. F. Krauss, and B. J. Eggleton, "Ultracompact all-optical xor logic gate in a slow-light silicon photonic crystal waveguide," Opt. Express **19**(21), 20681–20690 (2011).
21. W. Liu, D. Yang, G. Shen, H. Tian, and Y. Ji, "Design of ultra compact all-optical xor, xnor, nand and or gates using photonic crystal multi-mode interference waveguides," Opt. Laser Technol. **50**, 55–64 (2013).
22. Y. Fu, X. Hu, and Q. Gong, "Silicon photonic crystal all-optical logic gates," Phys. Lett. A **377**(3-4), 329–333 (2013).
23. L. P. Caballero, J. Vasco, P. Guimaraes, and O. P. Vilela Neto, "All-optical majority and feynman gates in photonic crystals," in *2015 30th Symposium on Microelectronics Technology and Devices (SBMicro)*, (IEEE, 2015), pp. 1–4.
24. N. M. D'souza and V. Mathew, "Interference based square lattice photonic crystal logic gates working with different wavelengths," Opt. Laser Technol. **80**, 214–219 (2016).
25. L. E. P. Caballero, J. P. V. Cano, P. S. Guimarães, and O. P. Vilela Neto, "Effect of structural disorder on photonic crystal logic gates," IEEE Photonics J. **9**(5), 1–15 (2017).
26. P. Rani, S. Fatima, Y. Kalra, and R. Sinha, "Realization of all optical logic gates using universal nand gates on photonic crystal platform," Superlattices Microstruct. **109**, 619–625 (2017).
27. H. M. Hussein, T. A. Ali, and N. H. Rafat, "New designs of a complete set of photonic crystals logic gates," Opt. Commun. **411**, 175–181 (2018).
28. V. Jandieri, R. Khomeriki, and D. Erni, "Realization of true all-optical and logic gate based on nonlinear coupled air-hole type photonic crystal waveguides," Opt. Express **26**(16), 19845–19853 (2018).
29. L. He, W. Zhang, and X. Zhang, "Topological all-optical logic gates based on two-dimensional photonic crystals," Opt. Express **27**(18), 25841–25859 (2019).
30. V. Jandieri, R. Khomeriki, J. Berakdar, and D. Erni, "Theory of soliton propagation in nonlinear photonic crystal waveguides," Opt. Express **27**(21), 29558–29566 (2019).
31. L. E. P. Caballero and O. P. Vilela Neto, "A review on photonic crystal logic gates," J. Integr. Circuits Syst. **16**(1), 1–13 (2021).
32. V. Jandieri, R. Khomeriki, T. Onoprishvili, D. H. Werner, J. Berakdar, and D. Erni, "Functional all-optical logic gates for true time-domain signal processing in nonlinear photonic crystal waveguides," Opt. Express **28**(12), 18317–18331 (2020).
33. L. P. Caballero, M. L. Povinelli, J. C. Ramirez, P. S. Guimarães, and O. P. Vilela Neto, "Complementary photonic crystal integrated logic devices," Opt. Lett. **45**(19), 5502–5505 (2020).
34. R. Wilson, T. J. Karle, I. Moerman, and T. F. Krauss, "Efficient photonic crystal y-junctions," J. Opt. A: Pure Appl. Opt. **5**(4), S76–S80 (2003).

Optics EXPRESS

35. T. Stomeo, M. Grande, A. Qualtieri, A. Passaseo, A. Salhi, M. De Vittorio, D. Biallo, A. D'orazio, M. De Sario, V. Marrocco, V. Petruzzelli, and F. Prudenzano, "Fabrication of force sensors based on two-dimensional photonic crystal technology," Microelectron. Eng. **84**(5-8), 1450–1453 (2007).
36. A. Baron, A. Ryasnyanskiy, N. Dubreuil, P. Delaye, Q. V. Tran, S. Combrié, A. de Rossi, R. Frey, and G. Roosen, "Light localization induced enhancement of third order nonlinearities in a gaas photonic crystal waveguide," Opt. Express **17**(2), 552–557 (2009).
37. X. Zhang, K. Takeuchi, X. Cong, Y. Xiong, M. Morifuji, A. Maruta, H. Kajii, and M. Kondow, "Dry etching of deep air holes in gaas/algaas-based epi-wafer having inas quantum dots for fabrication of photonic crystal laser," Jpn. J. Appl. Phys. **56**(12), 126501 (2017).
38. T. Yamaguchi, Y. Ota, R. Katsumi, K. Watanabe, S. Ishida, A. Osada, Y. Arakawa, and S. Iwamoto, "Gaas valley photonic crystal waveguide with light-emitting inas quantum dots," Appl. Phys. Express **12**(6), 062005 (2019).