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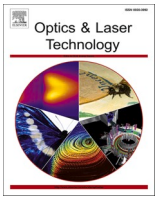

Full length article

Simple and reconfigurable all-optical logic gate

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A B S T R A C T

A photonics-based digital signal processing structure that has the ability to realise all the six basic logical operations, namely XOR, OR, AND, XNOR, NOR and NAND, is presented. It is based on applying the two digital inputs into a dual-polarisation modulator and adjusting the angle of a waveplate connected to the modulator output to realise different logical operations. The proposed dual-polarisation modulator based optical logic gate has a simple and compact structure and robust performance. Switching between different logical operations can be realised in high speed by adjusting only one system parameter, with no change in the system physical configuration. The proposed dual-polarisation modulator based optical logic gate is theoretically analysed. Using the system parameter setting obtained from the theoretical analysis, the six basic logical operations are experimentally demonstrated. To our knowledge, this is the first report of an optical logic gate that is capable of switching between all the six basic logical operations by adjusting only one system parameter.

1. Introduction

All-optical logic gates are attractive as they can overcome the speed limitation of their electronic counterparts. XOR, OR, AND, XNOR, NOR and NAND gates are the six basic logic gates. They are the fundamental components in future all-optical computers and high-capacity telecommunication networks. Nonlinear effects in devices such as semiconductor optical amplifiers (SOAs) [1–4], highly nonlinear fibres (HNLFs) [5–7] and periodically poled lithium niobate (PPLN) waveguides [8–10] have been employed to implement logical operations in the optical domain. An SOA generates amplified spontaneous emission (ASE) noise, a HLNF is bulky and a PPLN waveguide requires precise temperature control. Furthermore, optical logic gates implemented by these devices have complex structures, high cost, high power consumption or limited reconfigurability. Logic gates implemented using non-volatile hybrid electro-optic plasmonic switches [11], Y-shaped waveguides of 2-D photonic crystal [12] and a plasmonic-based Y-shaped power combiner [13,14] have also been proposed but without experimental verification. Recently there are reports on controlling the digital input amplitudes and the optical modulator bias voltages to realise various logical operations [15,16]. This technique has a simple structure and does not generate additional noise components. However, the logical operation is incorporated into the modulation process. This limits its practical use and makes it difficult to realise multiple logical operations. Furthermore, to our knowledge, all the reported optical logic gates, e.g. [1–10,15–19], require adjustment of several system parameters in order to switch between different logical operations.

In this paper, we propose, simulate and experimentally demonstrate a novel photonic signal processing structure that can realise all the six basic logical operations. It is based on a dual-polarisation modulator followed by waveplates and a polariser. Switching between different logical operations can be achieved by simply adjusting one system parameter, which is the angle of a half waveplate. The proposed optical logic gate offers a number of advantages including compactness, low cost, low power consumption, high speed reconfigurability and robust performance. Simulation and experimental results are presented that demonstrate the proposed all-optical and reconfigurable logic gate. The results show the system parameter settings required to obtain different logical operations are in excellent agreement with theory.

2. Topology and operation principle

Fig. 1 shows the proposed photonics-based digital signal processing structure for realising different logical operations. A laser source generates a continuous wave (CW) light, which travels in the slow axis of a fibre before launching into a dual-polarisation modulator. The dual-polarisation modulator consists of a 3-dB coupler, two phase modulators (PM_1 and PM_2), a 90° polarisation rotator (PR) and a polarisation beam combiner (PBC). The light launched into the dual-polarisation modulator is equally split into two portions via the 3-dB coupler. Each portion of the light is phase modulated by the digital input ($Data_1(t)$ and $Data_2(t)$) in the phase modulator (PM_1 and PM_2) inside the dual-polarisation modulator. As shown in Fig. 1, a 90° PR is connected to the output of PM_1. It rotates the polarisation state of the optical signal at

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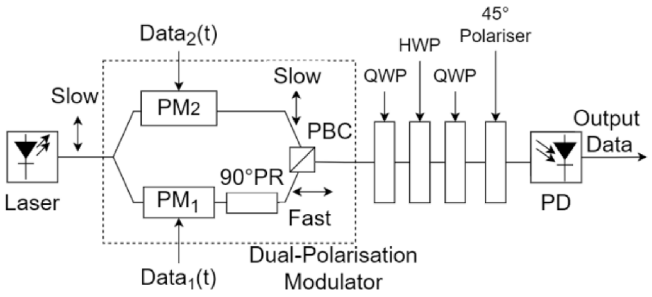

Fig. 1. Topology of the proposed reconfigurable optical logic gate. ↕ and ↔ represent the polarisation state of the light aligned to the slow and fast axis of a fibre respectively.

PM_1 output by 90°. The optical signals travelled in the two arms of the dual-polarisation modulator are combined by a PBC. The Jones vector representation [20] of the dual-polarisation modulator output electric field is given by

$$E_{DPolM}(t) = \begin{bmatrix} E_1(t) \\ E_2(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{\sqrt{2}} E_{in}\sqrt{t_{ff}}\, e^{j\omega_c t} e^{j\left(\frac{Data_1(t)\pi}{V_\pi}\right)} \\ \frac{1}{\sqrt{2}} E_{in}\sqrt{t_{ff}}\, e^{j\omega_c t} e^{j\left(\frac{Data_2(t)\pi}{V_\pi}\right)} \end{bmatrix} \quad (1)$$

where $E_1(t)$ and $E_2(t)$ are the electric fields of the optical signals travelled in the fast and slow axis respectively, E_{in} and ω_c are the electric field amplitude and the angular frequency of the CW light into the dual-polarisation modulator respectively, t_{ff} is the insertion loss of the dual-polarisation modulator and V_π is the PM switching voltage. A quarter waveplate (QWP), a half waveplate (HWP) and a QWP are connected to the dual-polarisation modulator output. By setting the two QWPs at 45° angle, the Jones matrix of the three waveplates can be written as [21]

$$J_{Waveplates}(\theta) = \begin{bmatrix} je^{j2\theta} & 0 \\ 0 & -je^{-j2\theta} \end{bmatrix} \quad (2)$$

where θ is the HWP angle. The electric fields of the two orthogonally polarised optical signals after passing through the three waveplates are given by

$$E_{Waveplates}(t) = \begin{bmatrix} \frac{1}{\sqrt{2}} E_{in}\sqrt{t_{ff}}\, e^{j\omega_c t} je^{j\left(\frac{Data_1(t)\pi}{V_\pi}+2\theta\right)} \\ -\frac{1}{\sqrt{2}} E_{in}\sqrt{t_{ff}}\, e^{j\omega_c t} je^{j\left(\frac{Data_2(t)\pi}{V_\pi}-2\theta\right)} \end{bmatrix} \quad (3)$$

This shows, rather than altering the light polarisation state, the function of the three waveplates is to introduce a phase shift of $\pm 2\theta$ to the two orthogonal polarisation signals. A polariser at an angle of 45° to the slow axis is connected to the output of the three waveplates. It aligns the two orthogonally polarised optical signals into a single polarisation state [22]. Hence the electric field at the output of the polariser is given by

$$E_{Polariser}(t) = \frac{1}{2\sqrt{2}} E_{in}\sqrt{t_{ff}}\, e^{j\omega_c t}\left[je^{j\left(\frac{Data_1(t)\pi}{V_\pi}+2\theta\right)} - je^{j\left(\frac{Data_2(t)\pi}{V_\pi}-2\theta\right)} \right] \quad (4)$$

The optical signal at the output of the polariser is detected by a photodetector (PD). The PD generates a photocurrent, which is the product of the PD responsivity $\Re$ and the absolute square of the electric field into the PD [23], and is given by

$$I_{out}(t) = \frac{\Re P_{in} t_{ff}}{8}\left[2 - 2\cos\left(\frac{\pi}{V_\pi}\left(Data_1(t) - Data_2(t)\right) + 4\theta \right) \right] \quad (5)$$

where P_{in} is the power of the CW light into the dual-polarisation modulator.

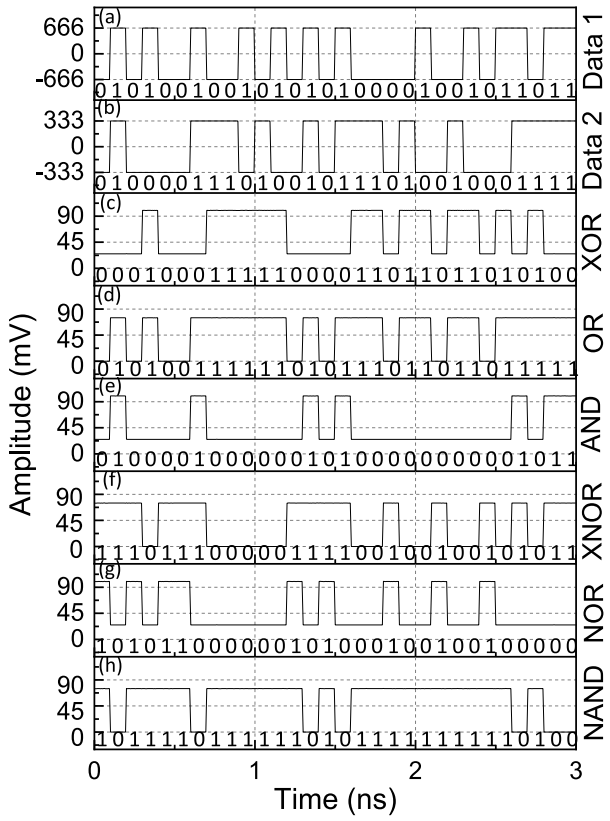

Fig. 2. Two input data streams ((a) and (b)), and the system output waveform for the HWP angle of (c) 0°, (d) 15°, (e) 30°, (f) 45°, (g) 60° and (h) 75°.

Table 1
Settings of the HWP angle required to obtain different system output photocurrent amplitudes for realising different logical operations.

Logic Gate	Input Bit Combination	Output Bit	HWP Angle θ	Resultant Photocurrent Amplitude
XOR	00, 11	0	0°	$\Re P_{in} t_{ff}/8$
	01, 10	1		$\Re P_{in} t_{ff}/2$
OR	00	0	15°	0
	01, 10, 11	1		$3\Re P_{in} t_{ff}/8$
AND	00, 01, 10	0	30°	$\Re P_{in} t_{ff}/8$
	11	1		$\Re P_{in} t_{ff}/2$
XNOR	01, 10	0	45°	0
	00, 11	1		$3\Re P_{in} t_{ff}/8$
NOR	01, 10, 11	0	60°	$\Re P_{in} t_{ff}/8$
	00	1		$\Re P_{in} t_{ff}/2$
NAND	11	0	75°	0
	00, 01, 10	1		$3\Re P_{in} t_{ff}/8$

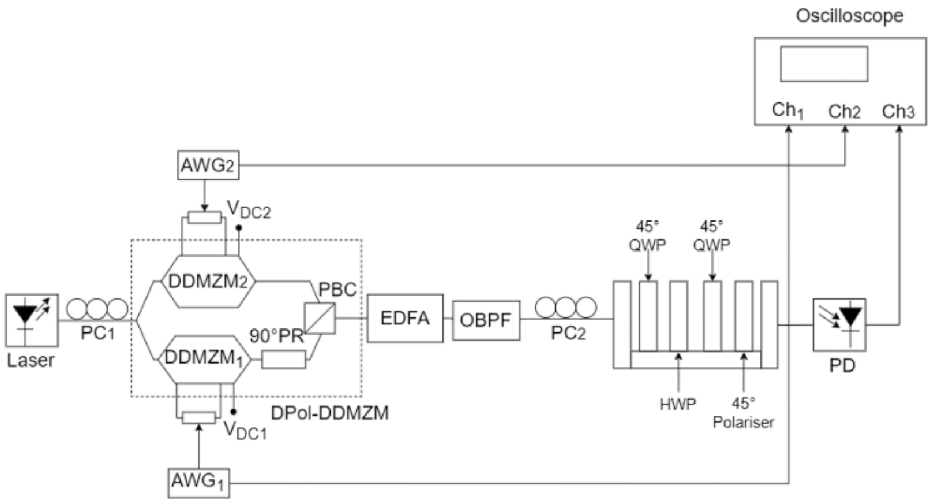

Fig. 3. Experimental setup of the proposed reconfigurable optical logic gate.

The two digital input amplitudes (D_1 and D_2) are designed to be

$$D_1 = \begin{cases} -2V_\pi/3 & for\ ''0''\ bit \\ 2V_\pi/3 & for\ ''1''\ bit \end{cases} \tag{6}$$

$$D_2 = \begin{cases} -V_\pi/3 & for\ ''0''\ bit \\ V_\pi/3 & for\ ''1''\ bit \end{cases} \tag{7}$$

In this case, the HWP angle θ can be adjusted to obtain different photocurrent amplitudes that represent logic "0" and logic "1" for different logical operations. For example, for an XOR gate, an input bit combination of "00" or "11" results in logic "0", and an input bit combination of "01" or "10" results in logic "1". In order to obtain an XOR logical operation, the HWP angle is designed to be 0°. According to (5)-(7), the resultant output photocurrent amplitude from the PD is $\Re P_{in} t_{ff}/8$ for an input bit combination of "00" or "11", and the resultant output photocurrent amplitude is $\Re P_{in} t_{ff}/2$ for an input bit combination of "01" or "10". This shows the realisation of an XOR logical operation as the photocurrent amplitude of $\Re P_{in} t_{ff}/8$ is less than $\Re P_{in} t_{ff}/2$, which can be used to represent logic "0" and logic "1" respectively. Table 1 summarises the input bit combinations and the corresponding output bits for different logic gates together with the settings of the HWP angle required to obtain different system output photocurrent amplitudes. The table shows the proposed structure can realise all the six basic logical operations by simply controlling the HWP angle.

3. Simulation results and discussion

The dual-polarisation modulator based optical logic gate shown in Fig. 1 was set up using a photonic simulation software. The laser source was a laser diode, which generated a CW light with a frequency of 193.1 THz and a power of 100 mW. The polarisation state of the light was adjusted to ensure the light travels in the slow axis before launching into a dual-polarisation modulator. Two independent 10 Gbit/s pseudo-random binary sequence (PRBS) non-return to zero (NRZ) data streams (Data 1 and Data 2) as shown in Fig. 2(a) and (b) were applied to the two PMs with a switching voltage of 1 V inside the dual-polarisation modulator. Data 1 and Data 2 amplitudes were designed according to (6) and (7) and they are 0.67 V and 0.33 V as shown in Fig. 2. The output of the dual-polarisation modulator was connected to a 45° angle QWP, a HWP and another 45° angle QWP. This was followed by a polariser with a 45° angle away from the slow axis. Fig. 2(c)-(h) show the system output waveforms for every 15° change in the HWP angle from 0° to 75°. The corresponding bit patterns of the two input data streams and the system output waveforms are also shown in Fig. 2. Based on the input and output bit patterns, the simulation results show the proposed structure can realise all the six basic logical operations. The results also show the settings of the HWP angle required to obtain different logical operations agree with theory.

Compared to the reported optical logic gates implemented using SOAs, HNLFs or PPLN waveguides, the dual-polarisation modulator based optical logic gate has the advantages of a simple, compact and cost-effective structure, low power consumption, and robust and low noise performance. This is because the proposed logic gate only involves a dual-polarisation modulator, three waveplates and a polariser. The modulator and the waveplates can be integrated on a lithium niobate substrate and packaged with a polariser to form a compact device. Furthermore, these components are commercially available and hence the proposed structure is low cost. On the other hand, the logic gates based on SOAs require a number of components and the optical logic gates based on a HNLF is bulky. Unlike the logic gates based on SOAs or a PPLN waveguide, the dual-polarisation modulator based optical logic gate does not require thermal control. Hence it has low power consumption and robust performance. The system bit rate is only limited by the modulator and PD bandwidth, which can be made very large. Hence the dual-polarisation modulator based optical logic gate can realise different logical operations at a bit rate of tens of gigabits per second. Compared to the reported optical modulator based logic gates [15,16], which require using different digital input amplitudes and controlling the modulator bias voltages to realise different logical operations, the proposed dual-polarisation modulator based optical logic gate has a number of advantages. First, no modulator bias control is needed. Second, change in the input data amplitudes is not required when switching from one logical operation to another. The HWP angle is the only system parameter needs to be controlled when switching between all the six basic logical operations. Third, in the proposed structure, the logical operation is implemented outside the dual-polarisation modulator, via controlling the HWP angle. Hence multiple different logical operations can be realised simultaneously by using a single integrated optical modulator. This is different from the optical logic gates presented in [15] and [16] where the logical operation is implemented together with the modulation process at the optical modulator, via controlling the input data amplitudes and the modulator bias voltages. Hence, in this case, a single integrated optical modulator can only realise a single logical operation at a time. Furthermore, separating the logical operation from the modulation process is desirable for an optical logical gate to be used in practice and to be used as a building block to realise complex logical operations. Note that the waveplates used in the dual-polarisation modulator based optical logic gate can be integrated on a lithium niobate ($LiNbO_3$) substrate. The angle of the waveplate can be

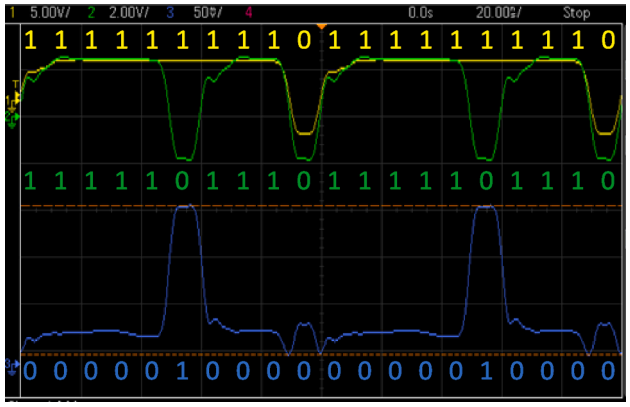

Fig. 4. Input data stream 1 (yellow line, 5 V/div, 20 ns/div), input data stream 2 (green line, 2 V/div), and the system output waveform (blue line, 50 mV/div), when the HWP angle is at 0°.

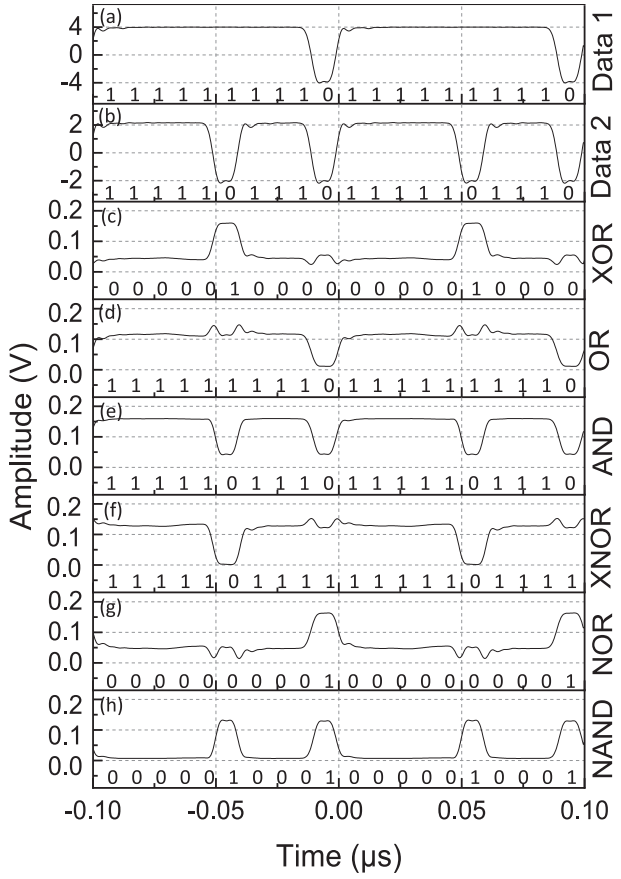

Fig. 5. Two data streams into the RF ports of the DDMZMs ((a) and (b)), and the system output waveform showing (c) XOR, (d) OR, (e) AND, (f) XNOR, (g) NOR and (h) NAND logical operations.

rotated to the desired value by applying a voltage to the electrode on the $LiNbO_3$ waveguide. Lithium niobate electro-optic waveplates with gigahertz rotation speed have been reported [24]. Hence very fast switching between different logical operations can be realised. Since $LiNbO_3$ is widely used as a substrate material in commercial integrated optical devices, the proposed optical logic gate can be made cost effectively.

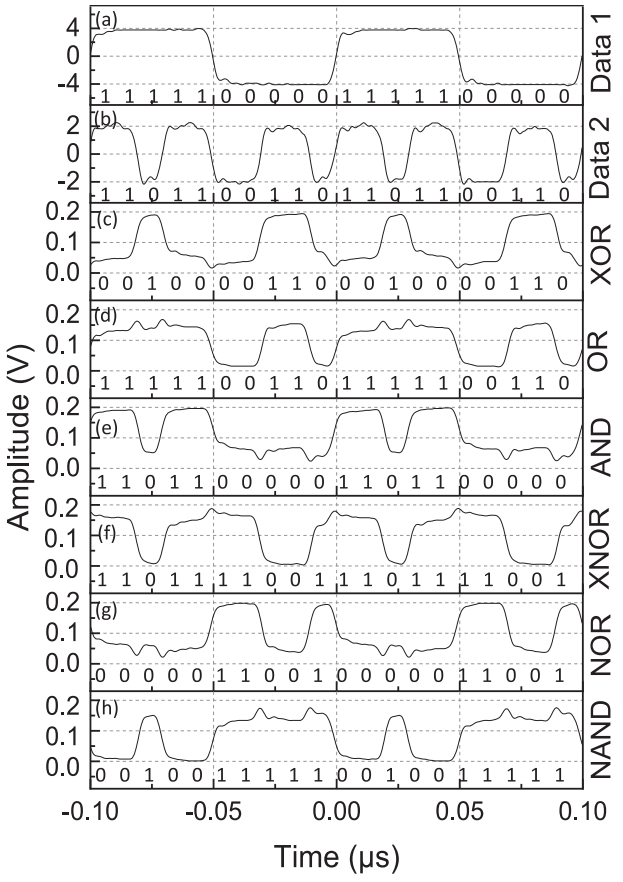

Fig. 6. Two input data streams ((a) and (b)), and the system output waveform ((c)-(h)) obtained using different HWP angle settings.

4. Experimental results

An experiment was set up as shown in Fig. 3 to verify the concept of the proposed dual-polarisation modulator based optical logic gate. The laser source was a tunable laser (Santec WSL-100). It generated a 1550 nm 10 dBm CW light. The light passed through a polarisation controller (PC_1), which was adjusted to ensure the polarisation state of the light was aligned to the slow axis before launching into an optical modulator. The optical modulator used in the experiment was a dual-polarisation dual-drive Mach-Zehnder modulator (DPol-DDMZM) (Fujitsu FTM7980EDA). The DPol-DDMZM consists of the same components as the dual-polarisation modulator shown in Fig. 1 except the two PMs are replaced by two DDMZMs. It has been demonstrated in [25] that a DDMZM behaves as a PM when the DDMZM is driven by two identical signals and is biased at the peak point. Therefore the dual-polarisation modulator shown in Fig. 1 can be implemented by simply connecting the outputs of a power divider to the two input RF ports of a DDMZM inside the DPol-DDMZM. The DPol-DDMZM had 7 dB insertion loss and 3.1 V RF port switching voltage. Two 100 Mbit/s data streams, which were generated by two dual-output arbitrary waveform generators (AWG_1 and AWG_2), were separately injected into the two DDMZMs via two power dividers (Minicircuits ZFSC-2–1-S+) as shown in Fig. 3. One of the two dual-output $AWG_{1(2)}$ outputs was connected to Channel 1(2) (Ch1 and Ch2) of a 100 MHz bandwidth oscilloscope (Keysight DSOX2014A) to view the input data streams. A dual-output DC power supply generated two DC voltages (V_{DC1} and V_{DC2}), which were used to bias the two DDMZMs at the peak point. The output of the DPol-DDMZM was connected to an erbium-doped fibre amplifier (EDFA) followed by a 0.5 nm 3-dB bandwidth optical bandpass filter (OBPF) to compensate for the system loss and to suppress the ASE noise respectively. A PC (PC_2)

Table 2
Performance comparison of the proposed and reported reconfigurable optical logic gates. FWM: four wave mixing, XGM: cross gain modulation, XPM: cross phase modulation, SFG: sum frequency generation, and DFG: difference frequency generation.

	Technique	Number of logical operations	System complexity	Number of parameters need to be controlled	Switching speed
[1]	FWM in SOA	6	Moderate	2	Moderate
[6]	XPM in HNLF	3	Moderate	2	Low
[8]	SFG and DFG in PPLN	3	High	3	Low
[15]	Modulator bias control	6	Low	5	Moderate
[16]	Modulator bias control	6	Low	4	Moderate
[17]	FWM and XGM in SOA	4	Moderate	2	Low
[18]	XPM in SOA	4	High	5	Low
[19]	XGM in SOA	3	High	3	Low
This paper	Optical signal phase control	6	Low	1	High

was connected to the OBPF output. It was adjusted to ensure the two orthogonally polarised optical signals from $DDMZM_1$ and $DDMZM_2$ were aligned to the fast and slow axis respectively before launching into a FiberBench PC kit (Thorlabs PC-FFB-1550), which was formed by a rotatable HWP sandwiched between two rotatable QWPs mounted between two fibre ports on a fibre bench. A rotating linear polariser module (Thorlabs FBR-LPNIR) was inserted after the second QWP in the FiberBench PC kit. The angles of the two QWPs and the linear polariser were fixed at 45°. The output optical signal was detected by a PD (Discovery Semiconductors DSC30S) whose output was connected to Ch3 of the oscilloscope to view the system output waveform.

Fig. 4 shows a screenshot of an oscilloscope display containing the two input data streams and the system output waveform when the HWP angle was set at 0°. As shown, the two input sequences are "11111111101111111110" and "11111011101111101110", and the corresponding output sequence is "00000100000000010000", which verifies the "XOR" logical operation. The two data streams into the RF ports of the DDMZMs were recorded and are shown in Fig. 5(a) and (b). As can be seen, the amplitude of Data 1 was designed to be twice the amplitude of Data 2, according to (6) and (7). The HWP angle was adjusted to the values shown in Table 1. The system output waveforms were recorded accordingly and are shown in Fig. 5(c)–(h). The corresponding input and output sequences are labelled in the figures. The experimental results shown in Fig. 5 indicate the settings of the HWP angle required to obtain different logical operations agree with theory. The experiment was repeated using another set of input data streams. Fig. 6(a) and (b) show the two input data streams where Data 1 amplitude is around twice the amplitude of Data 2. The system output waveforms were recorded and are shown in Fig. 6(c)–(h) when the HWP angle was adjusted to the values shown in Table 1. The corresponding input and output sequences are shown in the figure. The experimental results shown in Figs. 5 and 6 demonstrate all the six basic logical operations can be realised by simply controlling the HWP angle, which verifies the reconfigurability of the proposed structure. Only little changes in the system output waveforms were observed for 10 min. The changes were mainly caused by changes in the polarisation state of the two orthogonally polarised optical signals into the FiberBench PC kit, which can be avoided by integrating the optical logic gate on a lithium niobate substrate. Note that the rising/falling edge of the system output waveforms shown in Figs. 5 and 6 has a similar steepness as that of the input data. This indicates that the system does not degrade the data rise/fall time performance.

Table 2 provides a comparison of this work with the reported reconfigurable optical logic gates with experimental verification. As can be seen from the table, the logic gates based on SOAs, HNLFs or PPLN waveguides have moderate to high system complexity as they require a number of components. Also note that majority of them cannot realise all six basic logical operations. The logic gates implemented by controlling the modulator bias voltages have a simple structure but require adjustment of multiple system parameters including the modulator bias voltages and the input data amplitudes in order to switch between different logical operations. The proposed reconfigurable optical logic gate has a simple structure and is capable of realising all six basic logical operations. Only the angle of a HWP needs to be adjusted to switch from one logical operation into another. A HWP with a gigahertz rotation speed can be implemented using the electro-optic technique. Hence switching between different logical operations can be achieved in high speed.

5. Conclusion

In conclusion, a new photonic signal processing structure that can realise all the six basic logical operations has been presented. It is based on a dual-polarisation modulator that is formed by two PMs connected in parallel with a 90° PR at one of the PM outputs. Two orthogonally polarised optical signals carrying the two digital inputs are generated at the modulator output. They pass through a HWP sandwiched between two 45° angle QWPs followed by a 45° angle polariser, before detecting by a PD. Six logical operations can be realised by simply controlling the angle of the HWP. The proposed optical logical gate has a simple structure and robust performance. It can be integrated on a lithium niobate substrate. The dual-polarisation modulator based optical logic gate has been experimentally demonstrated with results in excellent agreement with theory.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

References

[1] Z. Li, G. Li, Ultrahigh-speed reconfigurable logic gates based on four-wave mixing in a semiconductor optical amplifier, IEEE Photon. Technol. Lett. 18 (12) (2006) 1341–1343.
[2] X. Chen, L. Huo, Z. Zhao, L. Zhuang, C. Lou, Reconfigurable all-optical logic gates using single semiconductor optical amplifier at 100-GB/s, IEEE Photon. Technol. Lett. 28 (21) (2016) 2463–2466.
[3] Z. Li, Y. Liu, S. Zhang, H. Ju, H. de Waardt, G.D. Khoe, H.J.S. Dorren, D. Lenstra, All-optical logic gates using semiconductor optical amplifier assisted by optical filter, Electron. Lett 41 (25) (2005) 1397–1399.
[4] J.-Y. Kim, J.-M. Kang, T.-Y. Kim, S.-K. Han, 10 Gbit/s all-optical composite logic gates with XOR, NOR, OR and NAND functions using SOA-MZI structures, Electron. Lett 42 (5) (2006) 303–304.
[5] W. Wang, J. Yu, B. Han, J. Guo, J. Luo, J. Wang, Y. Liu, E. Yang, Experimental research on 10 Gb/s all-optical logic gates with return-to-zero data in high nonlinear fiber, in: 2011 Asia Communications and Photonics Conference and Exhibition (ACP), 2011, pp. 1–6.
[6] J. Qiu, K. Sun, M. Rochette, L.R. Chen, Reconfigurable all-optical multilogic gate (XOR, AND, and OR) based on cross-phase modulation in a highly nonlinear fiber, IEEE Photon. Technol. Lett. 22 (16) (2010) 1199–1201.
[7] L. Li, J. Wu, J. Qiu, B. Wu, K. Xu, X. Hong, Y. Li, J. Lin, Reconfigurable all-optical logic gate using four-wave mixing (FWM) in HNLF for NRZ-PolSK signal, Opt. Commun. 283 (19) (2010) 3608–3612.

[8] A. Bogoni, X. Wu, I. Fazal, A.E. Willner, 160 GB/s time-domain channel extraction/insertion and all-optical logic operations exploiting a single PPLN waveguide, J. Lightwave Technol. 27 (19) (2009) 4221–4227.
[9] J. Wang, J. Sun, Q. Sun, Proposal for all-optical switchable OR/XOR logic gates using sum-frequency generation, IEEE Photon. Technol. Lett. 19 (8) (2007) 541–543.
[10] Y.L. Lee, B.-A. Yu, T.J. Eom, W. Shin, Y.-C. Noh, D.-K. Ko, J. Lee, K. Oh, All-optical AND/NAND logic gates based on Ti:PPLN waveguide by cascaded nonlinear optical processes, in: Conference on Lasers and Electro-Optics/quantum Electronics and Laser Science Conference and Photonic Applications Systems Technologies, 2006, p. CThO3.
[11] R.R. Ghosh, A. Dhawan, Integrated non-volatile plasmonic switches based on phase-change-materials and their application to plasmonic logic circuits, Sci. Rep. 11 (1) (2021) 1–13.
[12] S. Swarnakar, K.B. Kumar, K.C. Yashwanth, V. Palacharla, A. Muduli, S. Kumar, A Y-shaped photonic integrated device with XNOR/NAND/NOR for optical signal processing, Opt. Quant. Electron. 55 (2023) 801.
[13] S. Swarnakar, S.P.K. Anguluri, A. Sreevani, S. Kumar, A novel structure of all-optical optimised NAND, NOR and XNOR logic gates employing a Y-shaped plasmonic waveguide for better performance and high-speed computations, Opt. Quant. Electron. 54 (2022) 530.
[14] I. Charles, A. Sreevani, S.V. Krishna, S. Swarnakar, P.S. Sharma, S. Kumar, Enhanced all-optical Y-shaped plasmonic OR, NOR and NAND gate models, analyses, and simulation for high speed computations, Opt. Quant. Electron. 54 (2022) 330.
[15] X. Tang, Y. Zhai, L. Sun, Y. Feng, D. Zhao, X. Zhang, L. Xi, W. Zhang, Implementation of a reconfigurable optical logic gate using a single I/Q modulator with direct detection, IEEE Photon. J. 8 (3) (2016) 1–8.
[16] M. Ding, X. Tang, J. Zhao, X. Zhang, and L. Xi, Experimental demonstration of a 32 GB/s reconfigurable logic gate using a dual-drive Mach-Zehnder modulator, in: *14th Pacific Rim Conference on Lasers and Electro-Optics (CLEO PR 2020)*, 1-3 (2020).
[17] G. Berrettini, A. Simi, A. Malacarne, A. Bogoni, L. Poti, Ultrafast integrable and reconfigurable XNOR, AND, NOR, and NOT photonic logic gate, IEEE Photon. Technol. Lett. 18 (8) (2006) 917–919.
[18] J.-Y. Kim, J.-M. Kang, T.-Y. Kim, S.-K. Han, All-optical multiple logic gates with XOR, NOR, OR, and NAND functions using parallel SOA-MZI structures: Theory and experiment, J. Lightwave Technol. 24 (9) (2006) 3392–3399.
[19] C.W. Son, S.H. Kim, Y.T. Byun, Y.M. Jhon, S. Lee, D.H. Woo, S.H. Kim, T.-H. Yoon, Realisation of all-optical multi-functional logic gates using semiconductor optical amplifiers, Electron. Lett 42 (18) (2006) 1057–1059.
[20] B.E.A. Saleh, M.C. Teich, Polarization and crystal optics, Fundament. Photon. 193–237 (1991).
[21] W. Zhai, A. Wen, W. Zhang, Z. Tu, H. Zhang, Z. Xiu, A multichannel phase tunable microwave photonic mixer with high conversion gain and elimination of dispersion-induced power fading, IEEE Photonics J. 10 (1) (2018) 1–10.
[22] X. Wang, J. Zhang, E.H.W. Chan, X. Feng, B. Guan, Ultra-wide bandwidth photonic microwave phase shifter with amplitude control function, Opt. Exp. 25 (3) (2017) 2883–2894.
[23] E.H.W. Chan, R.A. Minasian, Microwave photonic downconverter with high conversion efficiency, J. Lightwave Technol. 30 (23) (2012) 3580–3585.
[24] F. Heismann, S.K. Korotky, and J.J. Veselka, Lithium niobate integrated optics: Selected contemporary devices and system applications, in: Optical Fiber Telecommunications IIIB, Elsevier, 1997, pp. 377-462.
[25] C. Huang, E.H.W. Chan, Photonics-based serrodyne microwave frequency translator with large spurious suppression and phase shifting capability, J. Lightwave Technol. 39 (7) (2021) 2052–2058.