Memristor based XNOR for high speed area efficient 1-bit Full Adder

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***Abstract*—: Memristor technology has tendered the new dimensions in the semiconductor technology as a potential solution to offer high density, low power, non volatile digital logic and memory functions. In this paper nano-device property of Memristor has been utilized to design an area efficient high speed full adder. In comparison to other design of logic gate and full adder, the novel full adder circuit has the advantage of simplified architecture, better speed and higher power efficiency. The adder comprises of only 15 NMOS transistors and 15 Memristors. The design is simulated in SPICE and found that it produces better results when compared to equivalent 28T conventional CMOS full adder circuit in terms of area utilization, speed and power.**

Keywords— Memristor; Logic gates; Full adder; Computational Circuits

I. Introduction

The device level complexity of scaling the transistors with respect to CMOS technology has emerged as frictional bar to Moore's Law and the semiconductor technology has encountered major challenges and limitations not only from physical and technological point of view, but also from material (e.g., high-k vs. low k) and economical point of view as well [1]. This tradeoff has channelized and created the necessary design space towards new nano-elements to clear the above blockade. A promising new nano-element the Memristor has emerged which was conceptualized by Dr. L. O. Chua in 1971[2] and was physically materialized in 2008 by Hp labs [3].

Area efficient, low-power, nonvolatile, compatible to CMOS are some of the promising features of the Memristor which can be potentially leveraged in data storage, designing computational function circuits, Boolean logic operation circuits and intelligent neural networks. The Material-implication (IMP) logic gate realization using Memristor is offered in [4], but the IMP-based universal logic gates NAND, NOR need multiple IMP operations which take much time and cause the accumulation of error [5]. Different compositions of Memristors (series, anti-series, parallel and anti-parallel) are comprehensively analyzed in [6] and MRL basic logic gates are presented in [7]. A universal NOR gate with lesser delay and higher power efficiency is presented and can be utilized for designing higher order logic circuits [8].

XOR logic function being the basic building block as logic realization is an important circuit to design. The Material implication logic (IMP) realization of XOR with Memristors needs only 6 Memristors and two steps [9], compared to CMOS XOR logic gate which requires ten transistors and consumes more power. Another hybrid CMOS XOR gate is also recently presented, designed with four voltage controlled switches and one Memristor [10]. The architecture and power efficiency of XOR gate can turn the tables of designing in the whole system being a basic operational function, so it is inevitably desirable to design XOR gate with, simplified architecture, better speed and higher power efficiency.

A full adder is a critical component of Computation-IN-Memory architecture and is a functional building block of most of the complete computational circuits. The design criterion of a full adder is multidimensional, transistor count, power consumption and area being some of them. There is a tradeoff between design dimensions and several Memristor based adder circuits have been proposed [11-13]. The design philosophy of these circuits can be concluded in two ways, one way is using Memristor based multilevel storage and unique number system leveraging the feature of dividing memristance into levels, representing a certain value for each level [11].With this way having drawback of getting the resistance values around margin possibly wrong ,the other way to overcome this is to design full adder using logic operations [12-13], but this way needs multiple steps forcing for complicated circuits and higher power consumption. A different approach, the hybrid Memristor-based adder implemented with the NOR gate as basic cell has shown remarkable improvement in speed, and power efficiency [8].

A novel design of XNOR logic gate using three Memristor and three NMOS by a single step is introduced through this paper. Leveraging the novel design of the gate a new one bit full adder circuit, with advantages of simplified architecture, better speed and higher power efficiency, is presented and simulation is performed by LTSPICE.

The organization of paper is as, Memristor and digital logic circuits are presented in section II. The Proposed XNOR logic circuit and its application in a novel full adder circuit are described in section III. Section IV is presented with simulation results and analysis. Section V gives the conclusion and the future scope.

II. Memristor and Digital Logic Circuits

Memristor was conceptualized by L. O. Chua in 1971 [2] as the fourth basic circuit element and after almost 40 years,

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Stanley Williams Group in HP Labs physically realized a two-terminal titanium dioxide nano-scale device manifesting Memristive characteristic [3]. Variation in the applied voltage or current makes the resistances of memristive devices vary and devices behave as two states switches when overdriven by large voltages, and exhibits hysteresis properties if small voltage is applied [2-3]. This confirms Memristor to be used in designing logic circuits, arrays and many other logic structures.

A. Memristor

The Memristor is a two terminal passive element, exhibits relationship between charge and magnetic flux defined as:

$$M = d\varphi/dq \tag{1}$$

where M is the Memristance (Ω), φ and q are the magnetic flux and charge, respectively. Stanley Williams Group developed TiO_2-based Memristor having a thin undoped titanium-dioxide layer (undoped region) and a doped TiO_{2-X} layer (doped region) which is having deficiency of oxygen. The layers are arrested between two platinum electrodes. Memristance depends on the width of undoped region, which can be varied through variation of applied current or voltage. The behaviour of resistance in Memristor realized by HP can be given by [3]:

$$R(w) = R_{on}\frac{w}{D} + R_{off}\left(1 - \frac{w}{D}\right) \tag{2}$$

where R(w) is the memristance at time t, w is the width of the doped region at time t, D is the thickness of the semiconductor layer TiO_2 , R_{ON} is the low resistance when the semiconductor layer TiO_2 is completely doped and R_{OFF} is the high resistance when the semiconductor layer TiO_2 is completely undoped. The non-linear drift model formed on the basis of the linear-drift model is used in this paper to model the memristor. The boundary effect is taken into account in the model of nonlinear dopant drift, by using a window function F(x(t)) as,

$$x(t) = w(t)/D \tag{3}$$

where x is the width of the doped region, referenced to the total length D of the TiO_2 layer.

$$dx(t)/dt = k.I(t).F(x(t)) \tag{4}$$

where I(t) is the charge derivative with respect to time, k is a constant and F(x(t)) is defined as Biolek window function as,

$$F\big(x(t)\big) = 1 - (x(t) - stp\big(-I(t)\big))^{2p} \tag{5}$$

$$stp\big(I(t)\big) = \begin{cases} 1 & \text{if } I(t) > 0 \\ 0 & \text{if } I(t) < 0 \end{cases}$$

Where p must be a positive integer [14].

B. Memristor based logic circuits

The logic circuit based on MRL (Memristor Ratioed Logic) family uses the programmable resistance of Memristive devices for computation of Boolean AND/OR functions with voltage as the state variable. Consistent with the CMOS technology where the logic state is represented as voltage in MRL, the Memristive devices are utilized solely for logic computation, and not as a storage element [15]. Since logic gates in this family are non-inverting, a complete logic structure can be achieved by adding a standard CMOS inverter as shown in Fig. 1. This approach is beneficial to extend Moore's law when CMOS scaling becomes problematic and increase the number of logic gates by more than the traditional factor of two [7].

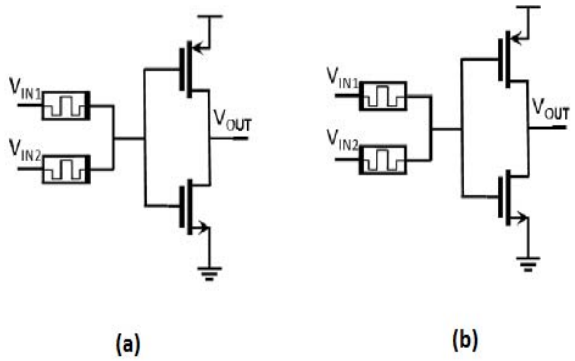


Fig.1. Schematic of an (a) two-input MRL NAND, and (b) two-input MRL NOR

The above design strategy can be further improved if we can remove the PMOS transistor from the design which will result in the faster logic leveraging the benefits of NMOS devices over PMOS. This design style proposed in [8] offers an advantage that an inverter gate can also be realized using Memristor. The schematic of an inverter using one Memristor and one NMOS is shown Fig 2(a).According to Kirchhoff's Law, the output voltage V_{OUT} can be given as follows,

$$V_{out} = \frac{R_T}{R_T + R_M}.V_{cc} \tag{6}$$

If V_{IN} = 0 (logic Low), NMOS drives into cutoff region , reistance offered by NMOS ,R_T=R_{CutOff}, Memristance, R_M=R_{OFF}. As, R_{CutOff} >> R_{OFF} from (6),

$$V_{out} \approx V_{cc}(Logic\ HIGH)$$

When V_{IN} = 1 (logic HIGH), NMOS drives into saturation region , R_T = R_{sat} , R_M = R_{OFF} As ,R_{sat}≈ 0, from (6),

$$V_{out} \approx 0(Logic\ LOW)$$

The design confirms the truth table for inverter and the same logic can be further extended to implement NOR logic as exhibited through Fig. 2(b).

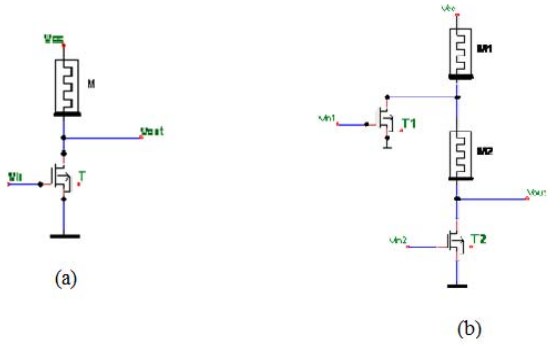
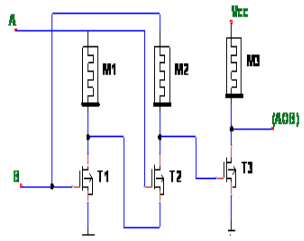


Fig. 2: Schematic of an (a) inverter and (b) NOR gate using Memristor (M) and NMOS (T) only.

III. Memristive XNOR & Full Adder

A. A Novel Memristive XNOR Circuit

Based on the logic design circuits a new kind of Memristor based XNOR circuit is designed and presented. The offered XNOR circuit comprises of three Memristor and three NMOS as shown in Fig. 3(a). V_A and V_B are the input voltages ,the value of V_{T3} is the output voltage.



V(A)	V(B)	V(T3)
0	0	1
0	1	0
1	0	0
1	1	1

(a) (b)

Fig. 3: Proposed design of XNOR gate. (a) XNOR gate designed using Memristor (M, M2, M3) and NMOS (T1, T2, T3). (b) Truth table for XNOR gate

When V_A and V_B =0(LOW), Transistors T1, T2 and T3 are in cutoff region and voltage at T3, $V_{T\ 3} \approx$ Vcc(HIGH). If V_A =0(LOW) and V_B =1(HIGH), T1 is in saturation region, T2 is in cutoff region and through Memristor M2 the voltage at input of T3 is HIGH driving T3 into saturation region and voltage at T3, $V_{T\ 3} \approx$ 0(LOW). When V_A = 1 (HIGH) and V_B =0(LOW), T1 is in cutoff region, T2 is in saturation region and through Memristor M1, the voltage at source terminal of T2 is HIGH, which makes the voltage at input of T3 as HIGH driving NMOS T3 into saturation region and the voltage at T3, $V_{T\ 3} \approx$ 0(LOW). If V_A and V_B =1(HIGH), T1, T2 are in saturation region and T3 is in cutoff and voltage at T3, $V_{T\ 3} \approx$ Vcc(HIGH). The circuit behaves in confirmation with truth table of XNOR gate Fig. 3(b) and the operation is in a single step.

B. A Full Adder Circuit Design

Leveraging the design of this XNOR circuit, a novel adder circuit is presented. Probably the simplest approach to design an adder is to implement gates to yield the majority of required logic functions. The general equations for SUM and Cout derived from the truth table of an adder are given as,

$$\text{SUM, S} = \text{A} \oplus \text{B} \oplus C_{in} \tag{7}$$

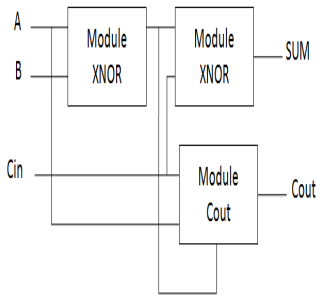
$$\text{CARRY}, C_{out} = \text{A.B} + C_{in}(\text{A} \oplus \text{B}) \tag{8}$$

These functions can be rearranged in XNOR expressions as below so that XNOR gates can be utilized to carry out majority of implementation.

$$\text{S} = \text{A} \odot \text{B} \odot \text{Cin} \tag{9}$$

$$\text{Cout} = \text{A} \odot \text{BCin}' + \text{A} \oplus \text{B Cin} \tag{10}$$

The block diagram for the direct implementation of the modified Boolean expression is exhibited in Fig. 4(a) and the truth table is in Fig. 4(b).



X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) (b)

Fig. 4: Full adder (a) Schematic Block Diagram for full adder. (b) Truth Table for full Adder

As shown in Fig. 5, the designed new XNOR circuit based full adder comprises of 15 NMOS and 15 Memristor only. Voltage at NMOS, T1, T2 and T5 are input voltages and Voltage at T6 and T15 are SUM and Carry Out respectively. The proposed adder implement the Sum using Memristor-based XNOR-XNOR stage and C_{out} using Memristor-based NOR-NOR stage.

IV. Simulation and Analysis

In this section the proposed XNOR and full Adder circuit is simulated in LTSPICE. The Memristive model proposed by Zdenek and Dalibor Biolek [14] is used to realize Memristive device. For the simulation of the Memristor for its desired characteristics, the width D of the TiO2 film is considered to be 10nm and the dopant mobility $\mu v \cong 10^{-14}\ m^2 s^{-1} V^{-1}$. The

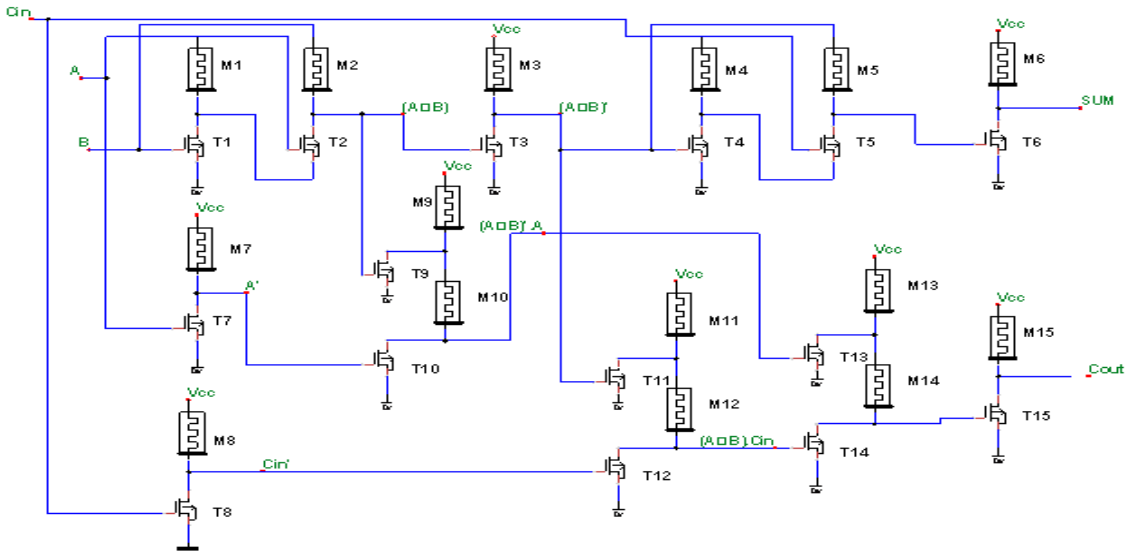


Fig. 5: A design of proposed Full Adder

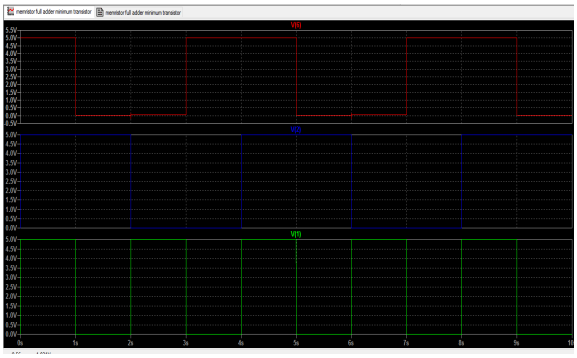


Fig. 6: Simulation results for XNOR operation

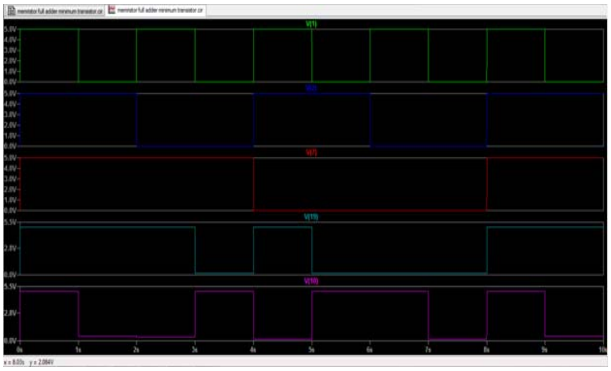


Fig. 7: Transient Response of Proposed Full Adder

values assumed for Ron = 1k, Roff = 100k and the initial resistance Rinit = 80k.

Fig. 6, shows the result of the XNOR circuit for the four possible input combinations. V(1) and V(2) are inputs and V(6) is the output of XNOR circuit in simulation results. The proposed circuit can be used for XNOR operation in a single step and is verified through simulation results. The transient response of proposed full adder circuit is shown in Fig. 7. V(1), V(2) and V(7) are taken as inputs, V(10) and V(19) are taken as sum and carry outputs respectively in simulation results Fig. 7. The proposed adder is analyzed with respect to its power consumption and total delay by providing all the possible input vector combinations.

TABLE 1: Comparison analysis between CMOS and XNOR based proposed Full Adder using Memristor

Parameters	**CMOS Adder**	**Memristor based Adder**	**Proposed Adder**
Total no of transistors	28	24	15
Delay	1.09ns	0.41ns	0.1ns
Power Consumption	150.2mw	1.9mw	1.3mw

Simulation result confirms that the proposed full adder gives 91% improvement in transient delay analysis and 99% improvement in average power consumption with respect to the conventional 28T CMOS full adder. Compared with another Memristive NOR based full adder consisted of 24 Memristor and 24 NMOS [8], the percentage improvement in transient delay is 75% and 32% improvement in average power efficiency. Table 1, describes the performance analysis of new XNOR based Full adder circuit.

V. Conclusion

Through the paper, a Memristor-based XNOR logic gate with 3 Memristors and 3 NMOS, which can execute XNOR operation in a single step, is presented. Leveraging this logic gate, a novel 1 bit full adder circuit is designed. The truth tables for the XNOR gate and full adder are simulated and substantiated by LTSPICE. In comparison to other design of logic gate and full adder, the tendered full adder circuit has the advantage of simplified architecture, better speed and higher power efficiency. The prime philosophy of the work is to provide a Memristor-based solution for designing the alternative Computation-In-Memory architecture and effective extension of Moore's Law. Based on the performance of adder circuits, this work can be extended further on complex logic architectures like encoder, multipliers, comparators & ALU etc.

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