

A Project Report on

# LOW POWER MEMRISTOR-BASED 3-BIT ENCODER DESIGN

*is submitted in partial fulfillment of the requirement for the award of the Degree of  
Bachelor of Technology*

*to*



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY  
ANANTAPUR, ANANTHAPURAMU**

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### CERTIFICATE

This is to certify that the project report entitled **“LOW POWER MEMRISTOR-BASED 3-BIT ENCODER DESIGN”** being submitted by **SD. JAVEED (19711A04A9), M.N. ROHITH (19711A0473), M. VENKATA SUBBAIAH (19711A0470), SK. MASTHAN (19711A04A1)** in partial fulfillment for the award of the Degree of Bachelor of Technology in Electronics & Communication Engineering Department to the Jawaharlal Nehru Technological University Anantapur, Ananthapuramu is a record of bonafied work carried out by them under my guidance and supervision.

The results embodied in this project report have not been submitted to any other University or Institute for the award of any Degree or Diploma.

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## **ABSTRACT**

In this project, power dissipation is reduced in digital circuits using memristors. The use of memristors in the design of digital logic gates presents an alternative approach to current integrated circuit (IC) design and is a promising development in computing architecture. The manufacturing process for memristor-based gates is straightforward, as memristors can be designed on top of the polysilicon gate of NMOS transistors. This can lead to an increase in transistor density on a chip. Additionally, to achieve even lower power consumption, we are tweaking the memristor's  $R_{on}$ ,  $R_{off}$ , and  $R_{int}$  values in this project. The memristor-based design can be utilised to model various combinational logic circuits, and the primary objective of this paper is to analyse and design a 3-bit encoder with different logics using LTspice.

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# CHAPTER 1

## INTRODUCTION

The ever growing demand of high end computing applications have posed the challenge of continuous technology upgradation. The upgrade in technology has enabled the complex applications like Cloud computing, Real-time transitions on huge databases, Biotechnological computations a reality. Technological advancements in terms of higher operational frequency and miniaturisation of chips in recent years have generated sufficient computing power to enable this growth. As predicted by Gordon Moore in 1960, popularly known as Moore's law, the transistor count in a chip will double every one and half years on the average. Transistor growth is shown by Gordon Moore in figure 1.1. ITRS (International Technology Roadmap for Semiconductors) has also drawn a road-map of required feature size in the future at atomic level in 2050. Shrinking in feature size resulted in a number of implementation and operational difficulties like heat dissipation, requirement of very thin laser beam, clock distribution etc

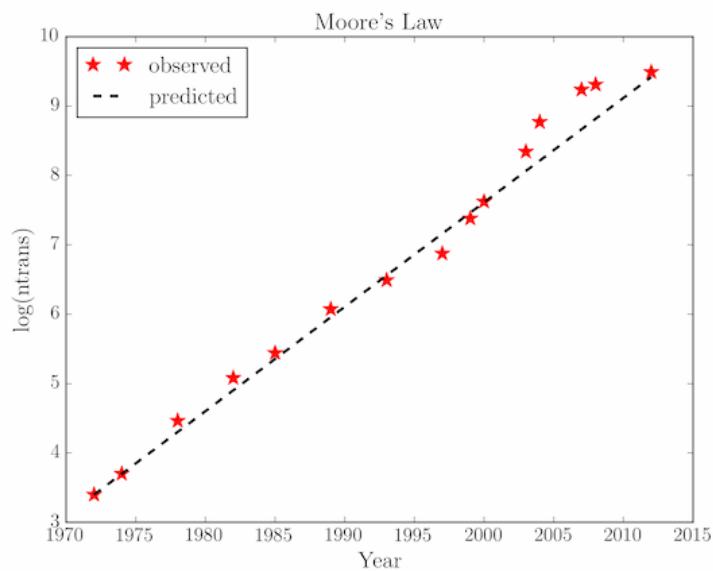


Fig. 1.1 Moore law's graph for transistors

Current technologies are finding it difficult to continue with the required level of growth. Alternative technologies are emerging to take place so that the growth momentum can be continued.

## 1.1 LIMITATIONS

Conventional technology has dominated the computing world for more than the last three decades. Right from the basic gates like AND, OR, NOT, EXOR, NAND etc. multimillion gates circuits have become available as per the need of the applications. As technology continues to advance, the size of VLSI (Very Large Scale Integration) circuits continues to shrink. While this trend brings many benefits, such as increased computing power and reduced cost, it also presents significant challenges related to power dissipation. In this paragraph, we will explore how making VLSI circuits smaller causes problems with power dissipation and the impact that these challenges can have on circuit performance.

One of the primary ways that making VLSI circuits smaller leads to power dissipation problems is through increased current density. When you pack more transistors into a smaller area, the current density within the circuit increases. This means that more current is flowing through a smaller area, which can cause the temperature of the circuit to rise. This increase in temperature can cause problems with overheating and can potentially damage the components within the circuit. Another challenge associated with making VLSI circuits smaller is increased leakage currents. As the size of transistors decreases, so does the thickness of the insulating layers that separate the various components of the transistor. Shorter interconnects are another issue that arises with smaller VLSI circuits. As the circuit size decreases, so do the interconnects between components. This can lead to problems with resistance and capacitance, which can increase power dissipation and cause signal degradation. These issues are particularly pronounced in high-speed circuits, where the interconnects must be carefully designed to avoid timing issues and signal integrity problems. In addition to these technical challenges, making VLSI circuits smaller also presents logistical challenges related to thermal management. As circuits become smaller, the available space for cooling components also decreases. Overheating can cause a range of problems, including reduced circuit lifetime, degraded performance, and potential damage to the components. Despite these challenges, there are many techniques that can be used to address the power dissipation problems associated with smaller VLSI circuits.

For example, designers can use low-power design techniques to reduce power consumption and heat generation. memristor can also use more efficient power delivery networks and power management strategies to minimise power dissipation. In addition, cooling techniques such as heat sinks, fans, and liquid cooling systems can be used to manage the thermal challenges associated with smaller circuits.

In conclusion, while making VLSI circuits smaller brings many benefits, such as increased computing power and reduced cost, it also presents significant challenges related to power dissipation. Increased current density, leakage currents, shorter interconnects, and limited cooling options are all issues that must be addressed in order to ensure that the circuits can function reliably and efficiently. Despite these challenges, there are many techniques that can be used to mitigate the impact of power dissipation on circuit performance, including low-power design techniques, efficient power delivery networks, power management strategies, and cooling techniques. As technology continues to evolve, it is likely that new approaches to addressing power dissipation in smaller VLSI circuits will continue to emerge, helping to ensure that these circuits remain an important tool in the development of new technologies and applications.

The Problems, which may arise in conventional design can be classified in following types.

1. Physical problems
2. Operational Speed

#### **1.1.1 Physical Problems**

The power dissipation issues in smaller VLSI circuits can lead to several physical problems that can affect the performance and reliability of the circuit. The most common issues include overheating, which can cause permanent damage and reduce the lifetime of the circuit. Another problem is signal degradation, caused by resistance and capacitance issues due to smaller interconnects between components. This can affect the overall performance of the circuit. Reduced circuit lifetime is also a concern, particularly in applications such as aerospace or medical devices where reliability is critical. Electromigration, a phenomenon that can occur in VLSI circuits when current flows through the interconnects, can lead to potential circuit failure due to metal migration over time.

### **1.1.2 Operational Speed**

The power dissipation issues associated with smaller VLSI circuits can also cause problems with operational speed. As circuits become smaller and more complex, the number of transistors on a chip increases, which can lead to increased power consumption and heat generation. This, in turn, can cause a reduction in operational speed. One of the primary factors that can impact operational speed is the delay caused by the resistance and capacitance of the interconnects. As circuits become smaller, the resistance and capacitance of the interconnects increase, which can cause signal delay and limit operational speed. Another factor that can impact operational speed is power supply noise. As power consumption increases, voltage fluctuations can occur, which can cause noise in the power supply. This noise can interfere with the timing of signals and limit operational speed. The thermal effects of power dissipation can also impact operational speed. As circuits become smaller and power density increases, the temperature of the circuit can rise rapidly. This, in turn, can cause the performance of the circuit to degrade, leading to slower operational speeds. Overall, the power dissipation issues associated with smaller VLSI circuits can have a significant impact on operational speed. To mitigate these issues, designers must carefully consider the impact of power consumption on the interconnects, power supply noise, and thermal effects. By implementing efficient power management, effective thermal management strategies, and careful design, designers can mitigate the impact of power dissipation on operational speed and improve the overall performance of VLSI circuits. Power dissipation due to scaling is a significant issue in VLSI, which affects both the reliability and performance of the circuit. As the number of transistors on a chip increases and feature sizes reduce, the power density also increases, leading to thermal problems that can cause delays in signal propagation and reduced performance. The high power consumption generates heat, which can increase the temperature of the chip, affecting carrier mobility and leading to increased parasitic capacitance and resistance, resulting in longer signal propagation delays. To address this issue, designers employ various techniques, however these techniques can also have their limitations, and power dissipation remains a critical concern in VLSI that requires further research and development to ensure optimal performance.

## **1.2 INTRODUCTION TO VLSI DOMAIN**

Due to the complexity of modern VLSI designs and applications, manual techniques for designing circuits have become impractical. As a result, automation in design has become the norm. Recent rapid advancements in technology have led to a consistent rise in the functionality and size of ICs, along with an increase in operating speed and gate density due to a constant reduction in feature size. Additionally, there has been a steady improvement in the predictability of circuit behaviour and a rise in the number and diversity of software tools available for VLSI design. As a consequence of these breakthroughs, numerous VLSI design methodologies have emerged, including VLSI computation. Moreover, the use of VLSI computation techniques can also help reduce power dissipation. By analyzing the computations performed by large integrated networks, it is possible to optimize the circuit design to reduce power consumption. Additionally, VLSI computation can help identify power-hungry portions of the circuit, allowing designers to optimize those sections to reduce power consumption. Overall, VLSI computation can help designers develop more power-efficient circuits, improving the circuit's reliability and longevity.

### **1.2.1 History Of VLSI**

The fundamental building blocks of digital systems, switching networks, were historically implemented by connecting discrete electrical elements like transistors, resistors, capacitors, etc. using conducting wires. The first transistors, the basic switching components, were created by properly altering several areas on the surface of a semiconductor material.

In the late 1950s, a significant innovation took place. The history of VLSI (Very Large Scale Integration) dates back to the 1960s when the first integrated circuits (ICs) were developed. These early ICs contained a few transistors and were used primarily in military and aerospace applications. However, the field of VLSI did not truly take off until the 1970s when advances in lithography and materials science enabled the production of ICs with thousands of transistors. This led to the development of microprocessors, which revolutionized the field of computing. In the 1980s, the introduction of complementary metal-oxide-semiconductor (CMOS) technology further improved the performance of ICs, leading to the development of more advanced

microprocessors, memory devices, and other electronic systems. Since then, the field of VLSI has continued to evolve, with continued advances in lithography, materials science, and design techniques enabling the production of ICs with billions of transistors. Today, VLSI technology is used in a wide range of applications, including computing, telecommunications, automotive, and consumer electronics, and is a critical component of modern technology.

### 1.2.2 VLSI Design Flow

The process of creating Integrated Circuits (ICs) through the very large scale integration (VLSI) of several components such as resistors, transistors, and capacitors on a single chip. The process of VLSI design is iterative. Problems like functional design, logic design, circuit design, and physical design are all part of designing a VLSI chip. Simulating the design process allows for accuracy checks. If a design fault is discovered at any point throughout the verification process, at least one of the prior design processes must be redone in order to fix the problem.

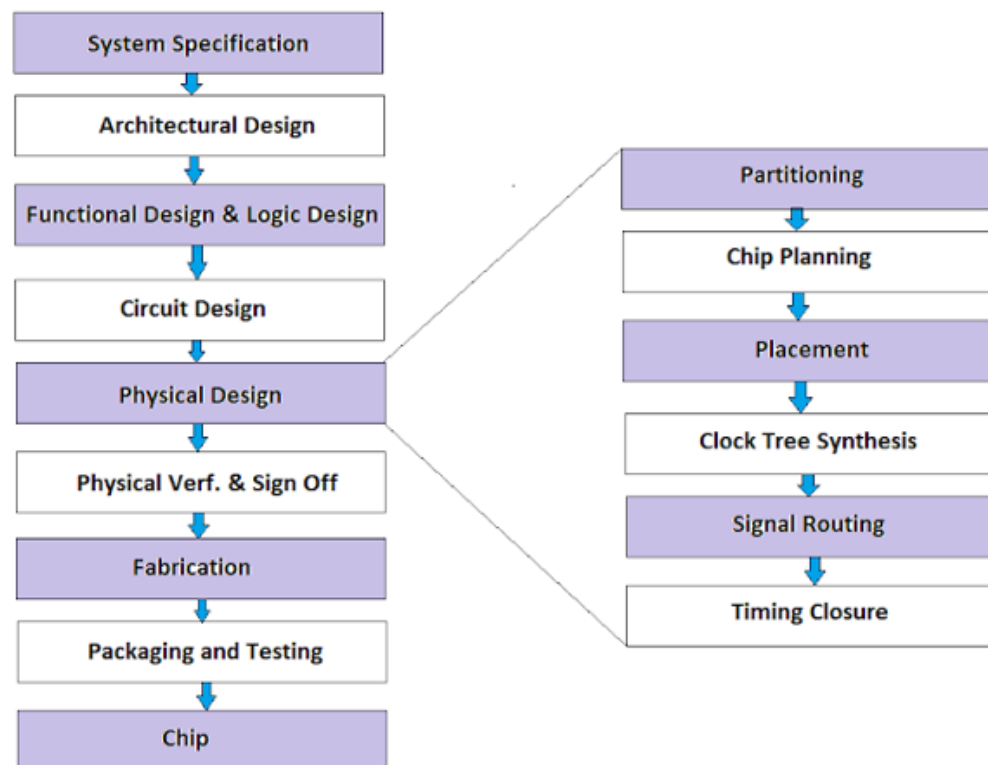


Fig. 1.2 VLSI design flow

### 1.2.3 Introduction To Memristors

Introduction of the memristor has paved the way to many inventions in the VLSI domain. The properties of memristor such as the nanometer scale measurements and its non-volatile memory qualities have yielded more attention towards research people. The nanometer scale highlight of the memristor makes another door open for the realisation of innovative circuits for logic blocks from the more standard designs. Non-volatile memory property empowers us to acknowledge new outline strategies for an assortment of computational components that prompt novel models. By this, there comes the idea of the combination of the Nano-scale memristor and CMOS, which ends up conceivable to diminish usage of silicon territory accordingly giving a promising alternative in the plan of memristor and CMOS based circuits.

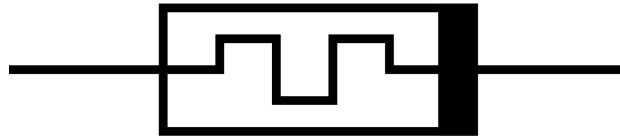


Fig. 1.3 Memristor symbol

Memristors are a type of passive two-terminal electronic component that have garnered increasing interest in the field of VLSI design due to their potential to address some of the challenges associated with conventional semiconductor technologies. Unlike transistors, which are commonly used to build digital logic and memory devices in VLSI, memristors offer the possibility of non-volatile memory and analog computation. This is due to their unique ability to change their resistance in response to the voltage applied across them, which allows them to store information and perform computations. Memristors are also capable of emulating the synapses in neural networks, which makes them attractive for building neuromorphic computing systems. The use of memristors in VLSI design could lead to more energy-efficient and faster computing systems, as well as new applications in areas such as artificial intelligence and machine learning. However, there are still many technical challenges that must be overcome before memristors can be widely adopted in VLSI design, including issues related to reliability and scalability with existing manufacturing processes.



### 1.2.4 Encoders

An encoder refers to a system or device that converts information from one format to another. Encoders are commonly used in digital communication systems to ensure that data is transmitted accurately and efficiently. The process of encoding involves taking a stream of data and converting it into a standardized format that can be easily transmitted or stored. This is achieved by mapping the original data to a set of binary digits, which are then transmitted or stored as a series of electrical or optical signals. Encoders can be used in a wide range of applications, including multimedia compression, error correction, and encryption.

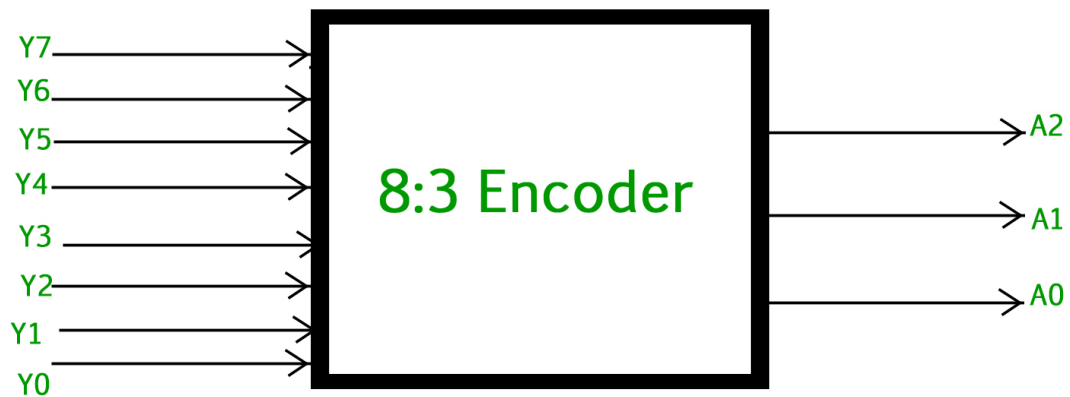


Fig. 1.4 3-bit Encoder

A 3-bit encoder is a type of encoder that can take 3 input bits and produce a corresponding output code based on the binary value of the input. The output of the encoder will be a unique binary code for each possible combination of the 3 input bits. The encoding process involves mapping each input combination to a unique output code.

$$A0 = Y7 + Y5 + Y3 + Y1$$

$$A1 = Y7 + Y6 + Y5 + Y4$$

$$A2 = Y7 + Y6 + Y3 + Y2$$

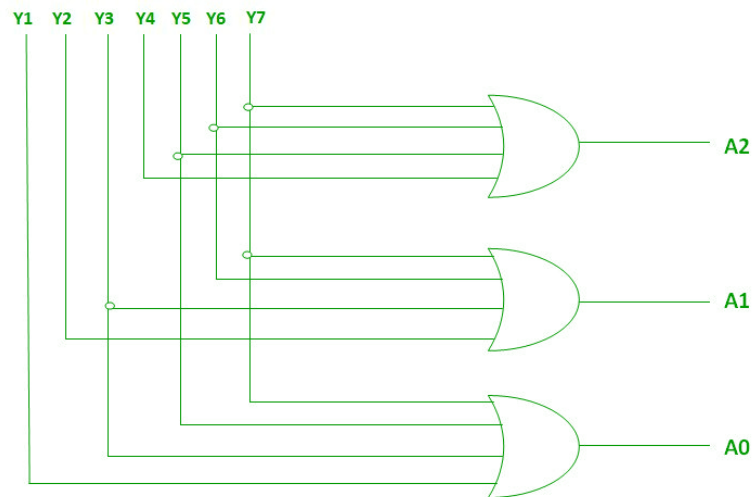


Fig. 1.5 Encoder in digital logic

An encoder is a combinational circuit that performs the reverse operation of decoder. It has a maximum of  $2^n$  input lines and 'n' output lines, hence it encodes the information from  $2^n$  inputs into an n-bit code. It will produce a binary code equivalent to the input, which is active high.

Table 1.1 Truth table for 8 to 3 encoder

INPUTS								OUTPUTS		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A2	A1	A0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Therefore, the encoder encodes  $2^n$  input lines with 'n' bits. The 3 bit encoder or octal to Binary encoder consists of 8 inputs : Y7 to Y0 and 3 outputs : A2, A1 & A0. Each input line corresponds to each octal digit and three outputs generate corresponding binary code.

## **CHAPTER 2**

### **LITERATURE SURVEY**

As the field of electronics has advanced, there has been a constant need to develop more efficient and reliable devices. With the discovery of memristors, a new era in electronics has been opened. Memristors are novel devices that have the unique property of being able to remember their previous state. This property has made them highly attractive for use in various applications, including logic gates. In this section, we will discuss how memristors work and can be used as logic gates. Memristors, also known as memory resistors, are a type of passive electrical component that has the potential to revolutionise the field of VLSI design. Unlike traditional resistors, which only dissipate energy, memristors have the ability to store and process information. This makes them an incredibly powerful tool for building high-performance circuits with low power consumption. In fact, some experts believe that memristors could be the key to unlocking a new era of computing, where devices are more intelligent, energy-efficient, and capable of processing vast amounts of data in real-time. While the technology is still in its early stages of development, researchers are working tirelessly to unlock the full potential of memristors and pave the way for a new era of VLSI design.

As presented in memristor has different voltage and current curve when compared to the basic resistor, inductor and capacitor which is called as the pinched hysteresis loop which can states as below when we increase the positive voltage of the memristor current through it will increase very small and this state is called as the high resistance state and if we further increase the voltage slightly then the current through it will increase rapidly and reached state called as the low resistance state and we will be using these states for our switching and from the low resistance state if you decrease the positive voltage the current will decrease gradually and it reaches zero when the voltage reaches zero and if you decrease the negative voltage current will decrease slowly and reaches the high resistance state and if voltage still reduces the current will decrease rapidly and reaches the low resistance state and from this point if you increase the negative voltage, current will also increase and when the voltage reaches near zero the current will also reach zero. This phenomenon of curve intersecting at the zero voltage and zero current is called as the pinched

## 2.1 A BRIEF OVERVIEW ON MEMRISTORS

The memory resistor idea was first developed in 1971 by Dr. Leon Chua, a professor at California University. He referred to it as a memristor, a passive electrical component. Professor Chua noticed a missing relationship in circuit theory, which led to the existence of a fourth passive fundamental element. Although memory resistors always follow the fundamental circuit, and variables of voltage, current, and their time integrals, memristor have a dynamic function with memory and can be described as a net load function.

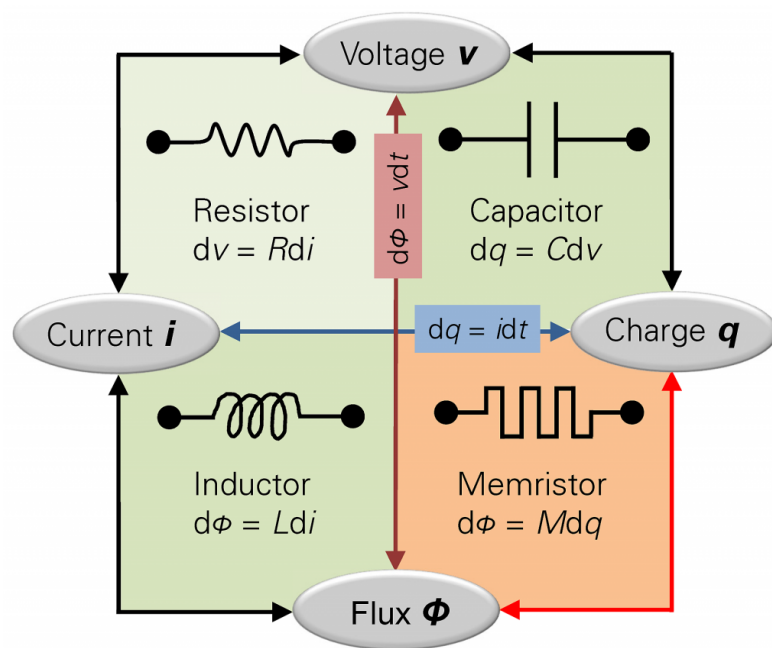


Fig. 2.1 Relationship between fundamental devices

### 2.1.1 Titanium-dioxide Memristors

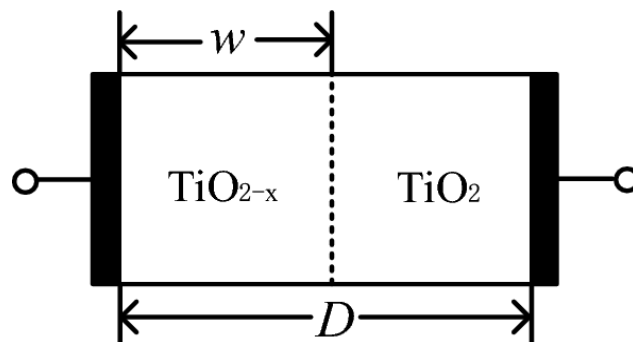


Fig. 2.2 TiO<sub>2</sub> memristor

There are several types of memristors, including titanium dioxide ( $\text{TiO}_2$ ), tantalum oxide ( $\text{Ta}_2\text{O}_5$ ), and polymeric memristors.  $\text{TiO}_2$ -based memristors are the most widely used because memristor are easy to fabricate, exhibit stable switching behaviour, and are highly compatible with CMOS technology.  $\text{TiO}_2$ -based memristors have been extensively studied and are currently used in various applications, including memory storage, neuromorphic computing, and logic gates. Titanium dioxide memristors are a type of memristor that is made using a thin film of titanium dioxide sandwiched between two metal electrodes. When an electric current is applied to the memristor, the resistance of the titanium dioxide film changes, causing the memristor to store information. Unlike traditional memory devices, which rely on the physical movement of electrons to store information, memristors use a process called resistive switching, where the movement of ions in the titanium dioxide film is used to change its resistance. This makes them an incredibly efficient and fast way of storing and processing information.

In recent years, researchers have shown that titanium dioxide memristors have several advantages over other types of memristors. For one, memristor have a high switching speed, which means that memristor can switch between states quickly and efficiently. Additionally, memristor have a low power consumption, which makes them ideal for use in applications where power efficiency is critical, such as in mobile devices. To make titanium dioxide memristors, a thin film of titanium dioxide is deposited onto a substrate using a technique such as sputtering or atomic layer deposition. The thickness of the film is typically in the range of a few nanometers to a few tens of nanometers. Metal electrodes are then deposited on top of the titanium dioxide film, forming a device structure known as a metal-insulator-metal (MIM) structure. The device can then be annealed at high temperatures to improve the quality of the titanium dioxide film and optimise the device's properties. While titanium dioxide memristors are still in the early stages of development, researchers are continuing to explore their potential for use in a variety of applications, from memory storage to signal processing. The fact that memristor can be mass-produced using existing semiconductor fabrication techniques makes them an attractive option for VLSI design, and many researchers are working to optimise their properties and improve their performance.

### 2.1.2 Characteristics Of Memristors

The characteristic V-i hysteresis curve of a memristor triggered by a periodic signal, such as square, sinusoidal, etc., serves as an important illustration of the device. From the following figure, it can be observed that for a memristor activated by a periodic signal (square or sinusoidal), the Hysteresis loop of the memristor.

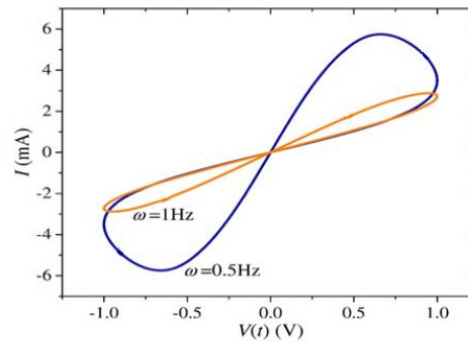


Fig. 2.3 Hysteresis curve

when the voltage is 0, the current is also zero, and vice versa. Therefore, the voltage and the (v, i) current both conform to the same zero crossing. We will present the polarity of the memristor as shown in Figure if the current is flowing into the black mark then the resistance of the device becomes less and current flowing out of the black mark the resistance of the device increases

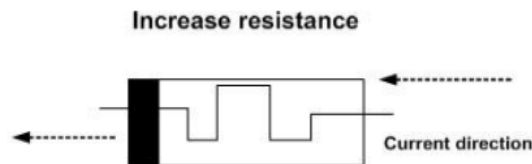


Fig. 2.4 Direction for increased resistance

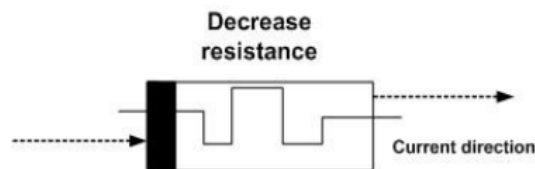


Fig. 2.5 Direction for decreased resistance

## 2.2 MEMRISTOR AS LOGIC GATES

Traditionally, logic gates are made up of transistors that act as switches. The performance of these gates depends on the number of transistors used and their corresponding connections. However, with the advent of memristors, there is a possibility of creating logic gates with fewer components, which could lead to improved performance and reduced power consumption. In memristor-based logic gates, the memristor is used as a switching element instead of a transistor. The resistance of the memristor can be changed by applying a voltage or current to it.

### 2.2.1 Logic AND

As shown below AND logic operation as follows if both the inputs are having logic 0 or memristor are connected to the ground we assume that the output node is floating, so there is no voltage upon the memristor, therefore, there is no current flow through the memristor, so the output is also ground or logical 0. If both the input nodes are connected to VDD or having logical 1 both nodes are same voltage again no current flows through the memristor so the input voltage appears across the output which is logical 1, now if one input is 1 and another input is 0, if the two cases so consider one in this case one input is logical 1 and another input is logical 0 so current flows from the upper memristor to the bottom memristor and because of the polarity of the memristor the resistance of the upper one is increased and the resistance of the lower one is decreasing so after enough time of this voltages will achieve the maximum resistance of the upper memristor  $R_{off}$  and minimum resistance for the lower memristor  $R_{on}$  so it just a regular voltage divider and therefore the output resistance is under the assumption that  $R_{off}$  is significantly higher than  $R_{on}$ , the voltage at the output is approximately equal to ground or logical 0.

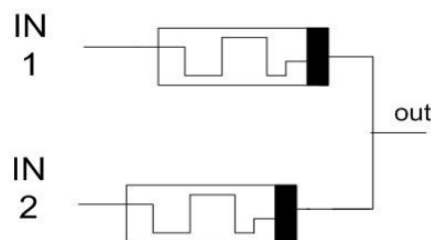


Fig. 2.6 Memristive logic AND

### 2.2.2 Logic OR

OR gate just interchange the terminals of the memristor, for the case where both the inputs are the same logical value again no current is flowing then again the output will be same voltage as the input voltage, when both inputs are logical 0 output will be logical 0, and both inputs are logical 1 then the output will be logical 1, if consider the Other two scenarios when the upper memristor input is logical 1 and lower memristor input is logical 0 current will flows from upper memristor to lower memristor, now the upper memristor resistance decreases and the lower memristor resistance increases after enough time will get the minimum resistance  $R_{on}$  in the upper memristor and the maximum resistance for the lower memristor and again it acts as a voltage divider output is logical 1( $V_{CC}$ )

The ability of memristors to remember their previous state can be exploited to create latch circuits, flip-flops, and registers, which are essential building blocks of digital systems. As the field of electronics continues to advance, memristors are expected to play an increasingly role.

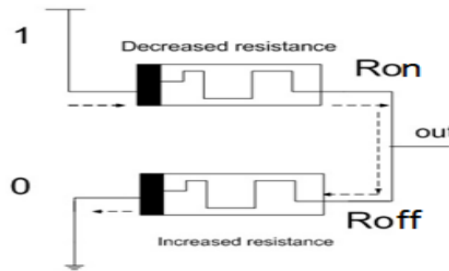


Fig. 2.7 Memristive logic OR

A memory element can function as a logic gate due to its ability to store and output data based on the inputs received. When used as a logic gate, the memory element compares the input data with the stored data and generates an output signal based on the logic function performed by the circuit. The output signal is then stored in the memory element for future use. Memory elements commonly used as logic gates include flip-flops, latches, and registers, which have different operating characteristics and applications. The memory element can perform logic functions such as AND, OR, NOT, and XOR, allowing it to implement complex digital circuits. The use of memory elements as logic gates provides high-speed operation and high-density integration, making it a popular choice in modern VLSI design.



Some of the advantages of using memristors for AND and OR gates are:

- **Low Power Consumption**

Memristors consume significantly less power than traditional transistors, making them ideal for low-power applications. This advantage is particularly important for AND gates, which are often used in digital circuits to perform power-intensive operations.

- **High Speed**

Memristors can switch states at a much faster rate than transistors, which results in faster AND gate operations. This speed advantage is essential for applications that require high-speed processing, such as digital signal processing.

- **Improved Accuracy**

Memristors are known for their high accuracy and precision, which makes them ideal for OR gates that require accurate inputs to produce accurate outputs. This advantage is particularly important for applications such as data analysis and machine learning, where accuracy is critical.

While memristors have several advantages some of the disadvantages of using memristors for AND and OR gates are:

- **Limited Availability**

While research into memristor technology is ongoing, commercial availability of memristors is still limited. This means that it may be difficult to obtain memristors in large quantities for use in complex digital circuits.

- **Cost**

Memristors can be more expensive than traditional transistors, which can increase the cost of digital circuits built with memristors. This cost disadvantage can be a significant barrier to the widespread adoption of memristor technology.

- **Sensitivity to Environment**

Memristors are sensitive to environmental factors such as temperature and humidity, which can affect their behaviour. This sensitivity can make memristors less suitable for some applications where environmental conditions are variable or difficult to control.

## **CHAPTER 3**

### **EXISTING METHODS**

Low power VLSI design has become a critical area of research due to the increasing demand for energy-efficient and portable devices. The conventional VLSI design techniques have been focused on achieving high performance, while power consumption has been considered as a secondary objective. However, with the emergence of battery-operated devices, low power design has become a crucial factor in determining the success of a product. The low power design techniques aim to reduce the power consumed by the system while maintaining its performance and functionality. It is crucial in the development of energy-efficient and long-lasting digital systems that are widely used in various applications, including smartphones, laptops, IoT devices, and wearable devices. The reduction in power consumption not only leads to longer battery life but also reduces the system's thermal dissipation, which can be beneficial in applications where thermal management is critical. Therefore, low power VLSI design has become an essential aspect of modern digital systems, and its importance is likely to increase further in the future with the growing demand for energy-efficient and sustainable technologies.

Power dissipation directly affects the performance, reliability, and overall functionality of electronic devices. With the increasing demand for portable and battery-powered devices, the power dissipation of VLSI circuits has become a major concern. Excessive power dissipation can lead to thermal issues and reduce the lifespan of the device. Additionally, power consumption also affects the cost of the device, as a higher power requirement results in the need for larger batteries or power supplies. Therefore, it is essential for VLSI designers to focus on minimizing power dissipation in their designs to ensure the efficient and effective operation of electronic devices. Power dissipation is a critical factor in VLSI (Very Large Scale Integration) design, and is closely linked to the choice of logic family used in a given application. Different logic families have varying power dissipation characteristics, and the amount of power consumed by a circuit is directly proportional to its performance and speed. For example, CMOS (Complementary Metal-Oxide-Semiconductor) logic is known for its low power consumption and high noise immunity, making it a popular choice for low-power digital circuits.

In contrast, ECL (Emitter-Coupled Logic) logic is used in high-speed applications but has high power consumption due to its non-linear characteristics. Similarly, TTL (Transistor-Transistor Logic) logic dissipates more power than CMOS, but is still used in certain applications due to its relatively fast switching speeds. Power dissipation can also be reduced by using advanced design techniques such as voltage scaling, dynamic voltage and frequency scaling, and clock gating. Overall, selecting the appropriate logic family is critical in minimizing power dissipation and ensuring efficient operation of VLSI circuits.

Logic families are a fundamental aspect of VLSI (Very Large Scale Integration) design, and refer to the different ways in which logic gates and circuits are constructed using electronic components such as transistors and diodes. There are a wide variety of logic families available, each with its own unique characteristics and performance parameters, that are chosen based on the specific requirements of a given application. Some of the most commonly used logic families include CMOS, NMOS, PMOS, Pseudo NMOS. Each of these families has its own set of advantages and disadvantages, which are carefully considered when designing circuits for specific applications

### **3.1 CMOS**

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. Today’s computer memories, CPUs, and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs). Microprocessors are built out of transistors. In particular, they are constructed out of metal-oxide semiconductor transistors. There are two types of MOS transistors, Positive-MOS (PMOS) and Negative-MOS (NMOS). Every PMOS and NMOS comes equipped with three main components — the gate, the source and the drain.

- **NMOS**

NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

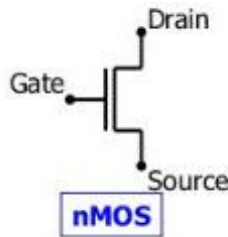


Fig. 3.1 NMOS transistor

- **PMOS**

P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

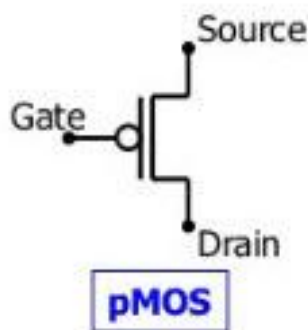


Fig. 3.2 PMOS transistor

In the IC design, the basic and most essential component is the transistor. So MOSFET is one kind of transistor used in many applications. The formation of this transistor can be done like a sandwich by including a semiconductor layer, generally a wafer, a slice from a single crystal of silicon; a layer of silicon dioxide & a metal layer. These layers allow the transistors to be formed within the semiconductor material. A good insulator like  $\text{SiO}_2$  has a thin layer with a hundred molecules thickness. The transistors which we use polycrystalline silicon (poly) instead of metal for their gate sections. The Polysilicon gate of FET can be replaced almost using metal gates in large scale ICs. Sometimes, both polysilicon & metal FET's are referred to as IGFET's which means insulated gate FETs, because the  $\text{SiO}_2$  below the gate is an insulator. The main advantage of CMOS over NMOS and BIPOLAR technology is the much smaller power dissipation. Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows integrating more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary Metal Oxide Semiconductor transistors consists of P-channel MOS (PMOS) and N-channel MOS (NMOS).

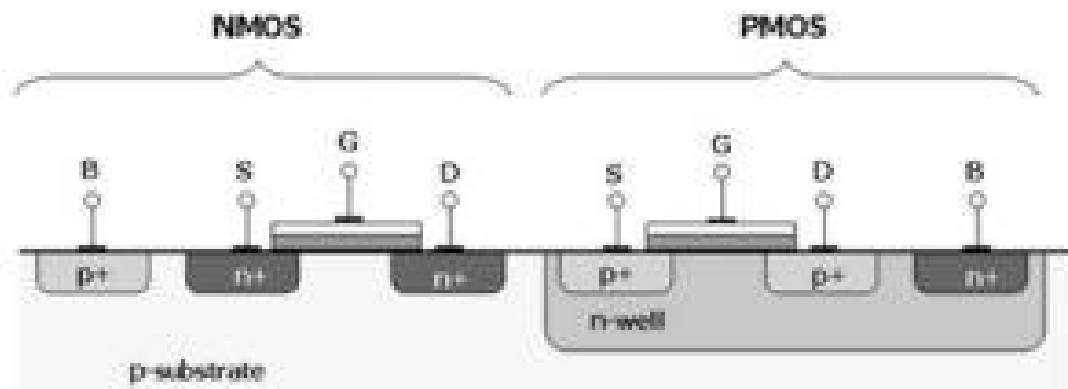


Fig. 3.3 CMOS well

### 3.1.1 CMOS Working Principle

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail ( $V_{ss}$  or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named  $V_{dd}$ ).

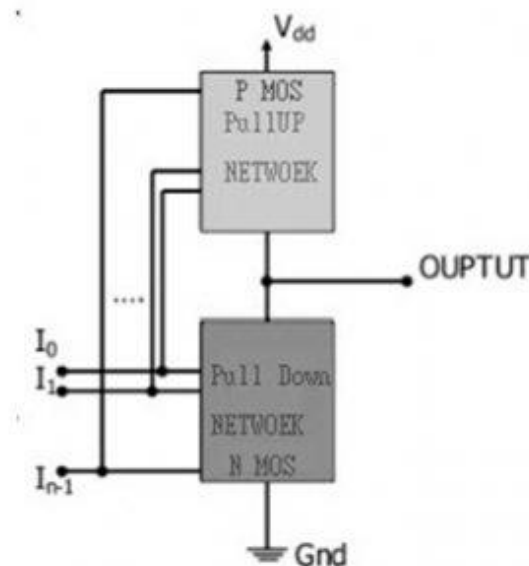


Fig. 3.4 CMOS using pull up & pull down

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure. CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed). Technology like CMOS is used in different chips like microcontrollers, microprocessors, SRAM (static RAM) & other digital logic circuits. This technology is used in a wide range of analog circuits which includes data converters, image sensors & highly incorporated transceivers for several kinds of communication.

### 3.1.2 Cmos Logic Gates

- **CMOS NOT Gate**

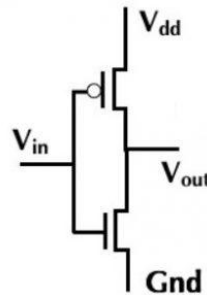


Fig. 3.5 CMOS inverter

The inverter circuit consists of PMOS and NMOS FET, where input A is the gate voltage for both transistors, and terminal Y is the output. When a high voltage is given at input A, the PMOS becomes an open circuit, and NMOS switched ON so the output is pulled down to Vss. Conversely, when a low-level voltage is applied to the inverter, the NMOS switched OFF and PMOS switched ON, pulling the circuit up to Vdd.

- **CMOS NAND Gate**

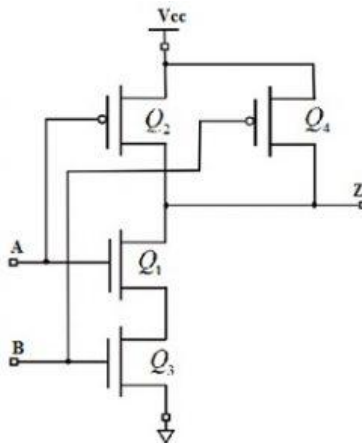


Fig. 3.6 Two input NAND gate

The 2-input Complementary MOS NAND gate comprises two series NMOS transistors between Y and Ground, and two parallel PMOS transistors between Y and VDD. If either input A or B is logic 0, at least one NMOS transistor will be OFF, and one PMOS transistor will be ON, creating a path from Y to VDD. This behavior results in a logical NAND function at the output.

- **CMOS NOR Gate**

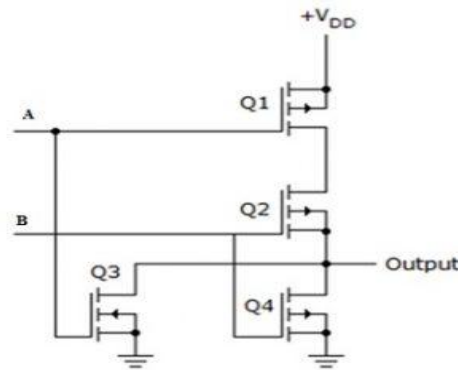


Fig. 3.7 Two input NOR gate

A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.

### 3.1.4 CMOS Characteristics

The most important characteristics of CMOS are low static power utilisation, huge noise immunity. When the single transistor from the pair of MOSFET transistor is switched OFF then the series combination uses significant power throughout switching among the two states like ON & OFF. As a result, these devices do not generate waste heat as compared with other types of logic circuits such as TTL or NMOS logic, which usually use some standing current and don't change their state.

### 3.1.5 CMOS Advantages And Disadvantages

#### Advantages

The main benefits of CMOS are good noise margin as well as less power consumption. This is due to no straight conducting lane from VDD to GND, fall times based on the conditions of input, then the transmission of the digital signal will become easy & low cost through CMOS chips. CMOS is used to explain the amount of memory on the motherboard of the computer that will store in the settings of BIOS. These settings mainly include the date, time, and settings of hardware. The outputs of CMOS drive actively in both ways.



**Advantages**

- Input impedance is high
- Fan out is high
- Stability of temperature
- Noise immunity is good
- Logic swing is large

**Disadvantages**

- Cost is more
- Packing density is low
- MOS chips should be secured from getting static charges
- CMOS uses more space
- CMOS has limited maximum operating speed.

**3.1.6 CMOS Applications**

Complementary MOS processes were widely implemented and have fundamentally replaced NMOS and bipolar processes for nearly all digital logic applications. CMOS technology has been used for the following digital IC designs. I.e. Computer memories, CPUs, Microprocessor designs, Flash memory chip designing, ASICs. Thus, the CMOS transistor is very famous because of electrical power efficiency. CMOS doesn't use electrical supply whenever, supply altering from one condition to another. Also, the complementary semiconductors work mutually to stop the o/p voltage. The outcome is a low-power design that provides less heat, due to this reason, these transistors have changed other earlier designs like CCDs within camera sensors & utilized in most of the current processors. The memory of the CMOS within a computer is a kind of non-volatile RAM that stores BIOS settings & the information of time and date. CMOS technology has several practical applications in home appliances, including smart home devices, digital displays, audio processing, power management, and timing and control circuits. CMOS circuits help to provide reliable and energy-efficient performance in these devices, making them more user-friendly and cost-effective. Overall, CMOS technology plays a critical role in the design and manufacture of modern home appliances.

## 3.2 PSEUDO-NMOS

Pseudo NMOS is a logic circuit that uses a PMOS transistor and an NMOS transistor in parallel to create a logic gate. It operates similarly to NMOS logic gates but with improved noise immunity and faster speed. However, it consumes more power and requires more space on the chip than standard NMOS circuits. Pseudo NMOS is still used in certain applications where its advantages outweigh its disadvantages. Pseudo NMOS (P-NMOS) is a type of digital logic circuit that is widely used in the design of integrated circuits. The basic idea behind P-NMOS is to use a P-channel MOSFET as a pull-up device and a resistor as a pull-down device to form a logic gate. The resistor is used to connect the output of the MOSFET to the ground, creating a voltage divider that provides the output voltage. The MOSFET is controlled by an input signal that drives the gate voltage high, allowing current to flow through the device and pulling the output voltage to a high state. When the input signal is low, the MOSFET turns off, and the output voltage is pulled low by the resistor. The P-NMOS logic family was widely used in the early days of digital electronics due to its simplicity and low power consumption. It was particularly well-suited for implementing circuits that required only a few logic gates and where power consumption was a critical factor.

### 3.2.1 Pseudo NMOS logic gates

As shown in all these figures, there is a block of NMOS FETs, which will contain one or more NMOS transistors, as required by the structure of the gate. However, there will be only one PMOS transistor in any pseudo-NMOS logic, and this will always be grounded. The p-NMOS circuit is a modification of NMOS circuits with DMOS loads. In p-NMOS circuits, we use a PMOS transistor, instead of the DMOS transistor, as its load. The advantages of using a PMOS load are:

- The circuit retains its basic CMOS structure. Hence, the chip area is minimal compared with the conventional CMOS structure.
- The circuit becomes compatible with CMOS devices.
- The channel resistance of the pseudo-NMOS devices is higher than that of the NMOS devices. Hence, power dissipation is lower for the pseudo devices.
- Pseudo-NMOS circuits are useful in applications where the output remains in logic-1 state most of the time.

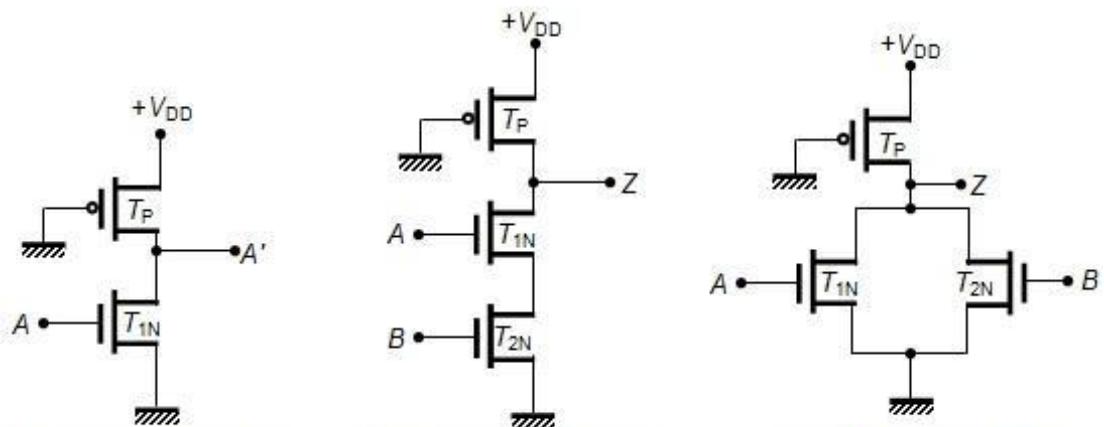


Fig. 3.8 Pseudo NMOS logic gates

However, the pseudo circuits have the disadvantage of possessing greater propagation delay than the NMOS devices. Despite its limitations, P-NMOS is still used in some specialized applications where low power consumption and simplicity are more important than speed. It is also used as a teaching tool to introduce students to the basic concepts of digital logic design. Understanding the operation of P-NMOS gates can provide valuable insights into the underlying principles of digital electronics and help students build a solid foundation for further study of more advanced digital circuits. P-NMOS uses only one PMOS device as a pull-up device. Therefore, the required number of transistors for an N input gate is an N+1 transistor.

### 3.2.2 Pseudo NMOS Characteristics

Pseudo NMOS is a type of logic circuit that is constructed using a PMOS transistor and an NMOS transistor in parallel. This configuration is used to create a logic gate that behaves like an NMOS transistor, while using a PMOS transistor as a pull-up resistor. The characteristics of a pseudo NMOS circuit are as follows

- **Logic Level**

Pseudo NMOS operates in the same way as NMOS logic gates, where a low input signal (0V) results in a high output signal (VDD) and a high input signal (VDD) results in a low output signal (0V).

- **Speed**

Pseudo NMOS circuits are faster than standard NMOS circuits because the PMOS helps to quickly charge the output to VDD when the NMOS transistor is off.

- **Noise Immunity**

Pseudo NMOS circuits have better noise immunity than standard NMOS circuits because the PMOS transistor helps to pull the output node up to VDD, reducing the effect of noise on the output.

- **Power Consumption**

Pseudo NMOS circuits consume more power than standard NMOS circuits because the PMOS transistor is always on, consuming a static current.

- **Size**

Pseudo NMOS circuits are larger in size compared to standard NMOS circuits because of the requirement of both a PMOS and an NMOS transistor. Overall, Pseudo NMOS is an improvement over standard NMOS circuits, with faster speed and better noise immunity. However, it is less power-efficient and requires more space on the chip.

### **3.2.3 Pseudo NMOS Advantages And Disadvantages**

Here are some advantages and disadvantages of Pseudo NMOS:

#### **Advantages**

- Pseudo NMOS circuits are simple to design and fabricate, and they require fewer transistors than other logic families, making them cost-effective.
- Pseudo NMOS gates operate at high speeds because the NMOS transistor turns on faster than the PMOS transistor turns off.
- Pseudo NMOS circuits consume less power than other NMOS-based logic families

#### **Disadvantages**

- P-NMOS circuits consume more power when the output is low because the pull-down network is made up of NMOS transistors that have a low resistance when turned on. This results in higher power dissipation and thermal issues.
- Pseudo NMOS circuits have poor noise margins because of the asymmetrical pull-up and pull-down network.
- Pseudo NMOS gates have limited fan-out because of the high output impedance of the pull-down network, which can limit the number of gates that can be connected to the output.

### 3.2.4 Pseudo NMOS Applications

While it has some limitations, it is still used in some specific applications

- **Arithmetic logic units**

Pseudo NMOS is used in ALUs due to its fast speed and simple design to control the selection of different logic functions.

- **Signal Processing**

Pseudo NMOS can be used in signal processing applications such as audio and video processing due to its fast speed and low power consumption.

- **Digital-to-Analog Converters**

Pseudo NMOS can be used in digital-to-analog converters (DACs) to convert digital signals into analog signals for use in audio equipment, instrumentation, and other applications.

- **Memory Arrays**

Pseudo NMOS can be used in memory arrays such as static random-access memory (SRAM) and read-only memory (ROM) due to its simple design and low power consumption.

- **Display drivers**

Pseudo NMOS is used in display drivers because of its simple and low-cost design, which is well suited for driving the high number of segments in a display.

- **Microcontrollers**

Pseudo NMOS circuits are used in microcontrollers, which are small, low-cost computers that are used in a variety of applications, such as embedded systems, automotive systems, and home appliances.

Pseudo NMOS technology has both advantages and limitations. However, its high speed and low power consumption, as well as its simple and low-cost design, make it a popular choice for several practical applications in electronic circuits, such as signal processing, sensor interfaces, digital-to-analog converters, memory arrays, power management, and more.

## **CHAPTER 4**

### **PROPOSED METHOD**

Memristor ratioed logic is a design approach that combines CMOS technology and memristors to create logic gates with several advantages over traditional CMOS designs. MRL enables easy fabrication of memristors on top of the CMOS polysilicon layer, which reduces the design's area and the number of transistors required. Moreover, MRL allows for reduced power consumption and faster operation compared to conventional designs. MRL uses memristors and resistors to implement logic functions. In MRL, memristors and resistors are connected in a way that implements logical operations, with the memristors acting as memory elements that retain the logic state of the circuit.

#### **4.1 INTRODUCTION TO MRL**

Memristor ratioed logic (MRL) is a new type of digital logic design that utilises memristors, a type of passive two-terminal electronic component with the ability to change their resistance based on the applied voltage. In MRL, memristors are used to implement digital logic functions, replacing conventional transistors used in conventional CMOS logic. MRL has the potential to overcome some of the limitations of CMOS logic, such as low energy efficiency and limited scaling, and has been proposed as a promising alternative for future computing systems. In MRL, a ratioed logic approach is used, where the output of the logic gate is proportional to the ratio of two resistances, rather than the absolute resistance value. This approach provides several advantages over traditional CMOS logic, including improved noise tolerance, reduced power consumption, and greater design flexibility. Additionally, MRL gates can be implemented using a smaller number of memristors compared to CMOS gates, leading to a reduction in area and complexity. MRL has been studied extensively in recent years, with several research groups demonstrating its potential in various applications, including arithmetic circuits, memory, and neuromorphic computing. However, there are still several challenges that need to be addressed before MRL can be commercialised, including variability and reliability issues associated with memristors, and the development of efficient fabrication techniques.

## 4.2 MRL CHARACTERISTICS

Memristor Ratioed Logic (MRL) is a design approach that combines CMOS technology with memristors to create logic gates with several distinct characteristics. Some of the key characteristics of MRL are

- **Reduced Power Consumption**

MRL requires fewer transistors than conventional CMOS designs, which results in lower power consumption. The incorporation of memristors in MRL also helps to reduce power consumption by enabling the design of circuits that operate at lower voltages.

- **Faster Operation**

MRL enables faster operation compared to conventional CMOS designs. The use of memristors in MRL allows for the creation of circuits with faster switching times, enabling faster overall circuit operation.

- **Reduced Area**

MRL requires less area than conventional CMOS designs due to the integration of memristors on top of the CMOS polysilicon layer. This integration reduces the number of transistors required, which in turn reduces the area required for the circuit.

- **Robustness**

MRL is more robust than conventional CMOS designs because it utilizes memristors, which are non-volatile and have high endurance. This means that MRL circuits can withstand harsh environmental conditions and can operate reliably over long periods of time.

- **Scalability**

MRL is highly scalable, which means that it can be used to design circuits for a wide range of applications, from simple logic gates to complex digital systems. This scalability is due to the use of memristors, which can be easily integrated into existing CMOS technology.

- **Fewer Transistors**

MRL requires fewer transistors than conventional CMOS designs, which leads to more efficient and cost-effective designs.

### 4.3 MRL AS LOGIC GATES

An interesting method for integrating memristive devices with standard CMOS logic is using memristive devices as computational elements, OR and AND. Since these functions are non-inverting logic gates, a complete logic structure can be achieved by adding a standard CMOS inverter. In this logic family, the logic is represented as a voltage, consistent with CMOS. The memristive devices are utilised solely for logic computation and not for storing a logical state. The computational result is independent of the initial state of the memristive devices, and the initial state only affects the computational time. Unlike other logic methods, the computational process is composed of only a single step.

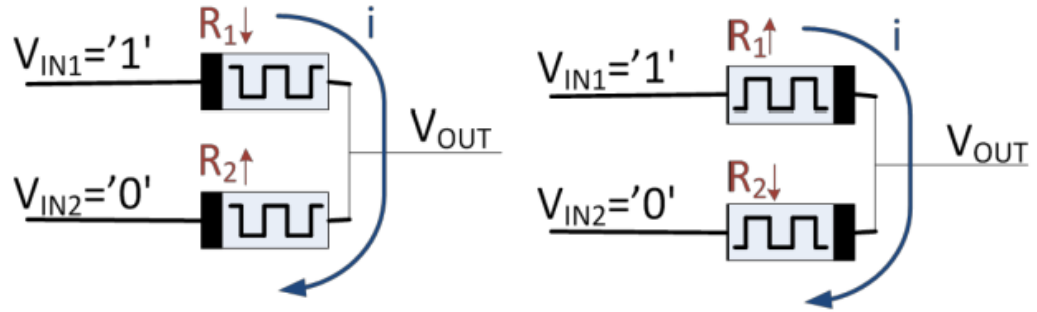


Fig. 4.1 Memristive OR gate & AND gate

An OR logic gate, and an AND logic gate when  $V_{IN1} = '1'$  and  $V_{IN2} = '0'$ . The current flows from  $V_{IN1}$  to  $V_{IN2}$  and the resistance of the memristive devices changes for the OR and AND logic gates

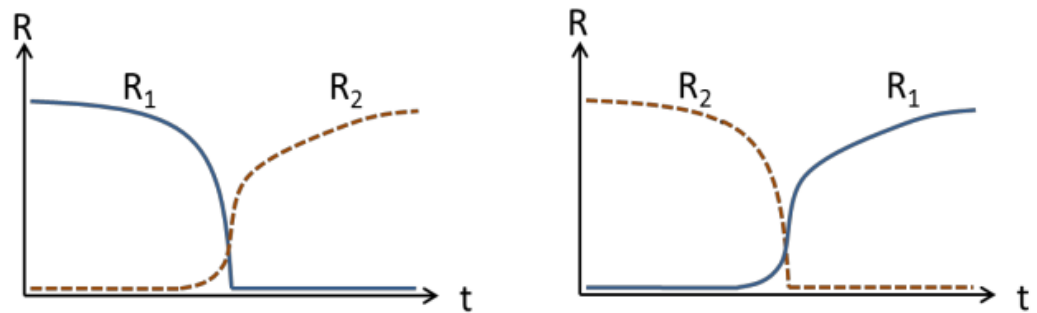


Fig. 4.2 The resistances of  $R_1$  and  $R_2$  of memristive OR logic & AND logic

Note that the initial resistance of both memristive devices has no effect on the result of the computation. The only effect of the initial resistance on the behaviour of the logic gate is the delay time of the execution



It is possible that the memristive devices do not fully switch and achieve the maximum and minimum resistance since the input voltages are not applied for a sufficiently long time or the input voltage is too low. In this case, it would be difficult to distinguish between the different output levels. The MRL family is inspired by Diode Logic and shares some characteristics, such as both logic families are non-inverting and non-restoring. The number of inputs for both MRL gates can be extended in a similar way as diode logic. To provide a complete logic family, an inverter is needed in addition to OR and AND logic gates. Furthermore, memristive devices are passive elements and therefore cannot amplify signals. The MRL OR and AND logic gates therefore lack signal restoration. A hybrid CMOS-memristive logic family called MRL (Memristor Ratioed Logic) is introduced. With the addition of CMOS inverters, this logic family's OR and AND logic gates, which are based on memristive components, are given a full logic structure and signal restoration.

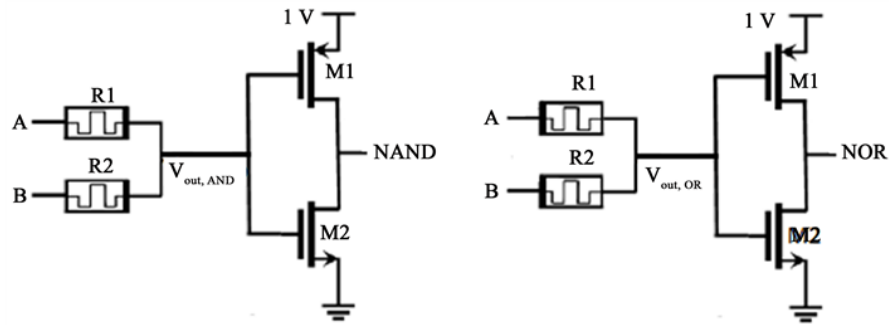


Fig 4.3 Schematic of an 2-input Hybrid CMOS NAND & NOR

The 2-input Hybrid CMOS NAND and NOR gates are digital logic gates used in integrated circuits. They both use a combination of NMOS and PMOS transistors in their circuit design to produce a logical output that is the complement of the logical AND or OR of two input signals. The NAND gate has two parallel PMOS transistors and two series NMOS transistors, while the NOR gate has two series PMOS transistors and two parallel NMOS transistors. Both gates play an essential role in digital circuits and are used in many electronic devices.

## 4.4 ENCODER USING DIFFERENT LOGICS

We are using LT - Spice for designing and simulation

### 4.4.1 CMOS

3 bit encoder is designed using 30 Transistors (15 PMOS + 15 NMOS)

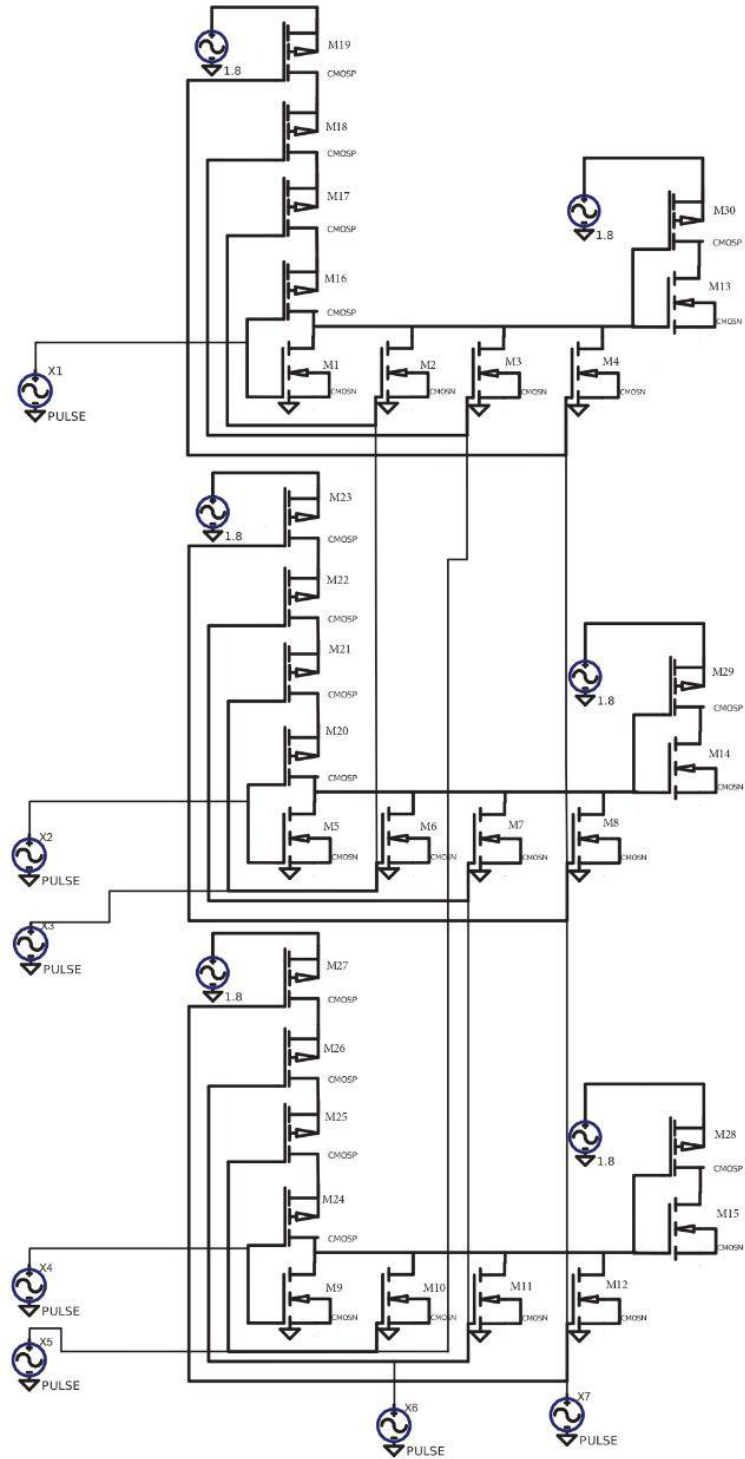


Fig 4.4 CMOS design for 3 bit encoder

#### 4.4.2 Pseudo NMOS

3 bit encoder is designed using 21 Transistors (6 PMOS + 15 NMOS)

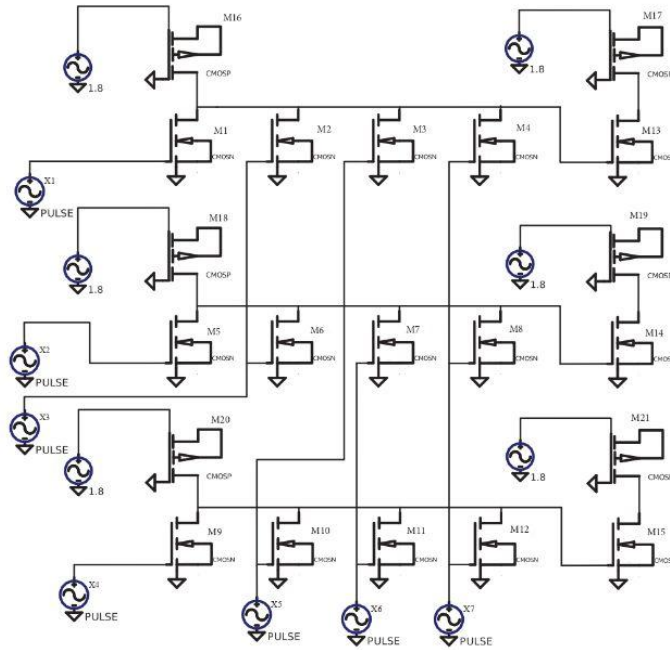


Fig 4.5 Pseudo NMOS design for 3 bit encoder

#### 4.4.3 Hybrid MRL

3 bit encoder is designed using 15 Transistors (0 PMOS + 15 NMOS) and 6 memristors

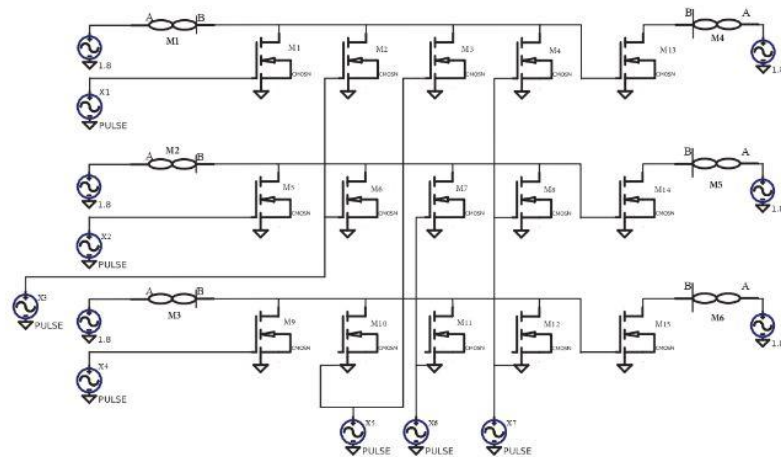


Fig 4.6 MRL design for 3 bit encoder

## **CHAPTER 5**

### **SIMULATION RESULTS**

Simulation results are an essential part of the design process in Very Large Scale Integration (VLSI) circuits. VLSI circuits are complex integrated circuits that can contain millions of transistors, and simulation is necessary to ensure the correct functionality of the circuit. Simulation results in VLSI can include data such as circuit response, power consumption, timing analysis, and other relevant parameters. These results are used to identify and resolve potential design issues before the circuit is physically fabricated.

Simulation in VLSI is done at various stages of the design process, including logic design, circuit design, and physical design. Simulation results are used to verify the functionality of the circuit at each stage and to ensure that it meets the design specifications. The accuracy and reliability of simulation results are critical in VLSI design as small design errors can result in significant performance issues or even complete circuit failure. Therefore, extensive simulation and verification are necessary to ensure the proper functioning of VLSI circuits.

#### **5.1 TOOLS REQUIRED**

##### **LT spice**

LTspice stands for Linear Technology Simulation Program with Integrated Circuit Emphasis. It was originally developed by Linear Technology Corporation, now part of Analog Devices, and is a widely used software tool for simulating analog electronic circuits. LTspice is a free software tool for simulating analog electronic circuits. It is widely used by engineers, designers, and hobbyists to design and test analog circuits such as amplifiers, filters, and power supplies. LTspice is developed by Linear Technology Corporation, and it includes a large library of components that can be used to build and simulate complex circuits. The software uses a simulation engine that can perform both transient and steady-state analysis of circuits, and it can generate output data such as waveforms, frequency response plots, and power dissipation estimates.

## **5.2 MODELS REQUIRED**

Memristor SPICE models are mathematical models used to simulate the behaviour of memristors in electronic circuits. Models are essential in the design and analysis of memristor-based circuits, which have the potential to revolutionise the field of electronics. Memristors are a type of passive electronic component that have the unique property of exhibiting a relationship between their resistance and the amount of charge that has passed through them. This means that the resistance of a memristor can be changed by applying an electrical voltage or current, and that it can retain its state even when the power is turned off. SPICE is a widely used software tool for simulating electronic circuits. It provides a way to model and simulate the behaviour of electronic components, such as resistors, capacitors, and transistors, and it can be used to design and analyse complex circuits. In recent years, there has been significant interest in the development of memristor-based circuits, particularly in the areas of memory and computing. However, the design and analysis of these circuits require accurate mathematical models that can capture the unique behaviour of memristors.

### **5.2.1 Joglekar Resistance Switch Memristor Model**

A research article was released by Biolek et al. in 2009, presenting an idealised model for a newly discovered memristor fabricated at HP labs. The model is commonly known by different names such as "The Ideal Memristor", "The nonlinear Dopant Drift" or "The Resistance Switch". For individuals who are new to simulating memristors in SPICE, this model may be the initial one they would attempt before moving on to more intricate and precise models. The discovery of the memristor by a research group from HewlettPackard labs and its potential use in ultradense memory cells and neural computing architecture. Since real samples of the memristor are difficult to obtain, a computer model is useful for analysing its behaviour and developing applications. The SPICE model of the memristor, which starts from the mathematical model of the memristor previously published by the research group, and demonstrates SPICE simulations based on the proposed model.

### 5.2.2 Model Overview

The model is described quite well in the above referenced paper, but lets review the most critical pieces needed to understand how SPICE implementation works. In this model, window function is

$$f(x)=1-(2x-1)^{2p}$$

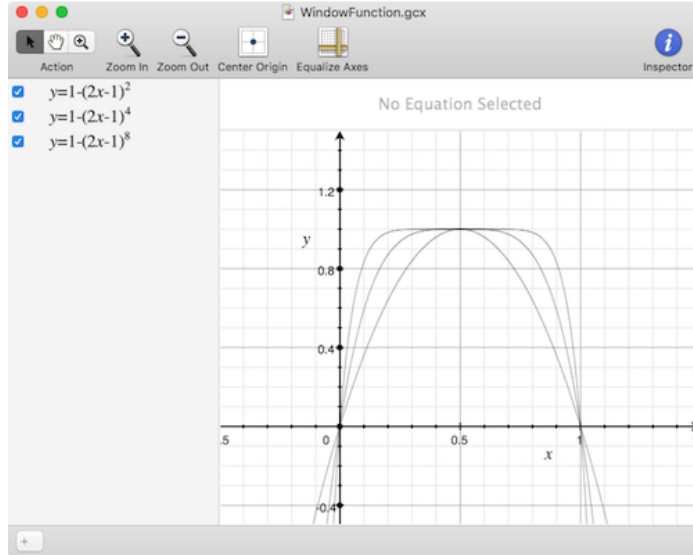


Fig. 5.1 Joglekar dopant drift window function

If you plot the integral of this function between 0 and 1, you get this:

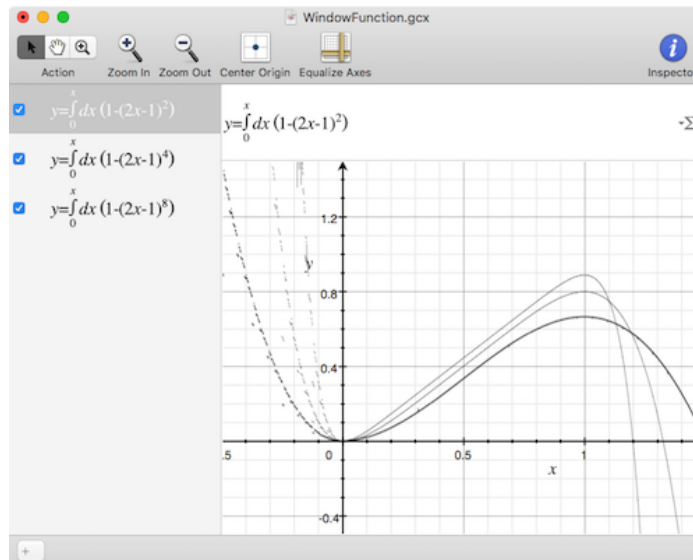


Fig. 5.2 Joglekar dopant drift window function integral

In this model the integral of the window function represents the state  $x$ , between 0 and 1, and is used to dynamically change a delta R value. delta R is  $R_{off} - R_{on}$ , and when in series with  $R_{off}$  (and given a minus sign) defines the memristor resistance.

### 5.2.3 Memristor subcircuit

```
*****
* HP Memristor SPICE Model for Transient Analysis only
*****
* Ron, Roff - Resistance in ON / OFF States, Rinit - Resistance at T=0
* D - Width of the thin film, uv - Migration coefficient
* p - Parameter of the WINDOW-function for modelling nonlinear boundary
conditions
* x - W/D Ratio, W is the actual width of the doped area (from 0 to D)
*****
.SUBCKT memristor plus minus PARAMS:
+ Ron=1 Roff=25M Rinit=20M D=10N uv=10F p=1
*****
* DIFFERENTIAL EQUATION MODELLING *
Gx 0 x value={I(Emem)*uv*Ron/D**2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1000000
*****
* RESISTIVE PORT OF THE MEMRISTOR *
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
*****
* FLUX COMPUTATION *
Eflux flux 0 value={SDT(V(plus,minus))}
*****
* CHARGE COMPUTATION *
Echarge charge 0 value={SDT(I(Emem))}
*****
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
* window function, according to Joglekar*
.func f(x,p)={1-(2*x-1)**(2*p)}
.ENDS memristor
*****
*****
```

A file named "memristor.sub" was created and saved in the directory ".../LTSpice/lib/sub". The provided code was then entered into the file in order to utilise the Joglekar Resistance Switch Memristor Model subcircuit.

### Symbol code

Version 4

SymbolType BLOCK

LINE Normal 8 33 -4 33

LINE Normal 0 -48 0 -32

LINE Normal 0 48 0 33

CIRCLE Normal 4 33 -4 0

CIRCLE Normal 4 -32 -4 0

SYMATTR SpiceModel memristor

SYMATTR Prefix X

SYMATTR Description Parameterized Memristor

SYMATTR ModelFile memristor.sub

PIN 0 -48 RIGHT 8

PINATTR PinName A

PINATTR SpiceOrder 1

PIN 0 48 RIGHT 8

PINATTR PinName B

PINATTR SpiceOrder 2

To define a graphical symbol for the memristor in LTSpice, the user should create a file named "memristor.asy" and save it in the directory ".../LTSpice/lib/sym". By defining both the subcircuit and graphical symbol, the memristor model can be easily and intuitively incorporated into LTSpice circuits

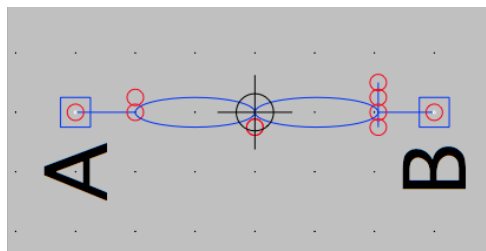


Fig. 5.3 Memristor symbol in LTSpice



## 5.3 RESULTS

The 3-bit encoder output has been achieved with less number of transistors and power has been reduced to lower power Memristor with  $R_{on} = 1\Omega$  and  $R_{off}$  as  $25M\Omega$  with initial resistance  $R_{init} = 20M\Omega$ . The memristor circuit element has been modelled using Verilog-AMS, transition analysis done with time period of .100ms, tweaking  $R_{off}$ ,  $R_{on}$  &  $R_{init}$  values can help in achieving lower power consumption in digital circuits like encoders. A comparison has been done between CMOS, P-NMOS and MRL logics by taking following parameters as input for pulse inputs with a delay of 12ms

Table 5.1 Periodic Signal Values

Vinitial [V]	Von[V]	Tdelay [S]	Trise [S]	Tfall [s]	Ton [S]	TPeriod [s]	Ncycles
0	1.8	0	0	0	10ms	100ms	1

### 5.3.1 CMOS

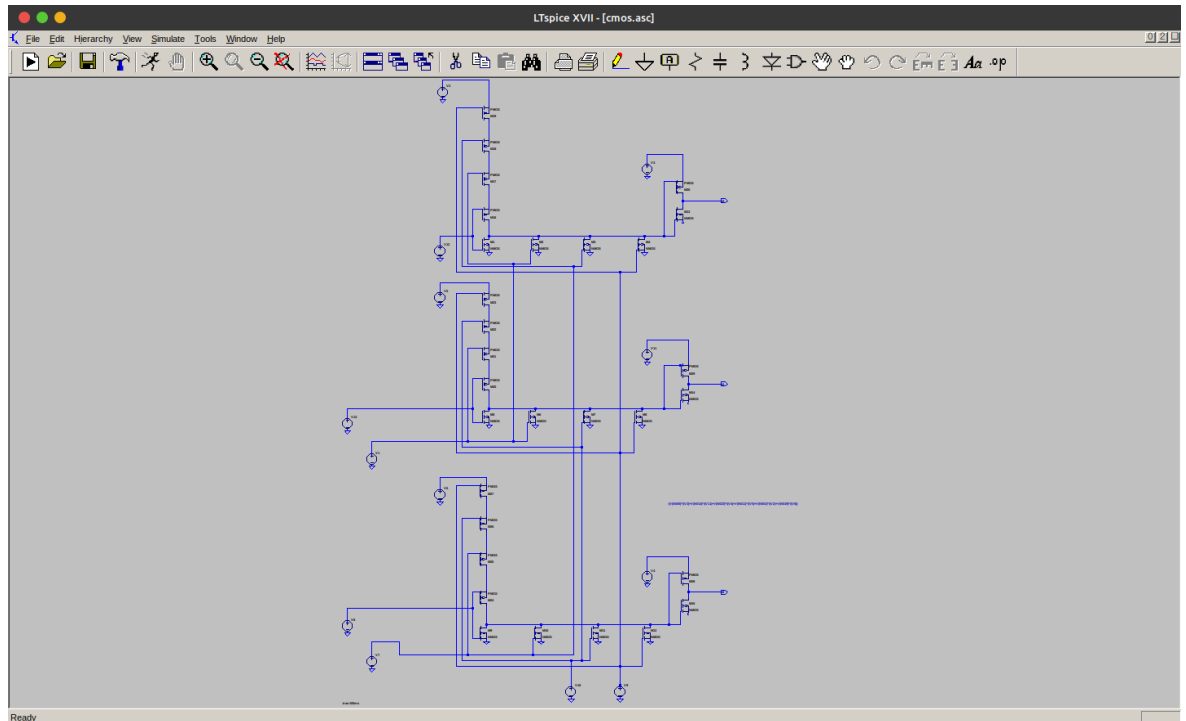
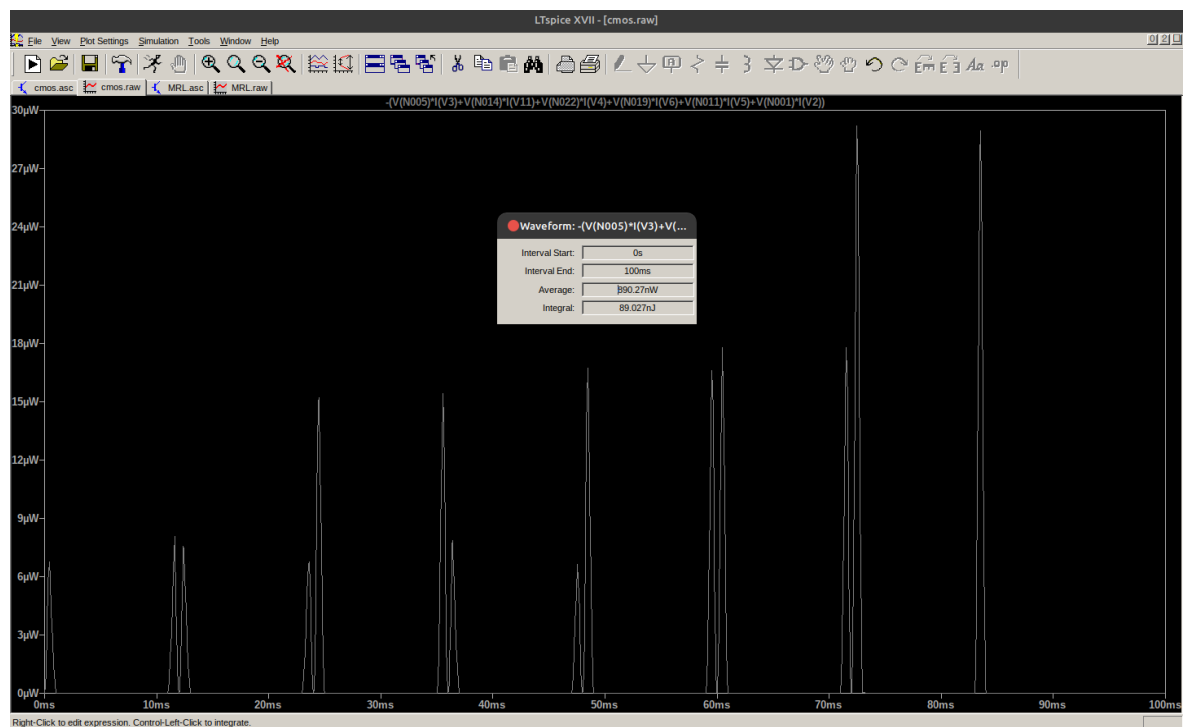
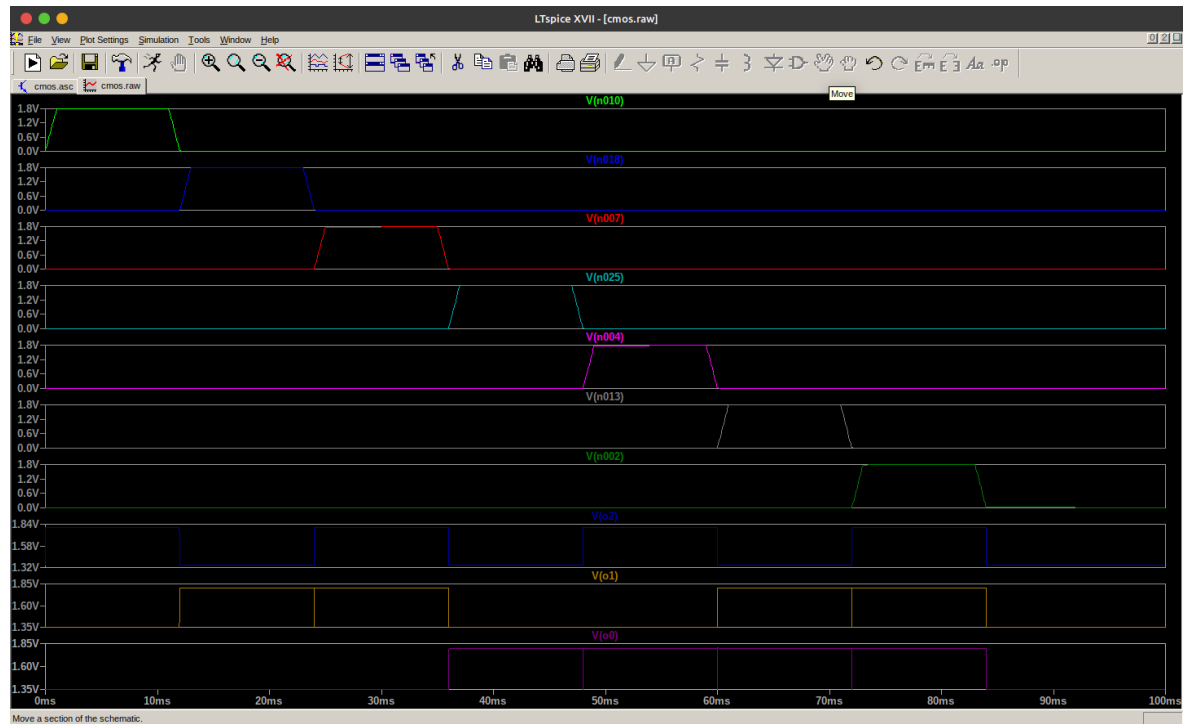


Fig. 5.4 CMOS design in LTspice



### 5.3.2 Pseudo NMOS

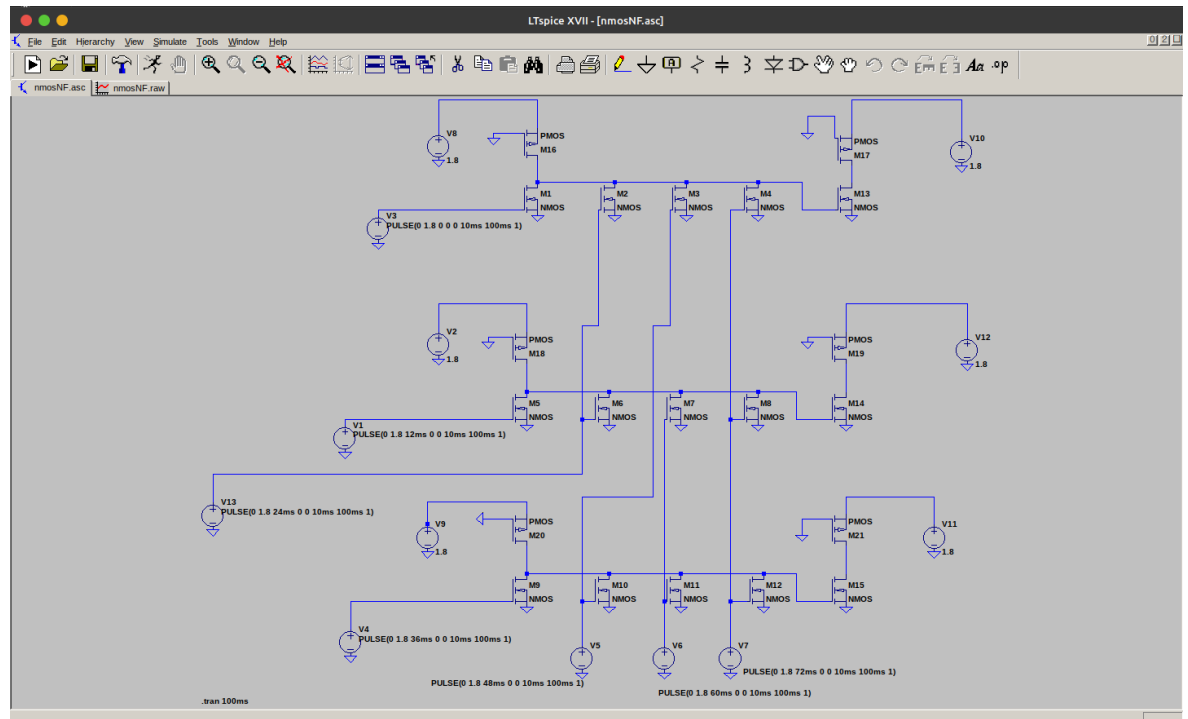


Fig. 5.7 Pseudo NMOS design in LTspice

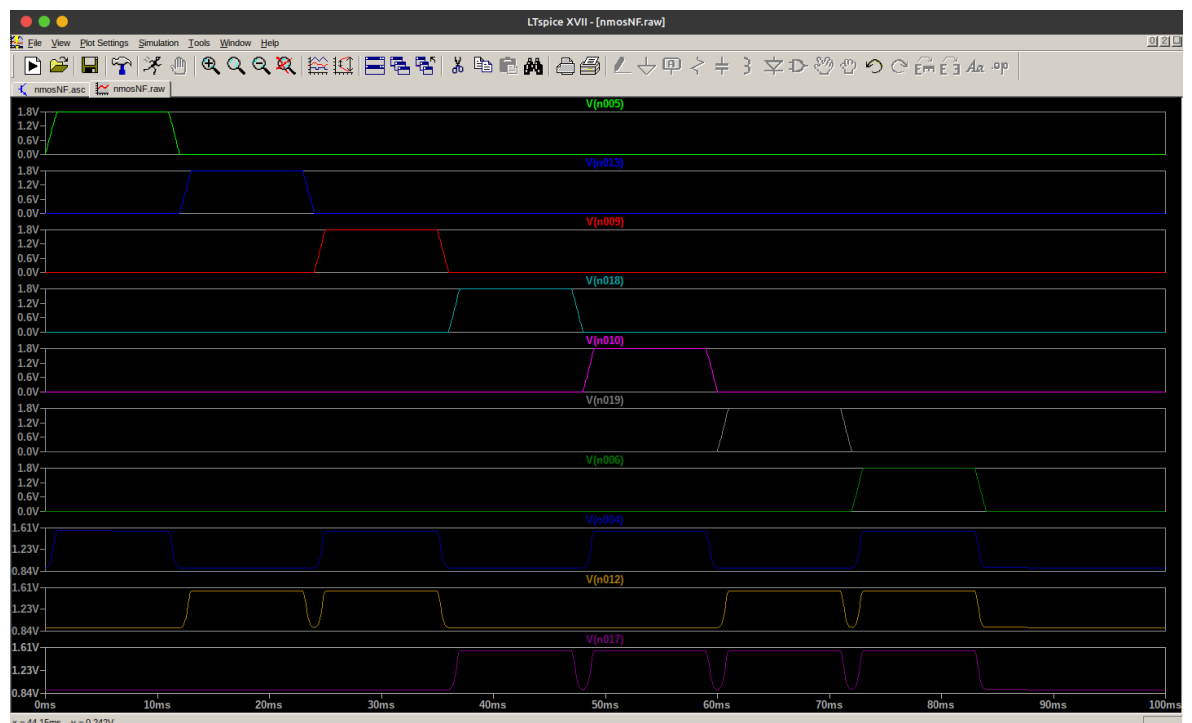


Fig. 5.8 Pseudo NMOS output in LTspice

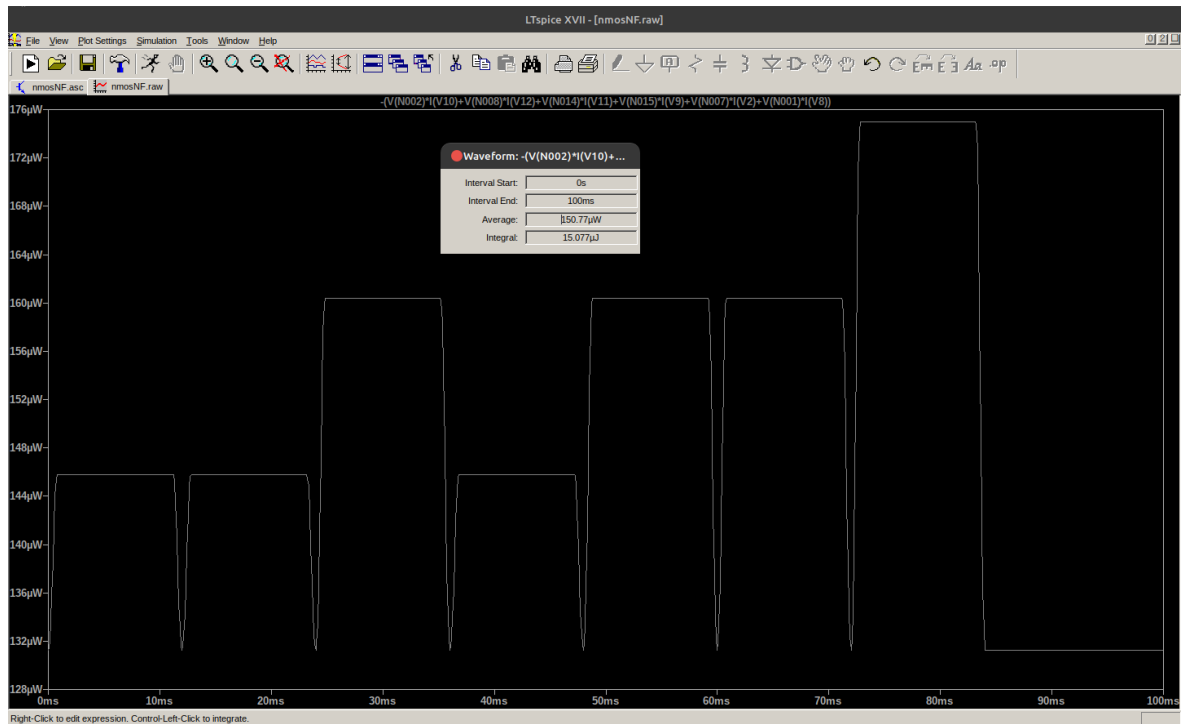


Fig. 5.9 Power analysis of encoder using Pseudo NMOS

### 5.3.3 Memristor Based Logic

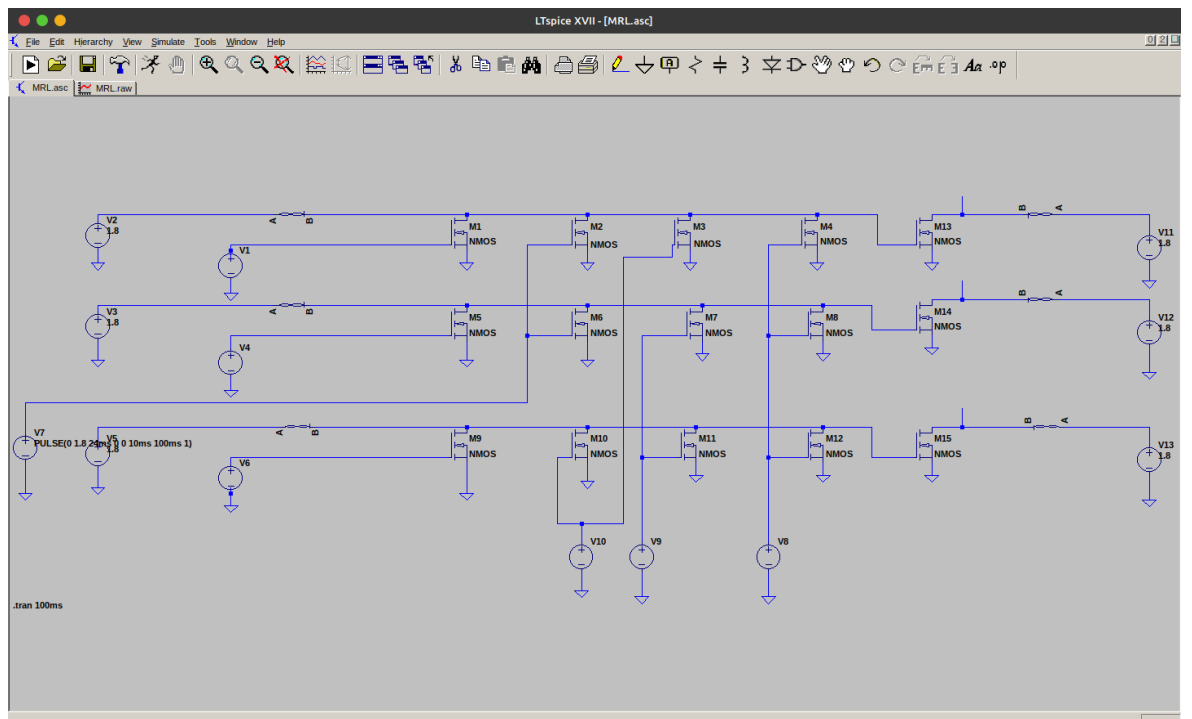


Fig. 5.10 MRL design in LTspice

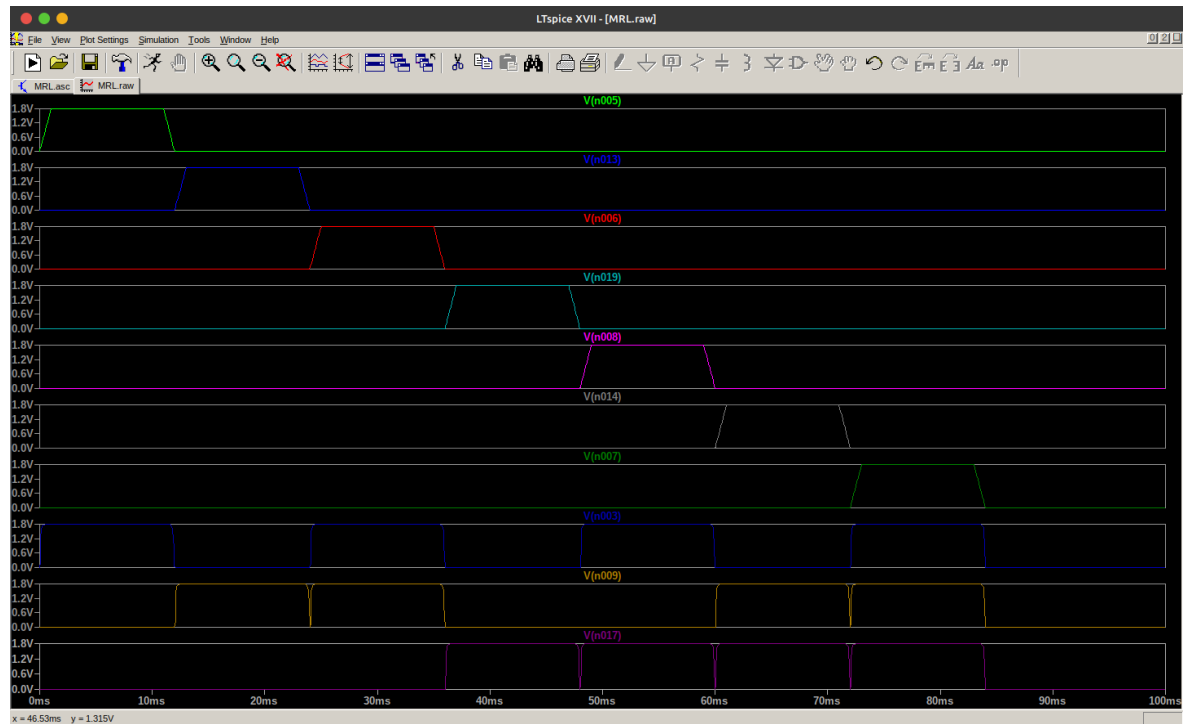


Fig. 5.11 MRL output in LTspice

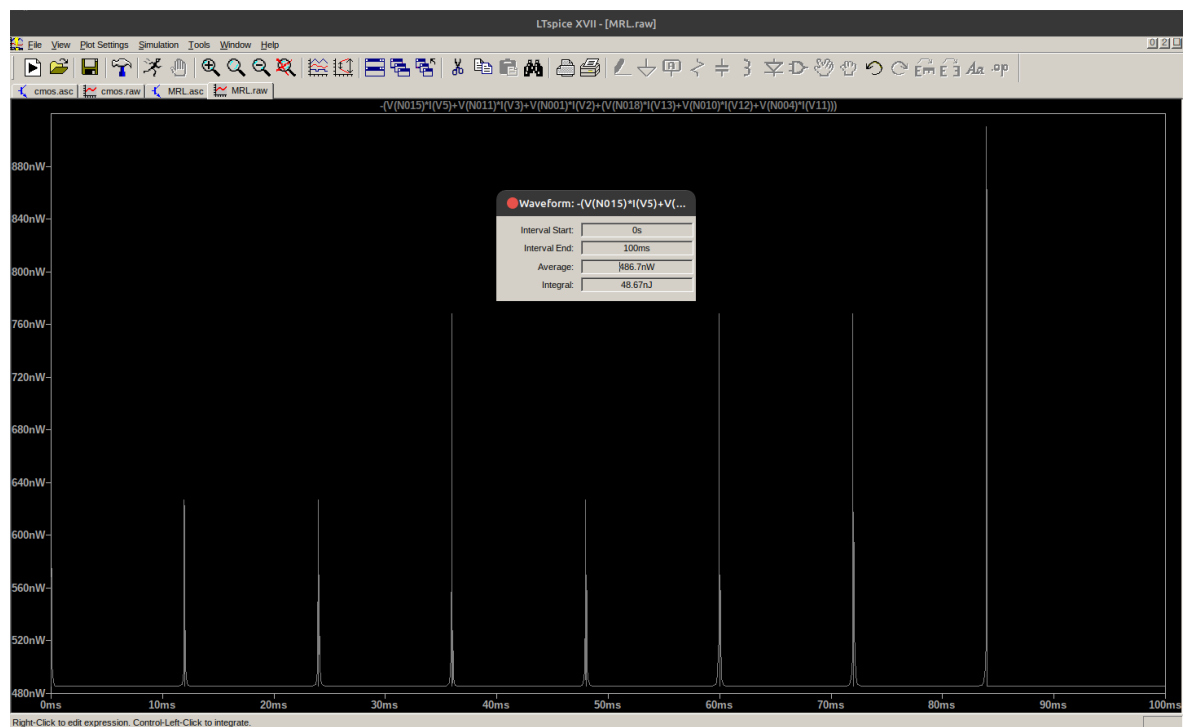


Fig. 5.12 Power analysis of encoder using MRL

#### 5.4 Comparison Of CMOS, PNMOS & MRL

Table 5.2 Comparison Of CMOS, PNMOS & MRL

Logic used for designing	Number of transistors used	Average Power Dissipated
CMOS	30 Transistors (15 NMOS + 15 PMOS)	890.27 nW
Pseudo NMOS	21 Transistors (15 NMOS + 6 PMOS)	150.77 $\mu$ W
MRL	15 Transistors (15 NMOS + 0 PMOS)	486.7 nW

Tweaking the value of memristor has been shown to help in achieving lower power dissipation in digital circuits. Memristors are a promising technology that can be used to replace traditional transistors in logic gates, memory devices, and other digital circuits. By adjusting the resistance of memristors, it is possible to optimise the power consumption of digital circuits, leading to improved energy efficiency. The window function used is Joglekar window. The encoder output has been achieved with a Memristor with  $R_{on}=1\Omega$  and  $R_{off}$  as  $25M\Omega$  with initial resistance  $R_{init}=20M\Omega$ . The circuit element has been modelled using Verilog-AMS. The memristor symbol has been created on LT spice can be seen in Fig. 5.3. The 3-bit encoder output has also been verified on CMOS and pseudo NMOS logic respectively. The power dissipated in the pseudo NMOS logic and the average power during the analysis is found to be 150.77  $\mu$ W. The power dissipated in the conventional CMOS logic and the average power during the analysis is found to be 890.27 nW. The Power dissipated in MRL design, the average power during the analysis was found to be 486.7 nW which is lower than power dissipated in conventional CMOS and pseudo NMOS based design. It can be depicted that there is a 45.33% decrease of power dissipated when compared to CMOS logic circuit design. The power dissipated is very low for the MRL when compared to pseudo NMOS based circuit design. As it is known that the area occupied by a Memristor based design is lesser than CMOS it can be depicted that this design is efficient with respect to the area consumed.

## **CHAPTER 6**

### **CONCLUSIONS AND FUTURE SCOPE**

In summary, the use of memristor-based logic design in encoder design is a promising approach to achieving energy-efficient and compact circuit designs. This technique has the potential to overcome some of the limitations of traditional CMOS technology, making it a more efficient way of designing digital circuits.

#### **6.1 Conclusions**

The utilisation of memristor-based logic design in encoder design has been found to be more effective in terms of power and area compared to traditional CMOS logic and Pseudo NMOS logic. Despite the persistent trade-off between power, area, and speed in circuit design, the memristor-based logic design technique has been observed to require fewer transistors, making it a more efficient approach to digital circuit design.

#### **6.2 Future scope**

Memristor-based logic design is a rapidly developing field, and there are several future scope areas where this technology could have significant impacts. Some of the potential future scopes for memristor-based logic design are:

- **Neuromorphic computing**

Memristor-based logic design has the potential to revolutionise the field of neuromorphic computing, which seeks to develop computing systems that mimic the structure and function of the human brain. Memristors can be used to design neural networks that are more energy-efficient and compact than traditional CMOS-based designs.

- **Non-volatile memory**

Memristors can be used to develop non-volatile memory systems that can retain data even when power is turned off. This can lead to the development of more efficient and reliable storage systems for data centres, mobile devices, and other applications.

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