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Low Power 3-Bit Encoder Design using Memristor

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***Abstract*—The design of digital logic gates using a memristor gives an alternative to the present IC design. This will be one among the upcoming Computing Architecture. The manufacturing of MRL gates is simple because memristor can be designed on top of the polysilicon gate of NMOS transistor. There will be an increase in density of transistors on a chip. The Proposed 3-bit Encoder design using MRL dissipates low Power as compared with CMOS design. This device is used to model different combinational logic circuits and this paper mainly aims to design and analysis of a 3-bit encoder with different logics using LT spice.**

***Index Terms*—Memristor,Encoder,Logic circuits.**

I. Introduction

The number of transistors per unit area of semiconductors has been rapidly expanding in recent decades, approximately doubling every two years, according to Moore's law. The constraints of transistors in physical materials, energy consumption, and economy, however, are challenging the aspect of area of semiconductors. To keep Moore's law alive, many alternatives have been suggested, one of which is to find a smaller component to substitute the standard transistor. The need to develop new approaches for obtaining a smaller area and more efficiency in the CMOS technique is still strong, and the efforts to do so are extremely helpful [1]. The main issue occurs when the size of CMOS cells shrinks owing to the major influence of leakage currents. The static power dissipation is increased by these leakage currents. Furthermore, because of the high error rates, the manufacture of such cells becomes difficult. All of these issues may be solved and considerably minimised by employing a passive device known as a "Memristor. " In 1971, Professor Chua proposed the notion of a Memristor, and in 2008, HP Lab realized the first nanoscale Memristor. Memristors have been proposed for usage in a variety of devices which inludes FPGA,amplifiers [2]. Many memory devices which are to be used in crossbars can be analysed using Memristors. It also increases the ease of manufacturing and area concerns [3]. Out of the logic circuits in Memristor, Memristor-aided Logic (MAGIC) and Material Implication (IMPLY) Memristor Logics are not suitable due to their inconsistency in multiple fan-outs and complexity. Memory, neuromorphic systems, and analog circuits are just a few of the uses for Memristors. Logic, which uses Memristors as building blocks for logic gates, is an intriguing application of Memristors. When using Memristors in a digital setting, a high memristance is deemed logic 0, whereas a low memristance is considered logic 1 [3]. Encoder is a circuit which is widely used in digital circuits for the process of encoding the signal and increase the ease of selection in the digital logic circuits. There are many logics that can be applied for designing a logic circuit using Memristor. This paper uses Memristor ratioed logic to implement the encoder design. This paper is focused on designing and analyzing the Memristor based encoder in power aspects to compare with the existing CMOS and Pseudo NMOS circuit logics.

II. Working of Memristor

A Memristor is a non-volatile and passive element which has two terminals. It is treated to be the fourth fundamental element that relates magnetic flux and charge. Fig. 1 shows the circuit representation of the Memristor symbol. The equation

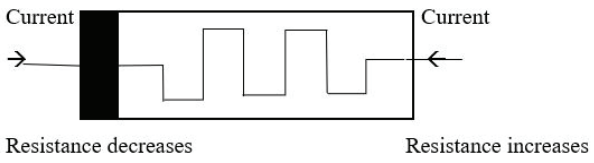

Fig. 1. Memristor model.

$M = d\phi/dq$ gives the realtion between charge and flux where memristance M(ohm), charge q(coulomb), magnetic flux ϕ (Volt-second)

Memristor is designed in a way that in between two platinum metal layers, pure(undoped) titanium dioxide (TiO_2) acts as a dielectric. On top of the dielectric, a doped titanium dioxide (TiO_{2-x}) acts as a semiconductor. The current through the memristor makes the resistance of the device to vary [4]. R_{on} is the low resistance when the width of the doped region is higher than the undoped region width of TiO_2. R_{off} is high resistance, where the width of the undoped region is higher than the width of the doped region. The black thick line gives the polarity of a Memristor [5]. When current flows towards the black line the resistance decreases, the minimum resistance offered by the Memristor is called ON resistance (R_{on}). If the current flows away from the black line the resistance increases,

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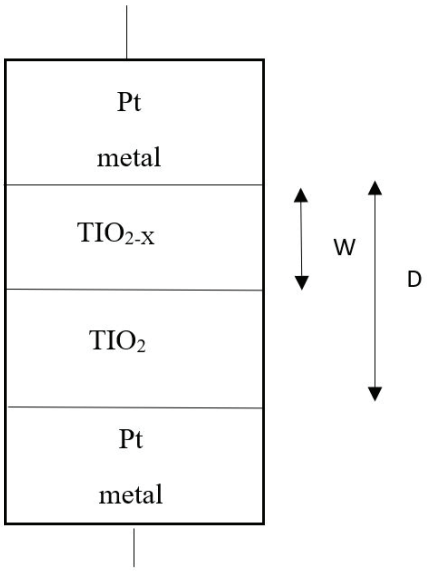

Fig. 2. Memristor schematic.

the maximum resistance offered by the Memristor is called OFF resistance (R_{off}). Typically $\frac{R_{off}}{R_{on}} \geq 1000$. The variable resistance of the Memristor equation is given as,

$$R(w) = R_{on}\left(\frac{w}{D}\right) + R_{off}\left(1 - \frac{w}{D}\right) \quad (1)$$

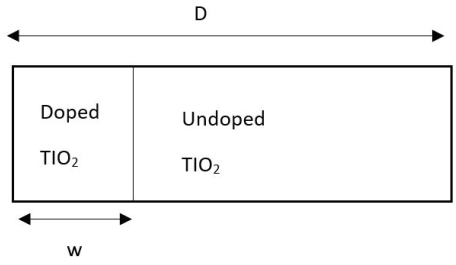

Fig. 3. Simple representation of a Memristor.

In the Fig. 3 w is the width of the doped TiO_2, D is the total width of the TiO_2. Memristor undoped width (w) gets overshot or undershot depending on the supply current. The window function, $F(x)$, controls the undoped width between the physical bounds of the Memristor [6].

$$x = w/D$$

Here x is the ratio of the width of the depletion region to the width of the total TiO_2.

$$\frac{dx}{dt} = F(x) \times K \times I(t)$$

K is constant, $I(t)$ is the current at time t and $F(x)$ is the window function

$$F(x) = 1 - \left(\frac{2w}{D-1}\right)^{2p}$$

p is a positive integer

A. Memristor ratioed logic

Designing logic gates by using CMOS technology and Memristor is called Memristor ratioed logic (MRL). This hybrid design gives the advantage over conventional CMOS design [7]. It is easy to fabricate Memristor on the top of the CMOS polysilicon layer, then it reduces the area of the design[7]. It also reduces the number of transistors [8]. In the Fig. 4, connecting two Memristors M1 and M2 in parallel, and output of that is given to the CMOS inverter it gives NAND gate logic. If we give A=0 and B=0 the potential across the terminals is zero. Then the out of CMOS inverter is one [9]. Similarly in Fig. 5 It can be observed that the NOR gate logic may be obtained by simply inverting the polarity terminals of the Memristors in the Fig. 4 architecture. This logic has a very low signal attenuation when compared to MAGIC and IMPLY logic [10] [11].

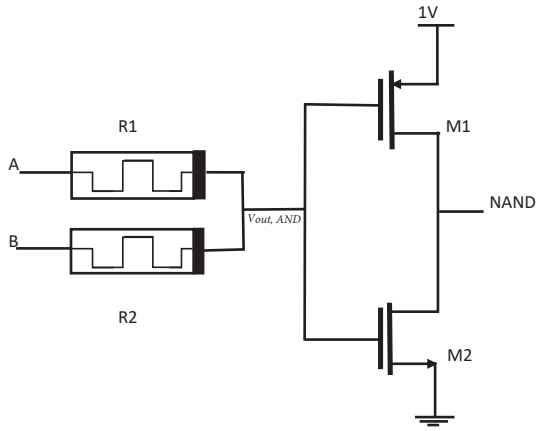

Fig. 4. NAND gate using Memristor.

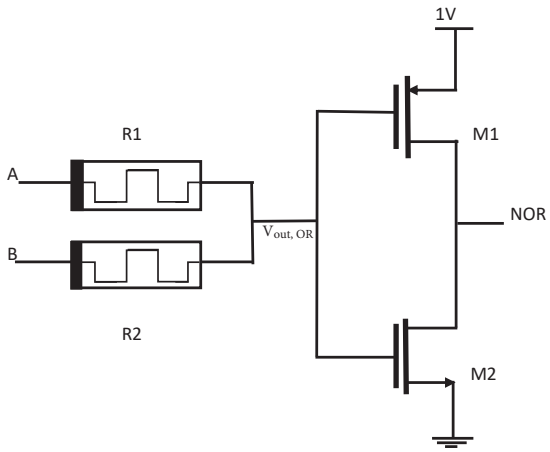

Fig. 5. NOR gate using Memristor.

III. Memristor Models

Research and development of Memristor is crucial in order to enhance the capabilities of present generation circuits.

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Memristors offer a lot of advantages such as Nonvolatility, with CMOS and higher density in designs. Nonvolatility of Memristors is specially motivating in memory design. With the help of Crossbar IMPLY logic gate implementation, in memory computations is being extensively researched, paving the way for a potential revolution in computer architecture, being termed as Beyond-Newman architecture. This has potential to get rid of the current bottleneck of the Von Newman architecture. Mainly three models

A. Linear Ion drift Model

$$R(w) = R_{on}\left(\frac{w}{D}\right) + R_{off}\left(1 - \frac{w}{D}\right)$$

This model assumes that the doped region width changes linearly with input current as

$$\frac{dw}{dt} = \frac{u_v R_{on}}{D i(t)}$$

It is easy to understand and implement, symmetric and uses window function

$$F(w) = 1 - \left(\frac{2w}{D-1}\right)^{2p}$$

B. Simmons Tunnel Barrier:

This Model uses the undoped region width (x) as state variable

$$\frac{dx}{dt} = C_{off} Sinh\left(\frac{i}{i_{off}}\right) \exp\left(\frac{x - a_{off}}{\frac{w_e - |i|}{\left(\frac{b-x}{w_c}\right)}}\right), i > 0$$

$$\frac{dx}{dt} = C_{on} Sinh\left(\frac{i}{i_{on}}\right) \exp\left(\frac{x - a_{on}}{\frac{w_e - |i|}{\left(\frac{b-x}{w_c}\right)}}\right), i < 0$$

This model is accurate and complexity is more, asymmetric switching timings.

C. ThrEshold Adaptive Model (TEAM):

TEAM model uses undoped region width as the state variable. Parameters can be adjusted to different models, it uses current thresholds. It provides sufficient [12] accuracy with reduced complexity, also uses window functions.

$$\frac{dx}{dt} = k_{off}\left(\frac{i(t)}{i_{off} - 1}\right)^{a_{off}} f_{off}(x),\ 0 < i_{off} < i$$

$$\frac{dx}{dt} = 0 \quad ,\ i_{on} < i < i_{off}$$

$$\frac{dx}{dt} = k_{on}\left(\frac{i(t)}{i_{on} - 1}\right)^{a_{on}} f_{on}(x),\ i < i_{on} < 0$$

Current is modelled as

$$V(t) = R_{on} i(t) \exp\left(\frac{y}{(x_{off} - x_{on})(x - x_{on})}\right)$$

$$\frac{R_{on}}{R_{off}} = e^{y}$$

D. Window Function:

There is a chance for the width of the Memristor to overshoot the physical dimension. So, we use window functions for simulation to restrict the width to be inbound with the physical dimensions of the Memristor. There are many models of window functions available such as Biolek,Joglekar etc. [10], [12]. This paper models encoder using the Ion Drift Model and Joglekar window function of Memristors.

IV. Encoder design and Operation

Information in digital logic circuits with specific meaning is encoded into corresponding binary bits. Encoder is a circuit which does this encoding function. The encoder's function is to encode when one of the input bits is of effective level, and the encoder's output changes in accordance with its input bits. The circuit has 'N' outputs and 'M' inputs and they are related by $M = 2^N$. The Fig. 6 and Table I shows the encoder diagram and its truth table respectively. From the Encoder truth table, the outputs and inputs are related by

$$Y_0 = X_1 + X_3 + X_5 + X_7$$

$$Y_1 = X_2 + X_3 + X_6 + X_7$$

$$Y_2 = X_4 + X_5 + X_6 + X_7$$

From these relations, logic circuit can be implemented using CMOS, Pseudo NMOS and MRL. In the Encoder circuits, X1-X7 are input bits and Y_2, Y_1, Y_0 are output bits. In Encoder circuit by using MRL, M_1, M_2, M_3, M_4 act as pull-down network and a Memristor acts as pull-up network. M_1, M_2, M_3, M_4 and Memristor constitute a 4-input NOR gate. X_1, X_3, X_5, X_7 are the input signals that pass through the NOR gate and the signal at the drain of M_1 is inverted signal of $(X_1 + X_3 + X_5 + X_7)$. M13 and Memristor constitute an inverter. The output of 4-input NOR gate is given as the input of inverter. The signal at the drain of M13 is $Y_0 = X_1 + X_3 + X_5 + X_7$. Similarly, a combination of 4-input NOR gate and an inverter has been used for each output of 3-bit encoder [13].

TABLE I
Encoder Truth Table

X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

V. Results and Discussion

The logic of Memristor that has been used is of Memristor Ratioed Logic(MRL). The window function used is Joglekar window. Fig. 7, Fig. 10 and Fig. 13 represent the circuits for 3-bit encoder sing MRL, CMOS and pseudo NMOS

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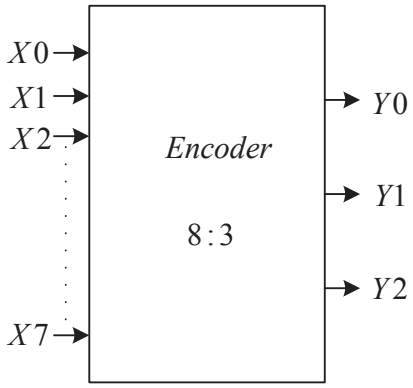

Fig. 6. 3-bit Encoder.

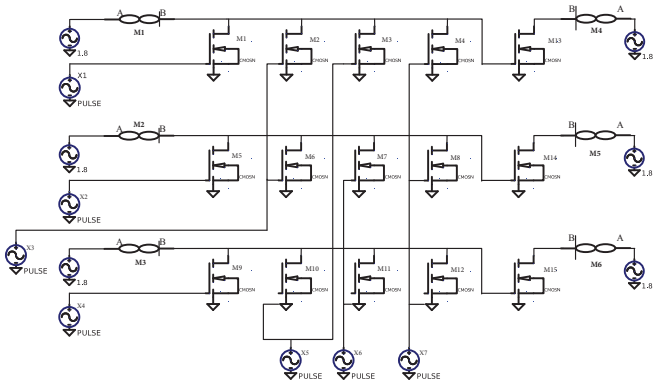

Fig. 7. Encoder using Memristor based logic.

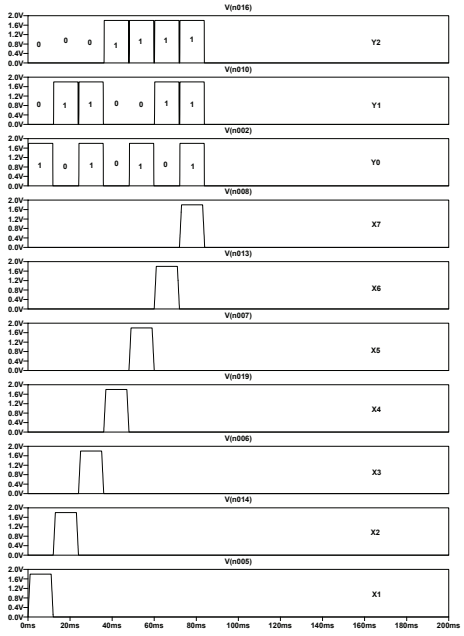

Fig. 8. Output of encoder using Memristor

TABLE II
POWER ANALYSIS

Logic used for designing	Average Power Dissipated
Pseudo NMOS	784.67uW
CMOS	1.2587uW
Memristor based design	1.2167uW

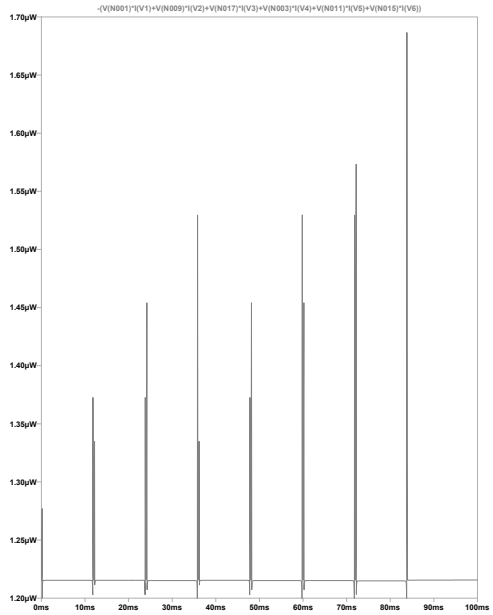

Fig. 9. Power analysis of encoder using Memristor

technologies. In Fig. 8the output can be depicted same as the table of encoder. It can be seen that the encoder output has been achieved with a Memristor with R_{on}=1Ωand R_{off} as 10MΩ with initial resistance R_{init}=8MΩ. The circuit element has been modeled using Verilog-AMS. The memristor symbol has been created on LT spice which can be seen in Fig. 7.The 3-bit encoder output has also been verified on CMOS and pseudo NMOS logic which can be seen in Fig. 11 and Fig. 14 respectively. The power dissipated in the pseudo NMOS logic can be seen in Fig. 15 and the average power during the analysis is found to be 784.67μW. The power dissipated in the conventional CMOS logic can be seen in Fig. 12 and the average power during the analysis is found to be 1.2587μW. The Power dissipated in MRL design can be seen in Fig. 9. The average power during the analysis was found to be 1.2167μW which is the lower than power dissipated in conventional CMOS and pseudo NMOS based design. It can be depicted that there is 3.3% decrease of power dissipated when compared to CMOS logic circuit design. The power dissipated is very low for the MRL when compared to pseudo NMOS based circuit design.

As, it is known that the area occupied by a Memristor based design is lesser than CMOS [11], [14], [15], it can be depicted that this design is efficient with respect to the area consumed. It can be seen that the number of transistors that are required for this design is the least when compared to the conventional

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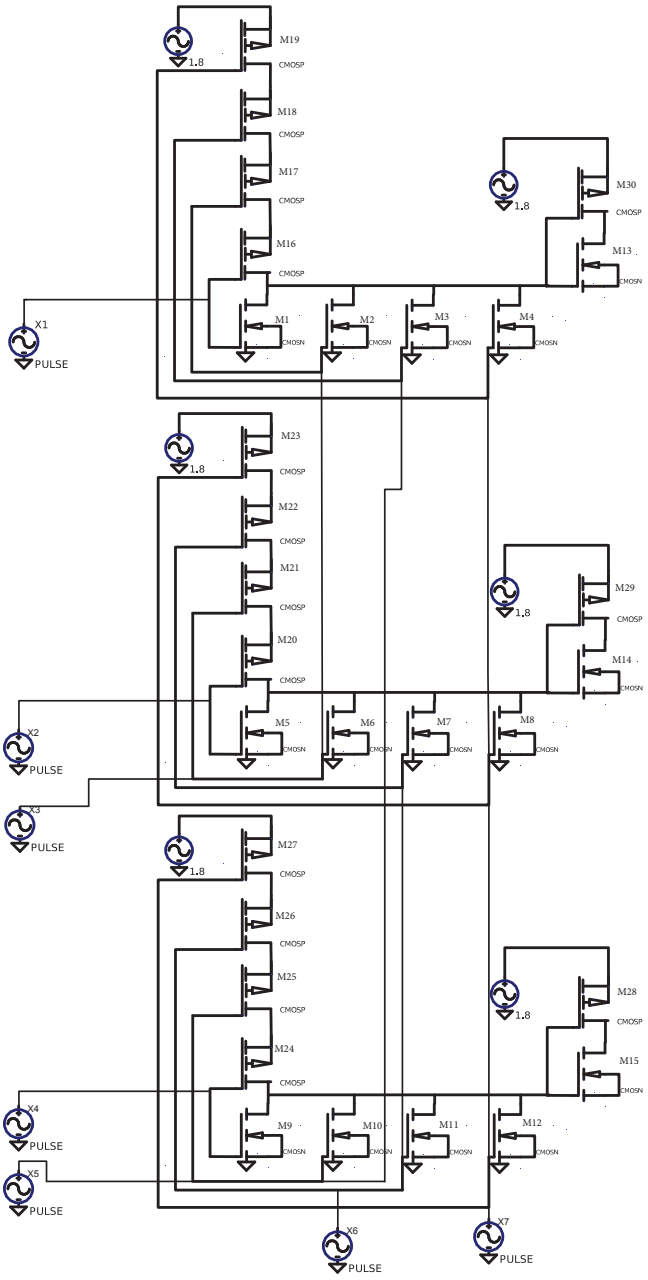

Fig. 10. Encoder Circuit using CMOS

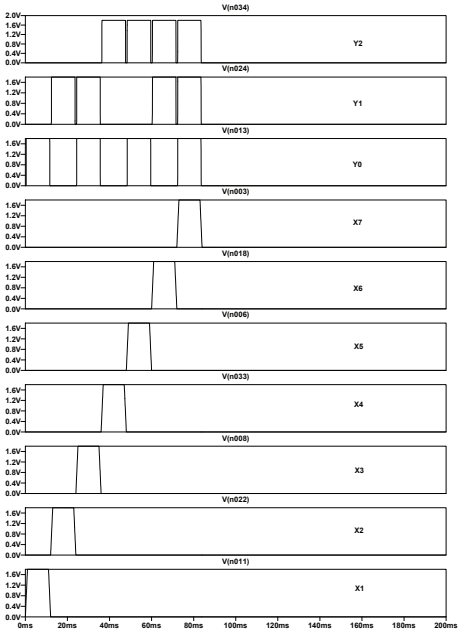

Fig. 11. Output of encoder using CMOS

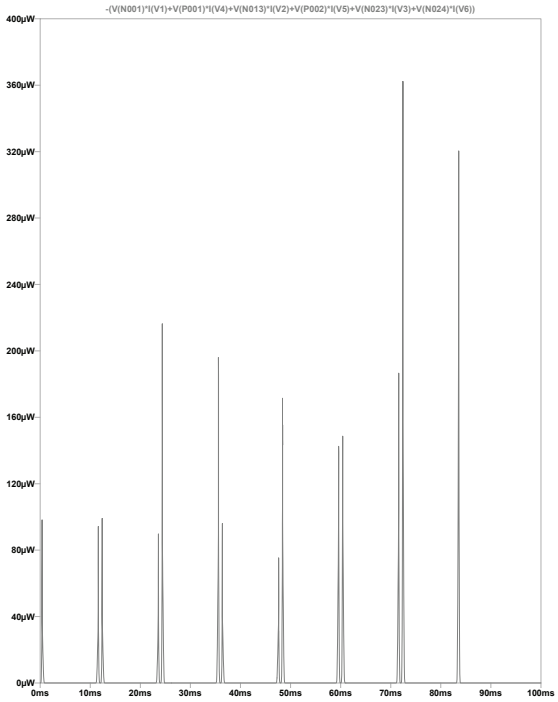

Fig. 12. Power analysis of encoder using CMOS

CMOS and Pseudo NMOS logic. By using CMOS technology, the encoder circuit has 30 transistors, of which 15 PMOS and 15 NMOS. By using Pseudo NMOS technology, the encoder circuit has 21 transistors, of which 5 PMOS and 15 NMOS. By using MRL technology, the encoder has 21 transistors, of which 6 Memristors and 15 NMOS.

VI. Conclusion

Design of encoder with Memristor based logic design is much efficient in the aspects of power and area when compared with conventional CMOS logic and Pseudo NMOS logic. The trade-off between the power, area and speed of a circuit is

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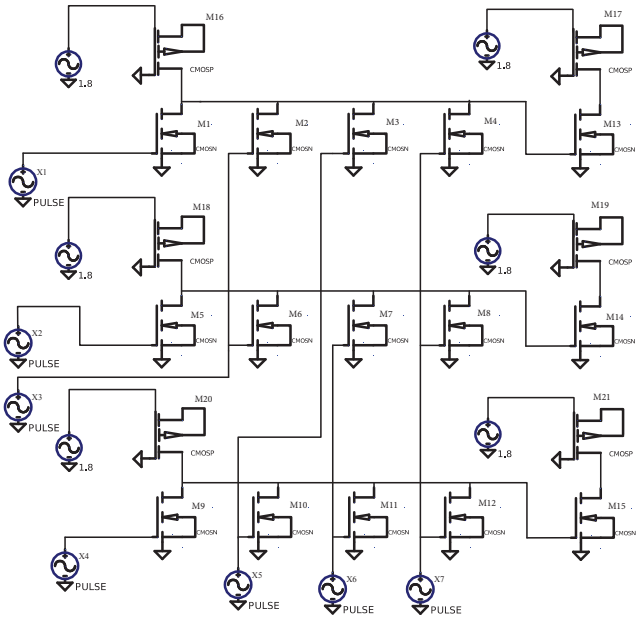

Fig. 13. Encoder Circuit using Pseudo NMOS

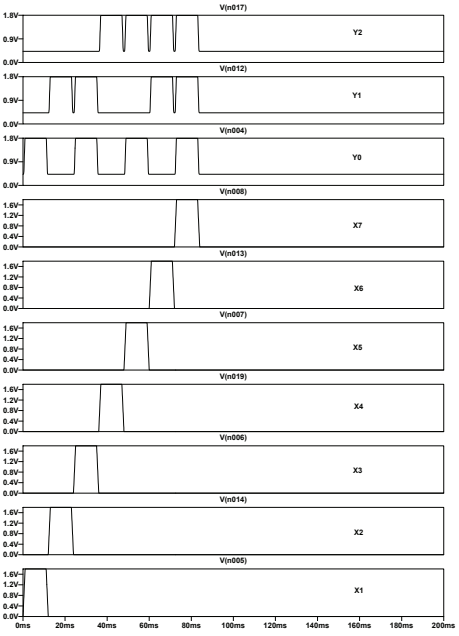

Fig. 14. Output of encoder using Pseudo NMOS

persistent. It can be concluded that this design technique gives lesser number of transistor count required and makes it more efficient way of designing a digital circuit.

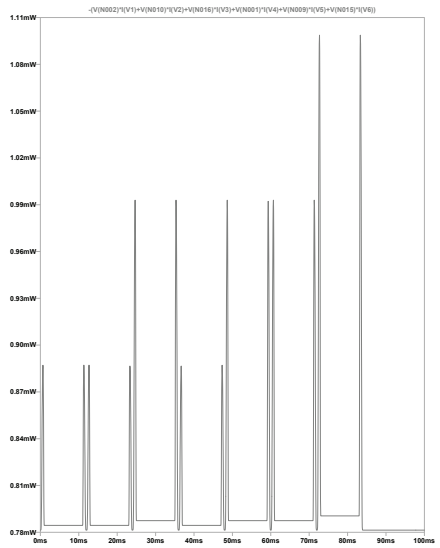

Fig. 15. Power analysis of encoder using Pseudo NMOS

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