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LAB INSTRUCTOR NAME : Sir Haris

COURSE ID : 67340

COURSE NAME : Digital Logic Design

PROJECT NAME:

- 24 Hour "Digital Clock" with Alarm

GROUP MEMBERS:

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PROJECT DESCRIPTION:

- The entire circuit is divided into two main parts
  i. A 24 Hour Digital Clock Circuit.
  ii. Preset time storage, comparator and relay driver circuit.

- 24-Hour Digital Clock and Timer Circuit" is a simple circuit with two different applications as per reflected through the name 24-hour clock and a timer. The Circuit of a versatile *24-Hour Digital Clock* and *Timer Circuit*.

PROJECT CIRCUIT DIAGRAM:

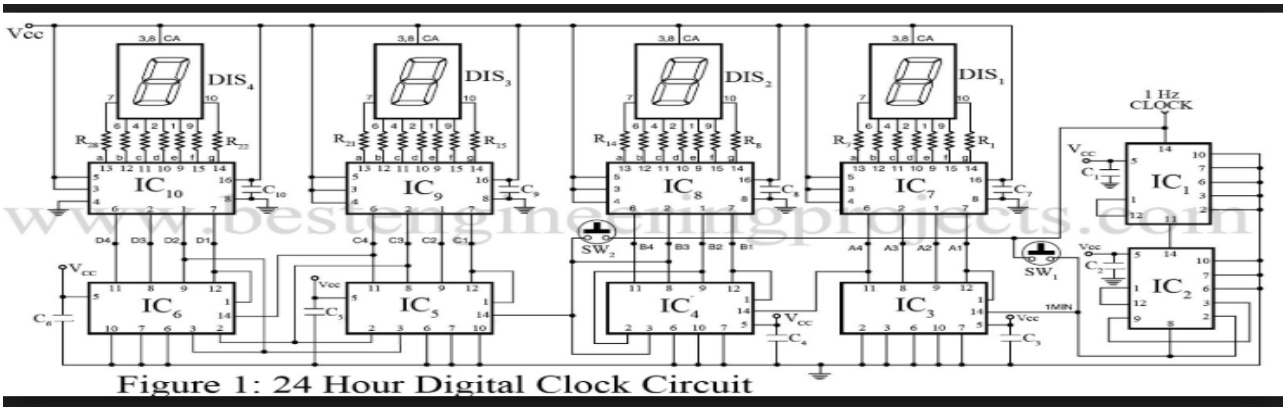


Figure 1: 24 Hour Digital Clock Circuit

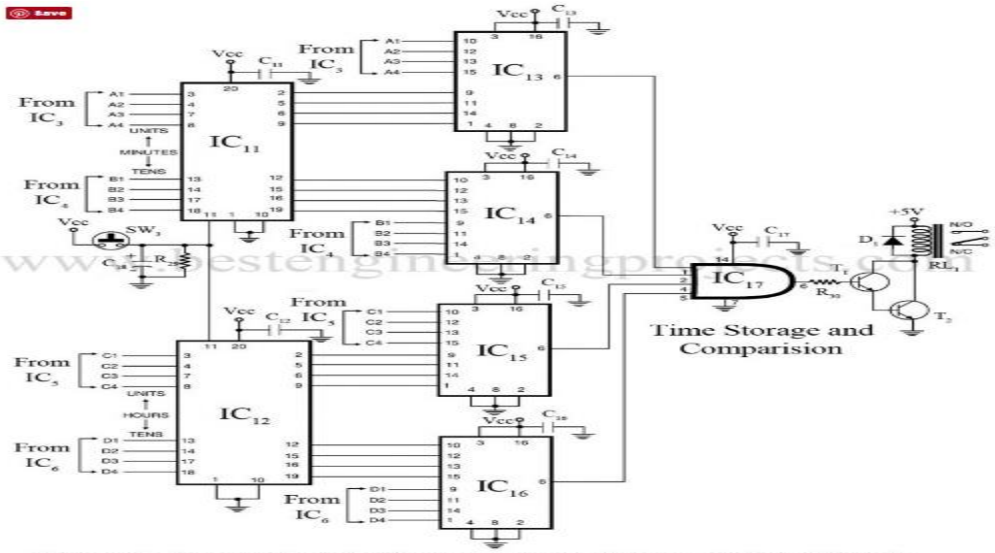


Figure 2: Storage/Latch, Comparator and Relay Driver Circuit

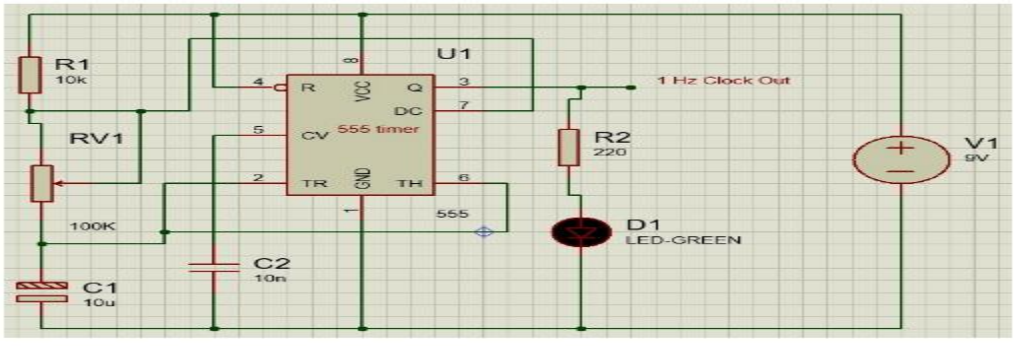


Figure : 1 Hz Clock Pulse Generator

PROJECT COMPONENTS:

Resistors (all ¼-watt, ±5% carbon, unless stated otherwise):

- ✓ R_1 – R_{28} = 560 Ω
- ✓ R_{29} = 10 KΩ
- ✓ R_{30} = 1.8 KΩ

Capacitors

- ✓ C_1 – C_{17} = 0.1 µF Caramic Disc
- ✓ C_{18} = 1 µF/16V Electrolytic Capacitors

Semiconductors

- ✓ IC_1 – IC_6 = 74LS90 (Decade Counter)
- ✓ IC_7 – IC_{10} = 74LS247 (BCD to 7-Segment Decoder/Driver)
- ✓ IC_{11}, IC_{12} = 74LS373 (Octal D-type transparent latches)
- ✓ IC_{13} – IC_{16} = 74LS85 (4-bit magnitude comparator)
- ✓ IC_{17} = 74LS21 (dual 4-input positive AND gate)
- ✓ T_1 = BC547 NPN Transistor

Miscellaneous

- ✓ DIS_1 – DIS_4 = FNDLTS542 (common anode display)
- ✓ SW_1 – SW_3 = PUSH-TO-ON Switch
- ✓ RL_1 = 5V, 200 Ω Relay

PROJECT WORKING

A 24-Hour Digital Clock Circuit:

Fig. 1. shows the circuit of 24-hour digital clock section. This section is designed to display the time in hours and minutes format, and is wired such that it functions in 24-hour mode. For this purpose, this circuit make use of six 74LS90 decade counters (in figure,IC1 through IC6), four 74LS247 BCD to 7-segment decoders/drivers (IC7 through IC10) and four LT S542 common anode displays (DIS1 through DIS4). In addition, passive components like few resistors, capacitors and push-to-on switches are employed. A 1Hz clock is used to supply the input to the IC1 through pin 14. 1 Hz clock generator circuit is shown in button of article. The output obtained from both of the above mentioned circuits become more accurate with the fact that sboth circuit take advantage of 32.768kHz quartz crystal.

Description of Counter Circuit:

Each ICs are designed/wired with particular task to perform. During this course, IC1 serves as divide-by-10 counter and the IC2 as divide-by-6 counter. Thus the output of IC2 connected to clock pin 14 of IC3 has a pulse recurrance period of one minute. In the similar way, following the connection pattern of IC1-IC2, IC3-IC4 pair is wired likewise. And, so the output of IC4 connected to clock pin 14 of IC5 has a pulse recurrence frequency of one hour. IC pair 5 and 6(IC5-IC6) is set such that it resets itself on reaching a count of 24. The BCD to 7-segment decoders IC7 through IC10 are used to decode the BCD outputs of IC3 through IC6. In response to which, the 7-segment common-anode displays DIS1 is driven through DIS4 respectively. The clock gets reset at 24 hour's count and for this reason, the maximum time that would be

displayed by the clock is 23 hours and 59 minutes. The BCD outputs of IC3 through IC6, marked A1 through A4, B1 through B4, C1 through C4 and D1 through D4 respectively, are also connected to various IC pins (Fig. 4) bearing identical markings. Circuit noise can rise as a major problem in the operation. To solve this, Decoupling capacitors of 0.1µF each have been used between Vcc and ground of all ICs. We can see in the figure, the 1Hz clock is also connected to one of the poles of push-to-on switches S1 and S2. These switches are used for quick adjustment of minutes and hours count respectively. With this arrangement of switches, the clock can be set to display any desired time between zero hours and zero minutes to 23 hours and 59 minutes.

Preset Time Storage, Comparator & Relay Driver Circuit:

The circuit design of second part is clearly illustrated in fig.2. which comprises preset time storage, magnitude comparator and relay driver part. Major components of this circuit can be enlisted as: two 74LS373 octal 'D' type transparent latches (IC11 and IC12), four 74LS85 4-bit magnitude comparators (IC13 through IC16), one 74LS21 dual 4-input AND gate (IC17) and Darlington pair comprising transistors BC547 (T1) and SL100 (T2). Each nibble (4-bit sequence) of BCD data from IC3 through IC6 of first part of the clock circuit is connected to IC11 and IC12 (two nibbles to each of these ICs). The reason behind doing so is to latch (store) by momentary depression of press-to-on switch S3. The latched nibbles are connected as one set of 4-bit data inputs to magnitude comparator ICs 74LS85, while the other set of 4-bit data (BCD output from IC3 through IC6) are directly connected to comparators as shown in Fig. 4. These nibbles directly connected and latched ones are compared. When all four nibbles of stored/latched data equal the directly connected four nibbles of data, pin 6 of all 74LS85 ICs go to logic 1 state. This results in pin 6 of 4-input AND gate of IC17 going high and then energizes relay RL 1 via Darlington pair comprising transistors T1 and T2. For further clarification of the operation procedure, one must go through the following description.

Operation Of 24-Hour Digital Clock and Timer Circuit:

The desired pre-setting time for the load or appliance to be switched 'on' or 'off ' is carried out with the help of switches S1 and S2 by looking at the digital display. Switch S3 is pressed briefly, once the display shows the desired time. IC11 and IC12 are used to store time just programmed. This latched time appears as one of the BCD inputs at each of the four comparator ICs (IC13 through IC16). Now using the same switches (S1 and S2), the current time is set. In similar way, the BCD equivalent of the current time appears as the second set of inputs for IC13 through IC16. The current time (real time) keeps advancing since the 1Hz input continuously updates the clock/timer. After a certain interval, time reaches the maximum limit. Once the current time reaches the preset time, both sets of input BCD numbers to 74LS85 comparator ICs become equal and this sets pin 6 reach the logic 1 state. As a result, output of AND gate (IC17) goes to logic 1 state and energises relay RL 1 via the Darlington pair of transistors Tl and T2 as stated earlier in the circuit description.:

PROJECT LOGIC DIAGRAM:

DECADE COUNTER

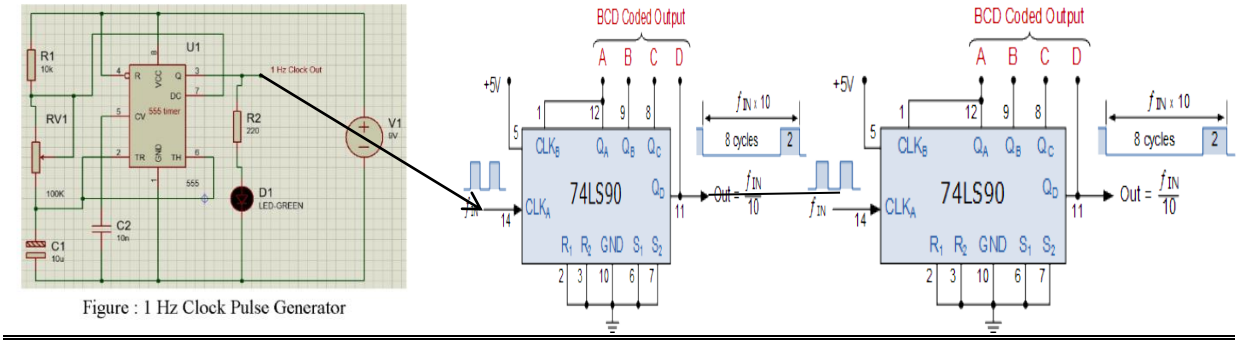
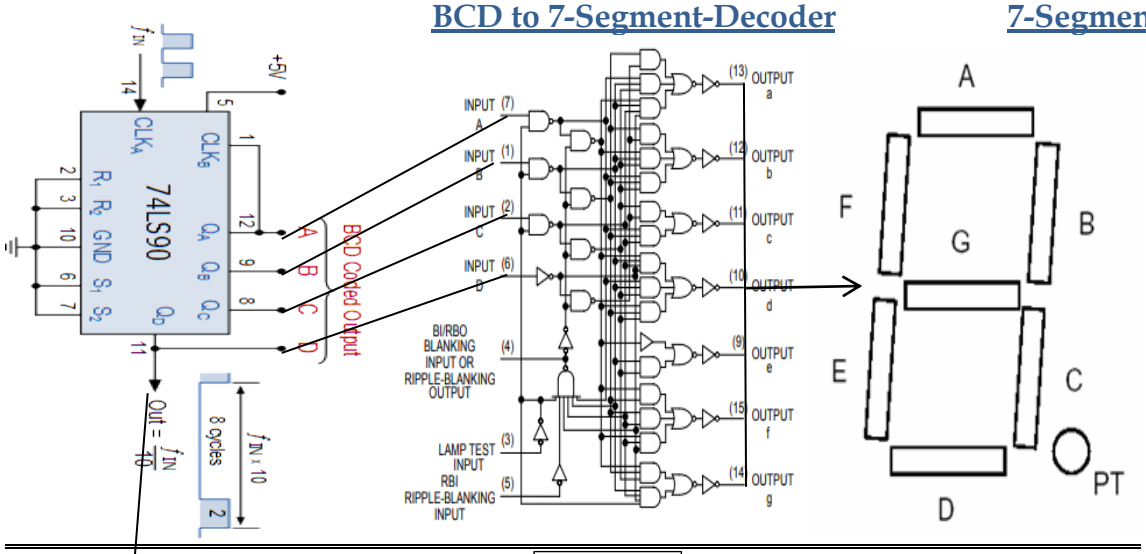


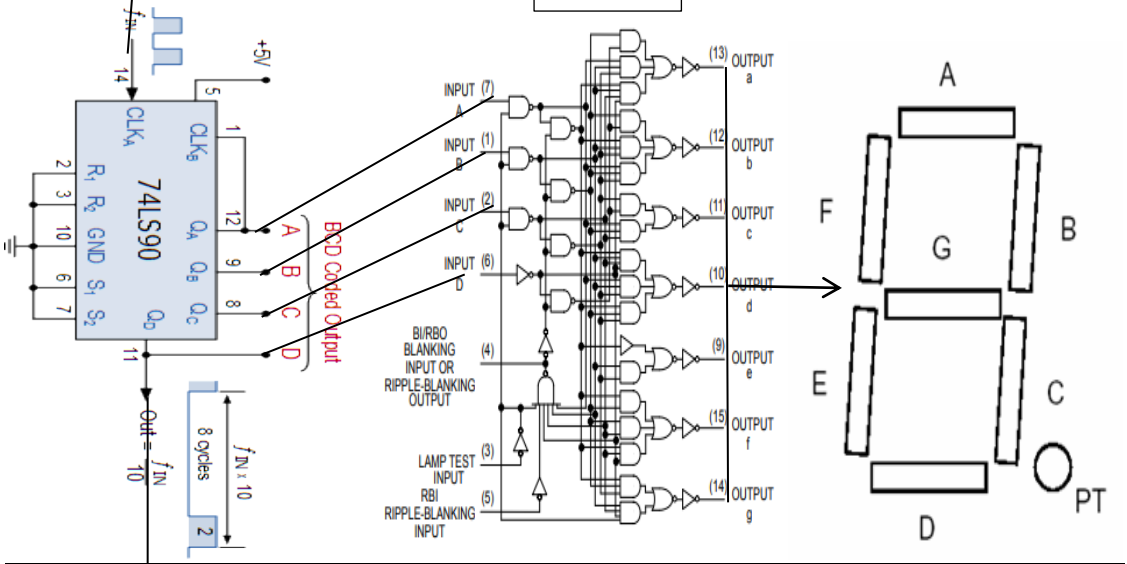
Figure : 1 Hz Clock Pulse Generator

DECADE COUNTER

BCD to 7-Segment-Decoder 7-Segment-Display



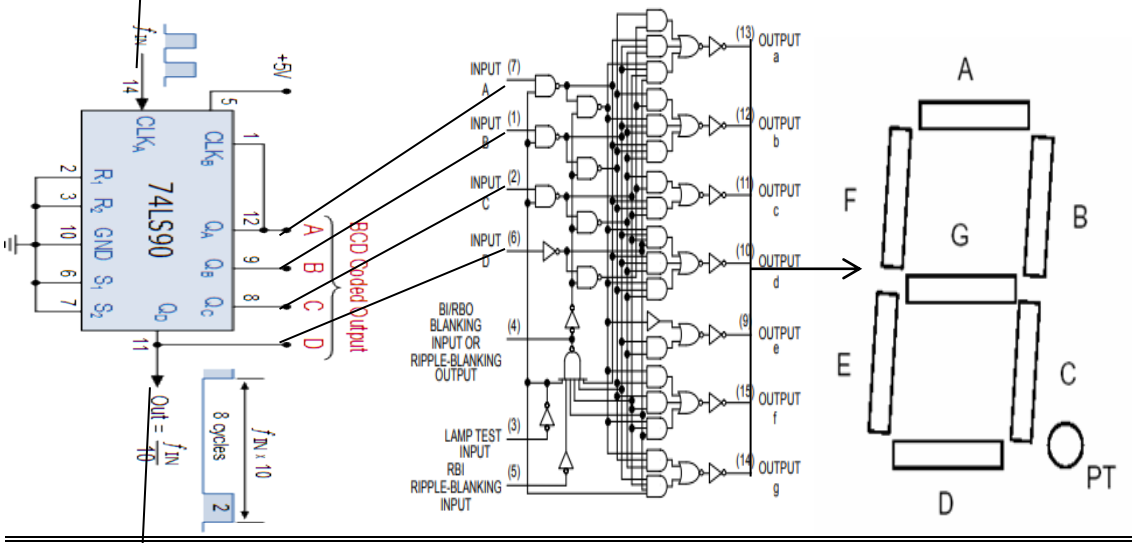
74LS247



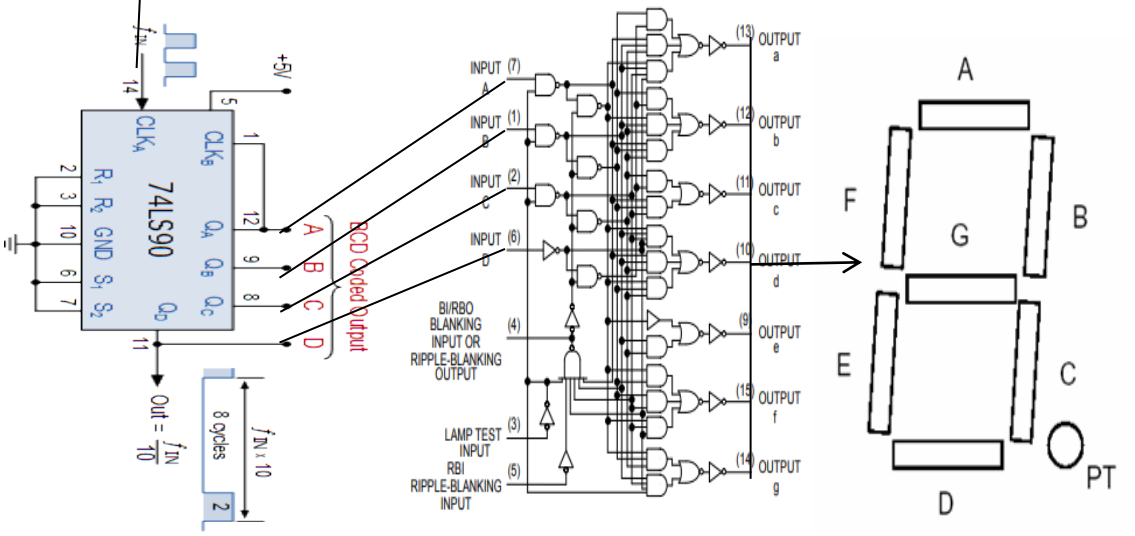
74LS247

DECADE COUNTER

DECADE COUNTER



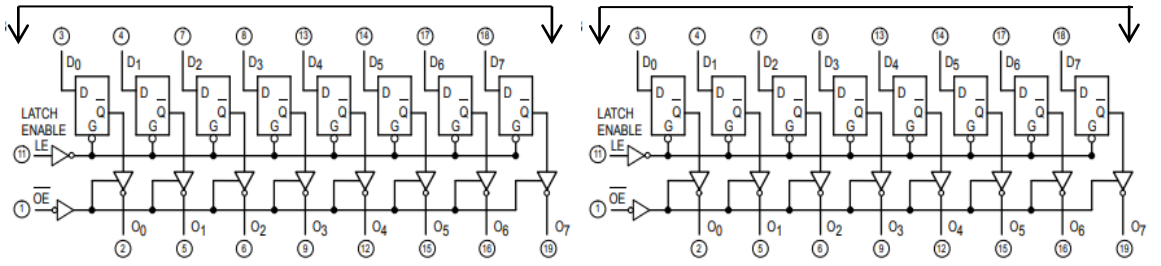
74LS247



74LS247

Outputs From IC-3 & IC-4 (74LS90)

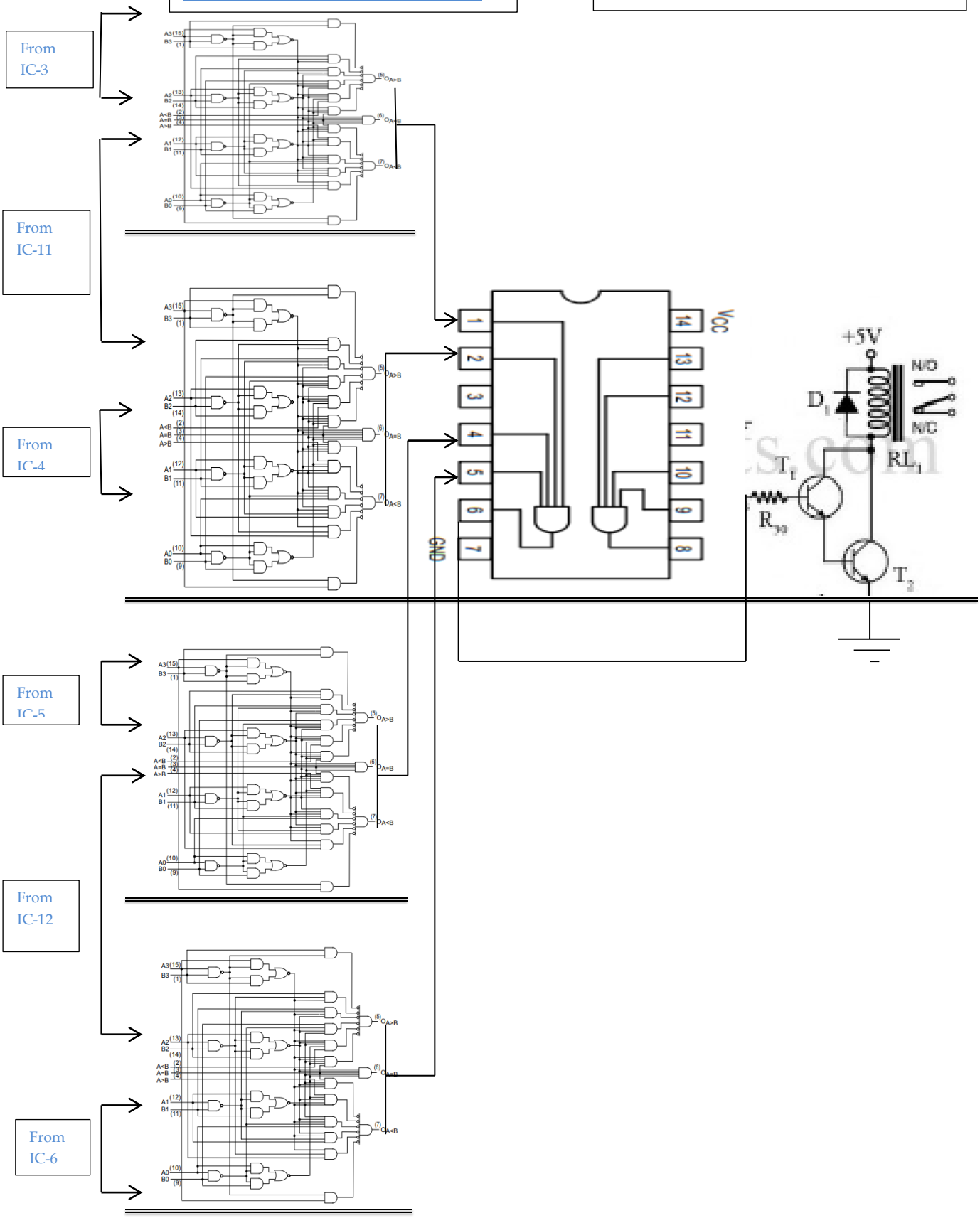
Outputs From IC-5 & IC-6 (74LS90)



IC-13 IC-14 IC-15 IC-16

4-bit-magnitude COMPARATOR(74LS373)

Dual-4-input-positive-AND-gate(74LS21)



TRUTH' TABLES:

DECADE COUNTER (74LS90):

General Description:

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the DM74LS90. All of these counters have a gated zero reset and the DM74LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications. To use their maximum count length (decade or four bit binary), the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the DM74LS90 counters by connecting the QD output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output QA.

Function Tables

BCD Count Sequence (Note 1)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2) (Note 2)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

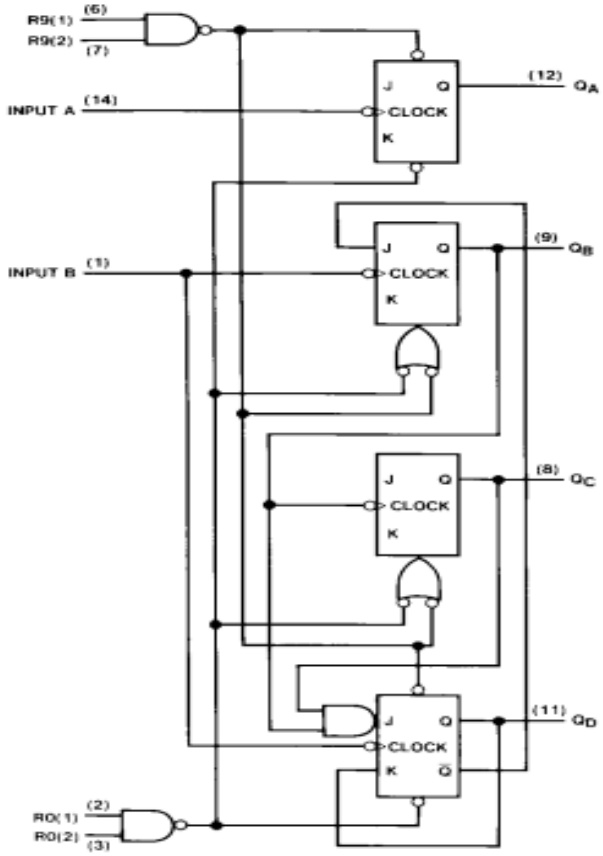
H = HIGH Level
L = LOW Level
X = Don't Care

Note 1: Output Q_A is connected to input B for BCD count.

Note 2: Output Q_D is connected to input A for bi-quinary count.

Note 3: Output Q_A is connected to input B.

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a high level.

BCD-to-7-SEGMENT-DECODER (74LS247):

General Description:

The 74LS247 is BCD-to-Seven-Segment Decoder/Drivers. The 74LS247 isfunctionally and electrically identical to the 74LS47 with the same pinout configuration. The LS247 has active-low outputs for direct drive of indicators. All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level.. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247

- *Open-Collector Outputs Drive Indicators Directly*
- *Lamp-Test Provision •*

Leading/Trailing Zero Suppression

LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	1
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

OCTAL "D" TRANSPARENT LATCH {FLIP-FLOP} (74LS373):

General Description:

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high immendense state . :

LS373

D_n	LE	OE	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

:

PIN NAMES

D_0–D_7	Data Inputs
LE	Latch Enable (Active HIGH) Input
$\overline{CP}$	Clock (Active HIGH going edge) Input
$\overline{OE}$	Output Enable (Active LOW) Input
O_0–O_7	Outputs (Note b)

4-BIT-MAGNITUDE-COMPARATOR (74LS85):

General Description:

The SN54/74LS85 is a 4-Bit Magnitude Camparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$, $O_{A<B}$, and $O_{A=B}$ Outputs Available

PIN NAMES

A_0-A_3, B_0-B_3	Parallel Inputs
$I_{A=B}$	A = B Expander Inputs
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs
$O_{A>B}$	A Greater Than B Output (Note b)
$O_{A<B}$	B Greater Than A Output (Note b)
$O_{A=B}$	A Equal to B Output (Note b)

TRUTH TABLE

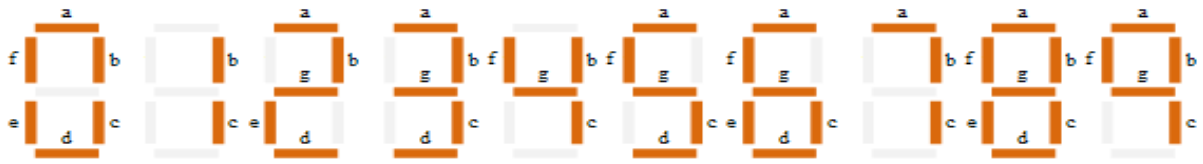
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

DUAL-4-INPUT-AND-GATE (74LS21):

A	*B*	*OUTPUT*
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

7-SEGMENT-DISPLAY (COMMON ANODE DISPLAY):

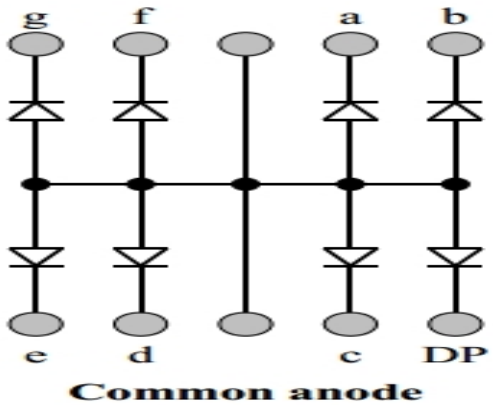


Common Anode 7-segment Display

In general, common anode displays are more popular as many logic circuits can sink more current than they can source. Also note that a common cathode display is not a direct replacement in a circuit for a common anode display and vice versa, as it is the same as connecting the LEDs in reverse, and hence light emission will not take place.

Depending upon the decimal digit to be displayed, the particular set of LEDs is forward biased. For instance, to display the numerical digit 0, we will need to light up six of the LED segments corresponding to a, b, c, d, e and f. Thus the various digits from 0 through 9 can be displayed using a 7-segment display.

Segments Inputs							7 Segment Display Output
a	b	c	d	e	f	g	
1	1	1	1	1	1	0	0
0	1	1	0	0	0	0	1
1	1	0	1	1	0	1	2
1	1	1	1	0	0	1	3
0	1	1	0	0	1	1	4
1	0	1	1	0	1	1	5
1	0	1	1	1	1	1	6
1	1	1	0	0	0	0	7
1	1	1	1	1	1	1	8
1	1	1	1	0	0	1	9



PROJECT BLOCK DIAGRAM: