LYNRED

CONFIDENTIAL

USER GUIDE

Thermal Imaging Cooled Sensor User Guide

PlugUp Platform
EOLE MW K588

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Chapter 1. Introduction

This technical manual deeply describes the operating principle of the Lynred product based on “PlugUp platform” EOLE . This platform is composed of:

- A Linear Cooler K588
- A housing/frame for mechanical integration and thermal management

This document includes:

- Mechanical integration
- Optical interfaces
- Thermal management
- Feature overview
- Electrical I/O definition
- Communication protocol and associated commands.

Chapter 2. Reference Documents

2.1. Applicable documents

1. **[AD 1]** AIA Camera Link® version 1.2: Specifications of the Camera Link Interface Standard for Digital Cameras and Frame Grabbers
2. **[AD 2]** MODBUS over serial line specification and implementation guide V1.02: Specifications of Cyclical Redundancy Checking generation
3. **[AD 3]** User Guide NTG003 - Optical interfaces of standard MW IDDCAs - Latest issue
4. **[AD 4]** 05_445_001_E Mechanical Drawing - Latest Issue
5. **[AD 5]** NTC098 Specification EOLE MW K588 - Latest issue

Chapter 3. Acronyms

ADC Analog to Digital Converter

BIT Built In Test

BP Bad Pixel

BPR Bad pixel replacement

BPT Bad Pixel Table

C&CE Command And Control Electronic (also called Proxyboard)

CL CamerLink

CTRL Control

DTI Double Integration Time

FPA Focal Plane Array

FPGA Field-Programmable Gate Array

FOV Field Of View

GP Good Pixel

ICD Interface Control Document

IDDCA Integrated Detector Dewar Cooler Assembly

INT Integration phase signal

IR Infra-Red

ISP Image Signal Processing

ITR Integration Then Reading

IWR Integration While Reading

JTAG Joint Test Action Group = Boundary Scan

MSB Most Significant Bit

MW Mid wave

N/A Not Applicable

NETD Noise Equivalent Temperature Difference

NOK Not Okay, Not Valid

NUC Non Uniformity correction

OEM Original Equipment Manufacturer

OK Okay, Valid

ROIC Read out integrated circuit

RO Read Only

RW Read Write

SRC Source

Tamb Ambient Temperature

TBC To Be Confirmed

TBD To Be Defined

TMCK Master Clock Period

UART Universal Asynchronous Receiver Transmitter

Chapter 4. General Description

4.1. General overview

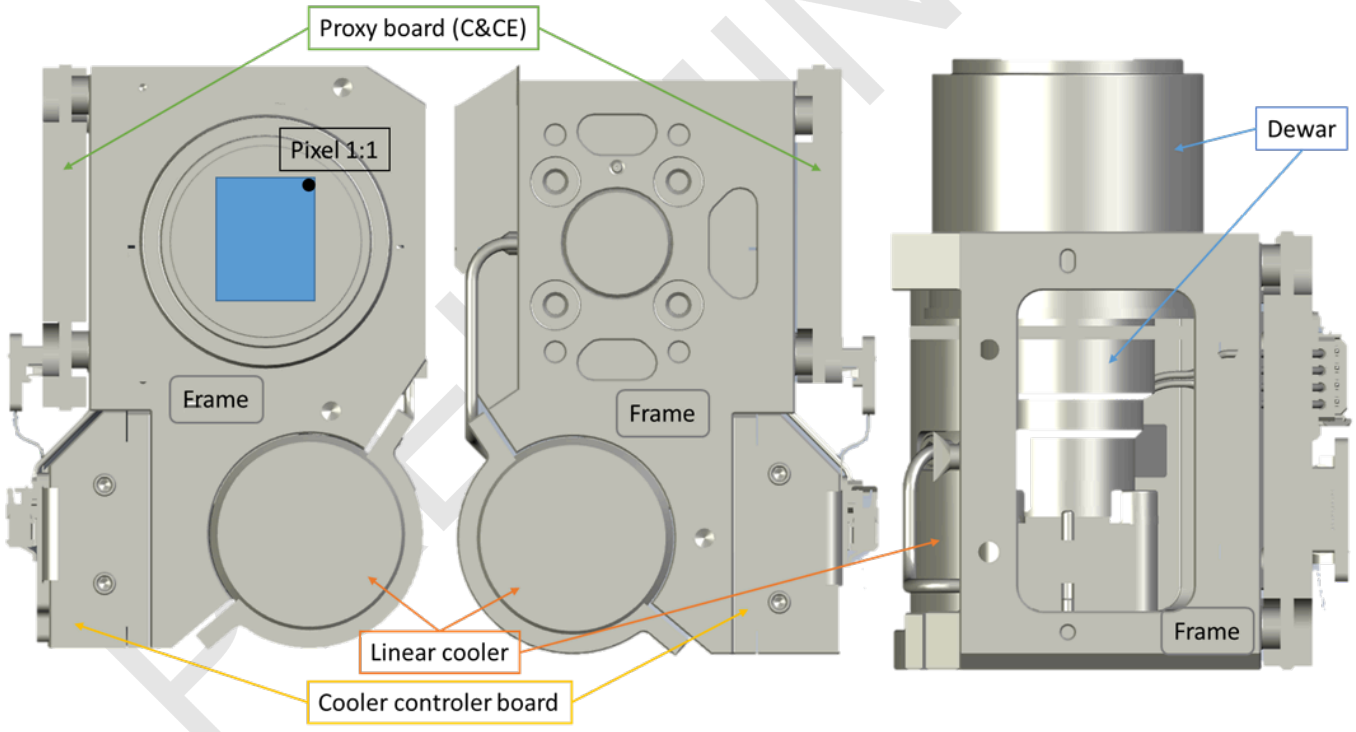
The product is composed of the following sub-assemblies:

Table 1. IDDCA sub-assemblies

Element	Function
Dewar	Hosts the FPA in a thermally-isolated environment while allowing photons to reach the sensitive area
Linear cooler	Cools the FPA down to its nominal operating temperature
Cooler driver Cooler controller board	Drives the cooler motor, and regulates the FPA temperature Provides a configuration interface (through C&CE)
Command & Control Electronics (C&CE) Electronic Proxy Board	Powers the FPA Provides a standard CameraLink© video output Provides a configuration interface

The following figure illustrate the product architecture.

Figure 1. Product overview

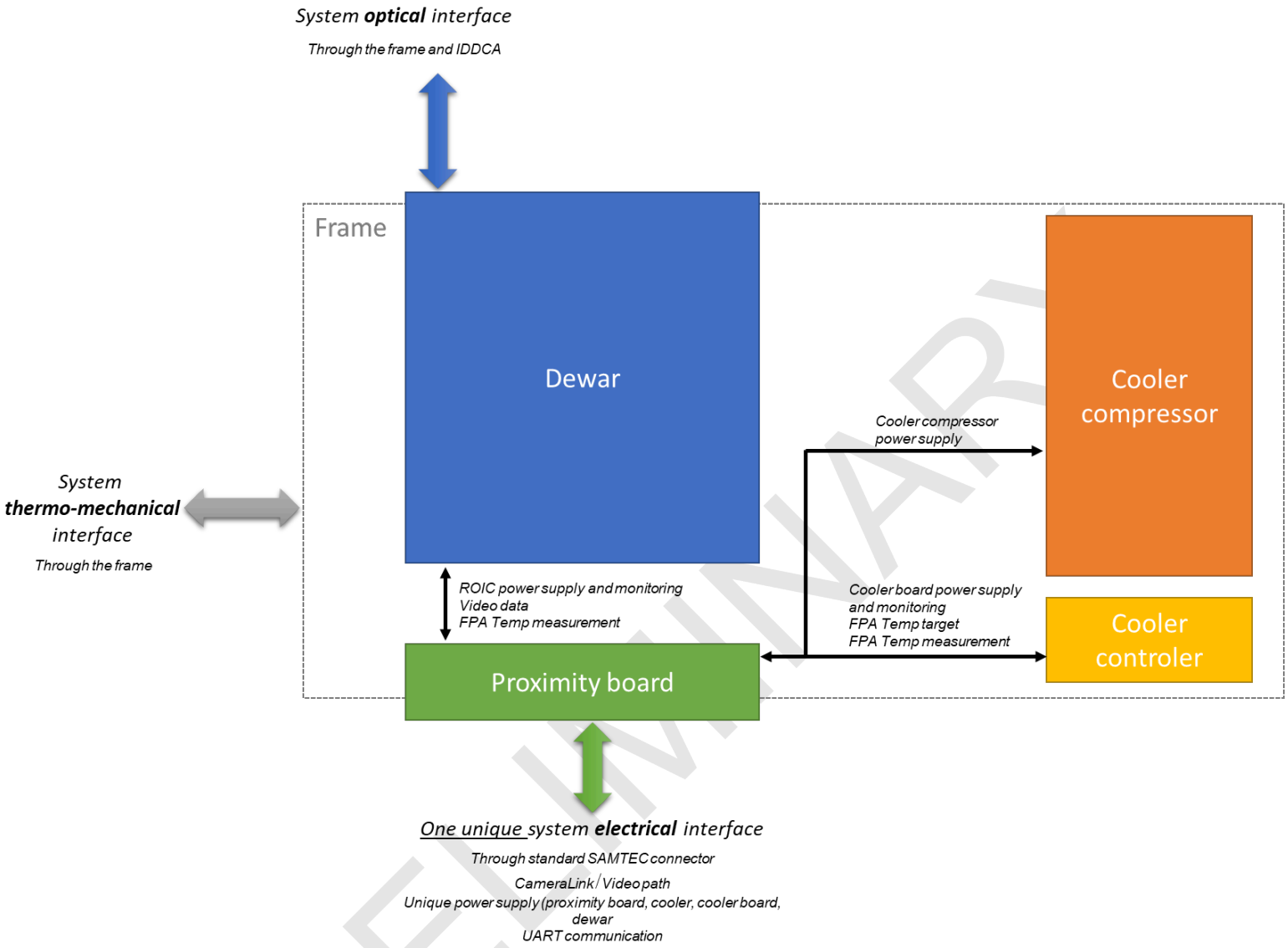


4.2. Product Schematic

The product schematic is visible below. All main components (Dewar, cooler, cooler board, proximity board) are maintained thanks to a frame. This frame allows mechanical interface, thermal dissipation and optical alignment.

There is one unique electronic interface to power supply IDDCA, configure it and catch video path on the proximity board.

Figure 2. Product schematics



Chapter 5. Mechanical Interfaces

5.1. Introduction

The detector can be positioned in the system using 2 mechanical interfaces (see bellow MI1 & MI2). Other attachments may damaged the product and are not recommended by Lynred. The interface called “MI1” is the one certified for all the mechanical and thermal environments. For more details regarding qualified environnments please refer to product specification (NTC) **[AD 5]**

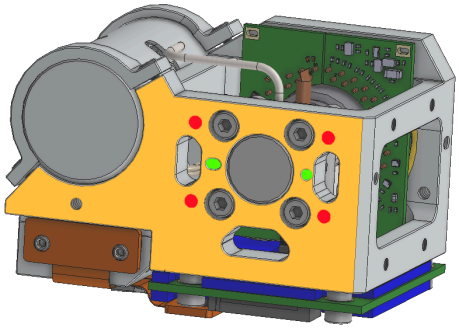
5.2. Mechanical Interface (MI1)

Detector can be positioned with 2 pins Ø2mm to be inserted in green hole & oblong hole here after

Detector can be fixed to the system with 4 screws M3, torque 0.9 Nm, in the threads in red here after

For dimensions, see detector drawing interface. **[AD 4]**

Figure 3. Mechanical Interface MI1



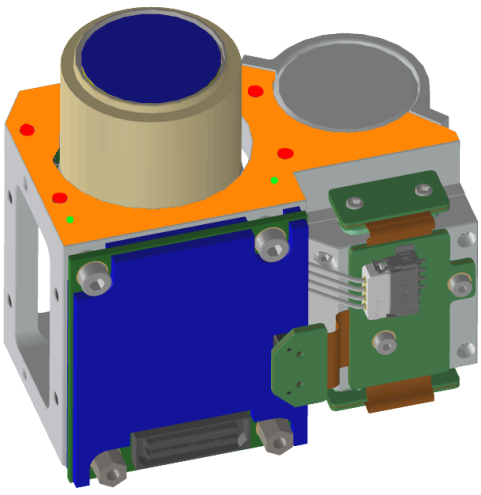
5.3. Second Interface (MI2)

Detector can be positioned with 2 pins Ø1mm to be inserted in green holes here after

Detector can be fixed to the system with 4 screws M3, torque 0.9 Nm, in the threads in red here after

For dimensions, see detector drawing interface **[AD 4]**

Figure 4. Mechanical Interface MI2



Chapter 6. Optical Interface

6.1. General

The optical interfaces consist of an antireflective coated infrared window, a cold filter,

a cold shield and the infrared focal plane array. All optical materials are described in product drawings and product specifications **[AD 4] [AD 5]**

6.2. Infrared window and cold filter

The infrared window is antireflective coated in order to optimize the incident radiation

on the FPA array from 2µm to 4.4µm. It is made of Silicon (refractive index = 3.4).

More details are visible in **[AD 3]**

Remarks: due to the window and filter materials and coatings, the IDDCA is not sensitive to visible radiations.

6.3. Infared focal plane array

The position of focal plane array is defined in product drawings and product specifications **[AD 4] [AD 5]**

6.4. Cold shield

The cold shield allows the elimination of the unwanted incident radiation on the FPA. The aperture is aligned relative to the focal plane array.

The main dimensions of the cold-shield are described in product drawings and product specifications **[AD 4] [AD 5]**

Chapter 7. Thermal Management

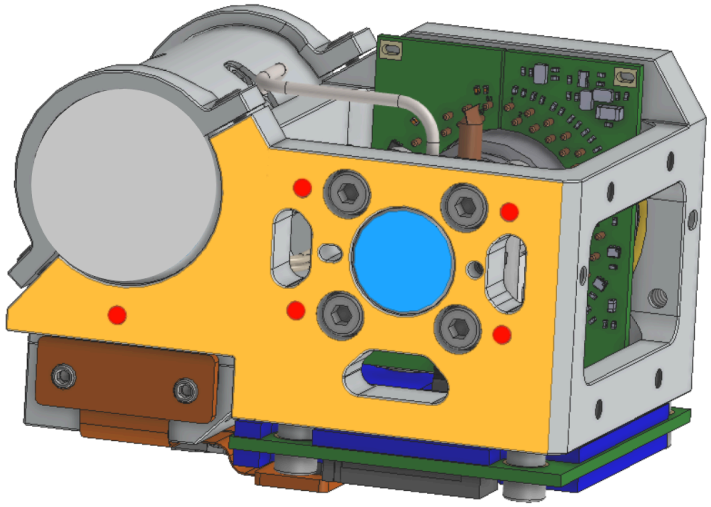
7.1. Specifications

Detector power dissipation must be correctly evacuated to limit the temperature of the whole product to a maximum of 10°C over the ambient temperature. Out of this domain of use, the detector can be damaged and will not work properly. Heat evacuation will limit the risks of burns and will maintain the detector within the acceptable temperature range. The system must be designed to reduce the detector temperature and to accept these maximal temperatures itself. The typical power that have to be dissipated is visible in product specification **[AD 5]**

The warm area of the detector from which the heat must be removed during operation are presented below:

- The main thermal interface surface in orange
- The optional thermal surface of the cooler in blue
  - Please note relative position between this blue surface and frame interface (orange) can change from one product to another. To improve thermal dissipation, LYNRED recommends to use a thermal pad on blue part to adjust heigh difference between these 2 surfaces (see **[AD 4]** and **[AD 5]** for more details about dimensions)

Figure 5. Thermal management



7.2. Technical information

The characteristics of the mechanical surface (in orange) are :

- Surface : 1333mm²
- Material : 7075 Aluminium with Nickel plating
- Surface Roughness : Ra < 1.6µm
- Flatness : <0.2mm

The characteristics of the cooler surface (in blue) are :

- Surface : 137mm²
- Material : SST 304L
- Surface Roughness : PER ISO 1302 NA
- Flatness : <0.1mm

Chapter 8. Programming recommendations

8.1. Maximum Frame Rate

Maximum frame rate achievable depends on several parameters:

- Integration mode: ITR or IWR
- nbr_{pixels} : Number of pixel read (640*512 = 327680 for full format)
- $Freq_{MCLK}$: Master Clock Frequency (Hz)
- $nbr_{outputs}$: Number of video outputs
- $Tint$: Integration time

$$\text{Max Frame rate}\,(\text{Hz}) = \frac{1}{\text{Min } T\,\text{trame}\,(\text{sec})}$$

- For ITR mode:

$$\text{Min } T\,\text{trame}\,(\text{sec}) = \text{Tint} + \frac{\text{nbr}_{\text{pixeks}}}{\text{Freq}_{\text{MCLK}} \times \text{nbr}_{\text{outputs}}}$$

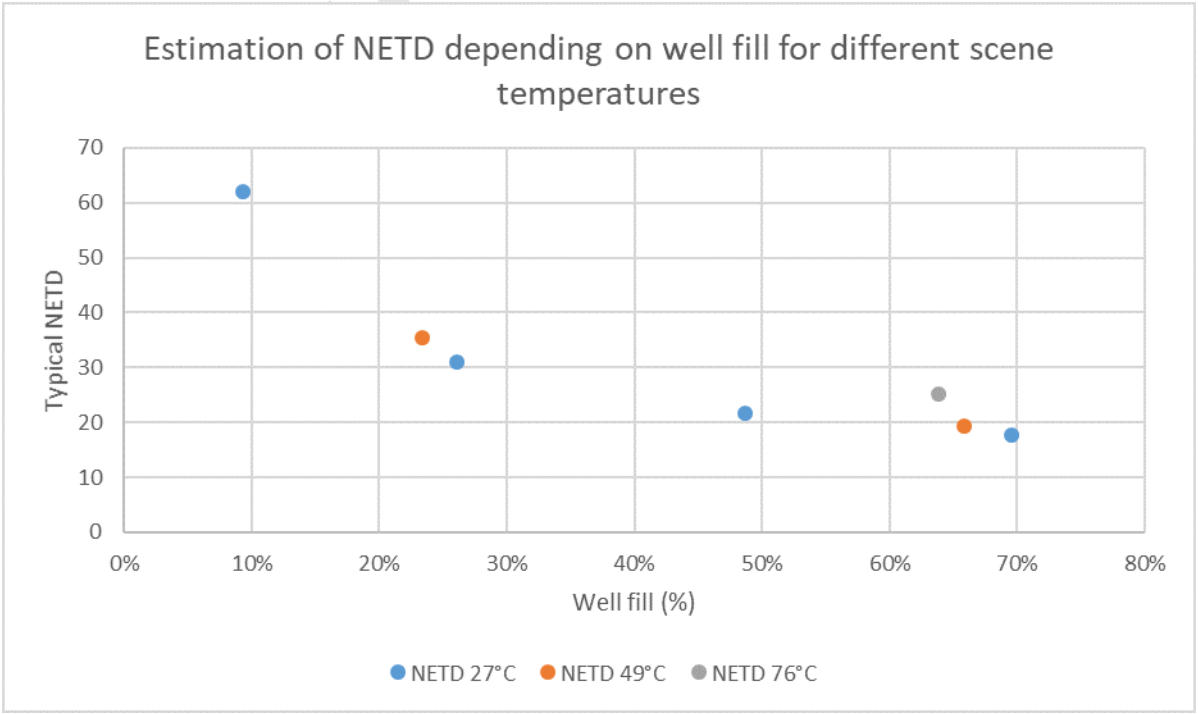
- For IWR mode:

$$\text{Min } T\,\text{trame}\,(\text{sec}) = \max\left\{\text{Tint}; \frac{\text{nbr}_{\text{pixeks}}}{\text{Freq}_{\text{MCLK}} \times \text{nbr}_{\text{outputs}}}\right\}$$

8.2. Impact of integration time on NETD

Integration time can affect NETD. The following graph provides an example of NETD evolution with different scene temperatures and different integration times (which impact well fill). Higher integration times (higher well fill) improves image quality.

Figure 6. Evolution of NETD depending on well fill and scene temperature



8.3. IDDCA Dynamic Range

Section **10.5.3. Video Analog to Digital Conversion** details how analog signal from FPA is converted into numerical values.

Minimum pixel value is called "reference" and corresponds to zero integration.

Typical reference level is 1.38Vdc = 1016

Maximum pixel value is called “saturation”.

Typical saturation level is 2.55Vdc = 15876

Chapter 9. Electrical Interface

The whole IDDCA is driven through the proximity board.

The aim of the proximity board is to simplify the use of a cooled infrared detector.

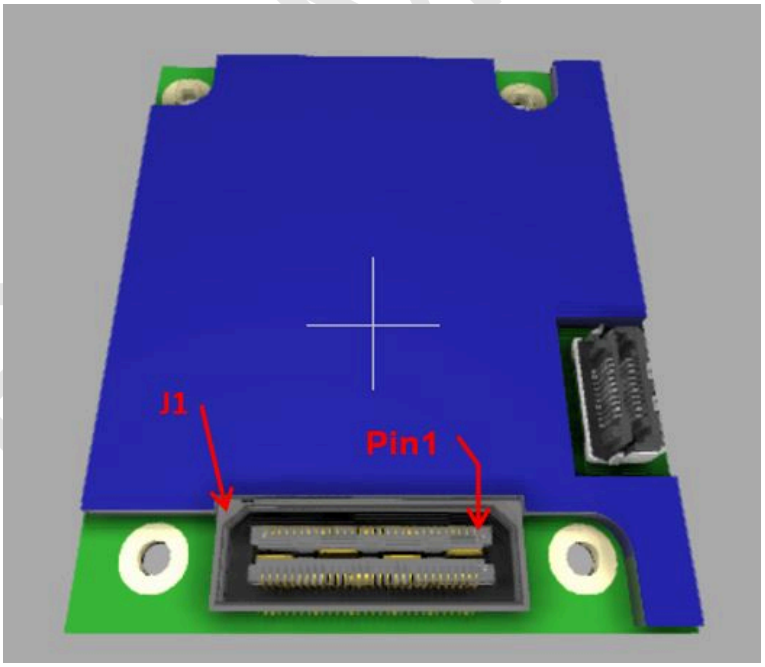
The proximity board provides the following functionalities:

- Power the IR detector (biases, analog and digital supplies).
- Configure the IR detector (frame size, frame flip, integration time …).
- Condition the detector analog video output (gain and offset).
- Digitalize the analog video signal (if needed)
- Format the video stream according to Camera Link standard.
- Monitor the FPA temperature.
- Perform Built in tests.
- Manage Power Consumption.
- Forward the FPA temperature diode signal to the cooler driver.
- Control cooler driver.

Please note this board is not protected with a conformal coating.

9.1. Connector Position and Pin Numbering

Figure 7. Connector Position and Pin Numbering



9.2. J1: System Connector and signals

9.2.1. Connector Reference

The J1 connector is the part number QSH-030-01-C-D-A from Samtec. It can mate with :

- Samtec QTH-30-0x-x-D-A connector.
- Please note a SAMTEC plane cable with a no cap connector is required to correctly mate with the board (example below)
  - HQCD-030-XX.XX-YYY-ZZZ-1-**N**
- This connector is compatible with vibration level up to 7.3 G_{rms}. For higher levels, a custom electrical interface attached to the detector frame using IDDCA standoffs is recommended (see detailled drawing for position **[AD 4]**)
- The maximum recommended torque is 0.6 Nm.

9.2.2. Connector Pinout

The J1 connector pinout is described in the table below:

Table 2. J1: System connector

Function	Signal Type	Name	Pin	Pin	Name	Signal Type	Function
Power supply	POWER	PSYS	1	2	PSYS	POWER	Power supply
Power supply	POWER	PSYS	3	4	PSYS	POWER	Power supply
Ground signal reference	POWER	GND	5	6	GND	POWER	Ground signal reference
Negative signal of differential X0 data pair	LVDS_OUT	X0_M	7	8	NC		Not connected
Positive signal of differential X0 data pair	LVDS_OUT	X0_P	9	10	NC		Not connected
Ground signal reference	POWER	GND	11	12	GND	POWER	Ground signal reference
Negative signal of differential X1 data pair	LVDS_OUT	X1_M	13	14	NC		Not connected
Positive signal of differential X1 data pair	LVDS_OUT	X1_P	15	16	NC		Not connected
Ground signal reference	POWER	GND	17	18	GND	POWER	Ground signal reference
Negative signal of differential X2 data pair	LVDS_OUT	X2_M	19	20	NC		Not connected
Positive signal of differential X2 data pair	LVDS_OUT	X2_P	21	22	NC		Not connected
Ground signal reference	POWER	GND	23	24	GND	POWER	Ground signal reference
Negative signal of differential X3 data pair	LVDS_OUT	X3_M	25	26	NC		Not connected
Positive signal of differential X3 data pair	LVDS_OUT	X3_P	27	28	NC		Not connected
Ground signal reference	POWER	GND	29	30	GND	POWER	Ground signal reference
Negative signal of differential PIX CLK pair (channel X)	LVDS_OUT	XCLK_M	31	32	NC		Not connected
Positive signal of differential PIX_CLK pair (channel X)	LVDS_OUT	XCLK_P	33	34	NC		Not connected
Ground signal reference	POWER	GND	35	36	GND	POWER	Ground signal reference
Negative signal of differential CC1 pair	LVDS_IN	CC1_M	37	38	TC_M	IN	Negative signal of differential TC pair
Positive signal of differential CC1 pair	LVDS_IN	CC1_P	39	40	TC_P	IN	Poitive signal of differential TC pair

Function	Signal Type	Name	Pin	Pin	Name	Signal Type	Function
Ground signal reference	POWER	GND	41	42	GND	POWER	Ground signal reference
Negative signal of differential CC2 pair	LVDS_IN	CC2_M	43	44	TFG_M	OUT	Negative signal of differential TFG pair
Positive signal of differential CC2 pair	LVDS_IN	CC2_P	45	46	TFG_P	OUT	Positive signal of differential TFG pair
Ground signal reference	POWER	GND	47	48	GND	POWER	Ground signal reference
Negative signal of differential CC3 pair	LVDS_IN	CC3_M	49	50	SPARE_M		Positive signal of differential Spare pair
Positive signal of differential CC3 pair	LVDS_IN	CC3_P	51	52	SPARE_P		Negative signal of differential Spare pair
Ground signal reference	POWER	GND	53	54	GND	POWER	Ground signal reference
Not connected		NC	55	56	NC		Not connected
Factory	LVCMOS25_ IN	SWCLK	57	58	SWDIO	LVCMOS25_ IN/OUT	Factory
Ground signal reference	POWER	GND	59	60	GND	POWER	Ground signal reference
Ground signal reference	POWER	GND	Metal Plane		GND	POWER	Ground signal reference

Note :

- TC shall not be left floating to avoid unwanted request to the proxy.
- CC1 and CC2 can be left floating if not used without damage. However floating differential input may pick up noise and falsely switch increasing power consumption.
- CC3 inputs have on-board failsafe bias stage and can be left floating.
- SPARE input is internally tied to GND by the FPGA I/O with a weak pull-down and can be left floating.
- SWDIO and SWCLK shall be left floating.

9.2.3. Signals DC Characteristics

9.2.3.1. Typical characteristics

The *Table 3, "Typical Characteristics at 25°C, PSYS=12V"* summarizes the typical characteristics with Input voltage = 12.0V, Ambient temperature = 25°C and no aging.

Table 3. Typical Characteristics at 25°C, PSYS=12V

Parameters	Typical value	Unit
Power Input Voltage	12.0	V
Max Power consumption (2 channels, f=10.29MHz)	800	mW
Max Power consumption (4 channels, f=10.29MHz)	900	mW
ADC Resolution	14	Bits
LSB size	78.74	µV
Video Noise Level (input equivalent)	<135	µVRMS
Video Linearity Error	<500	ppm
Detector Frequency	10.29	MHz

GPOL resolution	1	mV
VRINT/VRLEC	1.4	V
FPA temperature accuracy (T ≥ 140K)	±2	K
GPOL resolution	1	mV

9.2.3.2. LVCMOS 25

Symbol	Parameter	Condition / Comment	Min.	Typ.	Max.	Unit
Vol[1]	Voltage Output Low		0	--	0.4	V
Voh[2]	Voltage Output High		2.0	--	2.5	V
Vil[3]	Voltage Input Low		0	--	0.6	V
Vih[4]	Voltage Input High		1.7	--	2.5	V

1. Voltage Output Low. The maximum positive voltage from an output that the device considers will be accepted as the maximum positive low level
2. Voltage Output High. The maximum positive voltage from an output that the device considers will be accepted as the minimum positive high level.
3. Voltage Input Low. The maximum positive voltage applied to the input that is accepted by the device as a logic low
4. Voltage Input High. The minimum positive voltage applied to the input that is accepted by the device as a logic high.

9.2.3.3. Standard LVDS : TIA/EIA-644

Symbol	Parameter	Condition / Comment	Min.	Typ.	Max.	Unit
Vih, Vil	Input Voltage		0	--	2.05	V
Vid_thd	Differential Input Threshold	(Vih-Vil)	±100	--	--	mV
Vicm	Input Common Mode Votage		0.05	--	2.0	V
Vod	Output Differential voltage	(Voh-Vol), RT[1] =100 Ohm	250	350	450	mV
Vos	Output Offset Voltage	(Voh+Vol)/2, RT[1] =100 Ohm	1.125	1.2	1.395	V

1. Receiver load resistance

Note:

- All traces for X[3..0] and XCLK must have the same length in order to minimize the delay between each pairs.

Figure 8. : Waveform for LVDS IN Signal Type

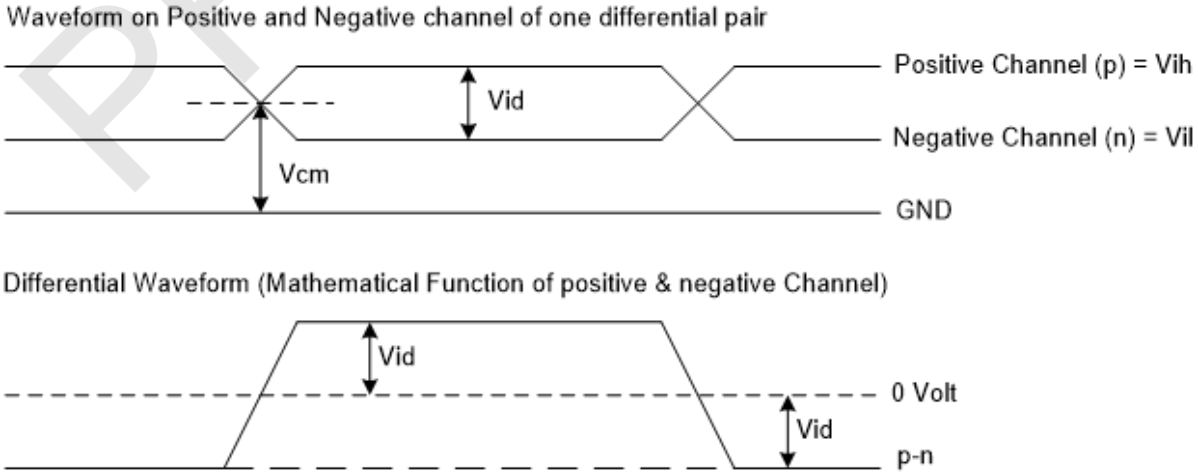
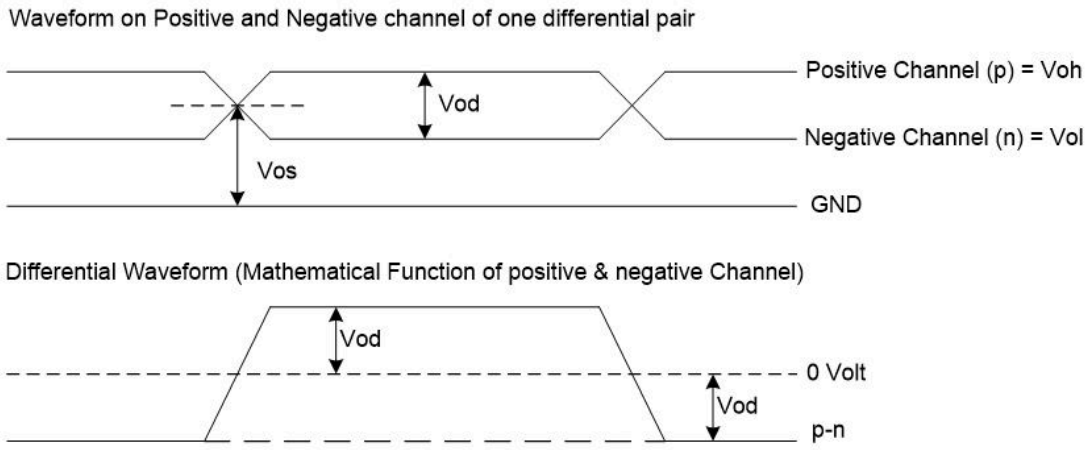


Figure 9. : Waveform for LVDS OUT Signal Type



9.2.3.4. Switching Characteristics

Parameter	Condition / Comment	Min.	Typ.	Max.	Unit
DCLKIN (CC2) frequency		7	--	20	MHz
DCLKIN (CC2) duty cycle		40	50	60	%
FSYNCIN (CC1) high level		300	--	--	ns
RESET (CC3) low time		50	--	--	ms
SER_TC / SER_TFG baudrate		4800	115200	460800	Baud
Board response time	115200 bauds[1]	2	5	10	ms
Board response time of COOLER registers	115200 bauds[1]		25		ms
Board startup time	External reset to board ready state	--	1	--	s
XClk Frequency		--		51.43	MHz
Xdata vs Xclk skew		--		+/-200	ps

1. Observed at TC / TFG signals level

Chapter 10. Proxy Electronics main functions

10.1. Power Up/Down Sequence

A strict power-up sequence is not required between the host system and detector. However the user should follow the requirements hereafter:

- Avoid driving inputs of an unpowered proxy board for a long time.
- Drive properly or left floating RESET inputs. Internal power-up reset is applied even if external reset is not asserted.
- Ensure that SER_TC UART input is in idle state (“1”) outside of communication requests.
- Power modes can reduce overall power consumption while keeping the FPA measurement fully operational.

10.2. Serial Communication

The host system communicates with the board using the Camera Link serial interface with a request / answer scheme. The board is controlled by reading and writing control and status registers.

10.2.1. UART Signals and Settings

The serial communication link is composed of two LVDS pairs:

Table 4. Serial communication signals

Connector Pin	Signal Name	Description
J1.SER_TC	TC	Serial communication to camera
J1.SER_TFG	TFG	Serial communication to frame grabber

The UART interface is set with the parameters below:

- 8 data bits
- 1 start bit
- 1 stop bit
- No parity bit and no handshaking
- The baud rate can be selected between 4300 and 430.800 bauds (default = 115200)

10.2.2. Protocol

The dialog with the proxy board uses a simple protocol, made of 5 commands to access the volatile registers that control the proxy and load or save their content in the internal non-volatile flash memory.

The registers access in only 32 bits wide. The frame integrity is verified with a cyclic redundancy check (CRC).

The proxy acknowledges all requests from the host. In case of failure, an error code details the origin.

10.2.2.1. Command

The communication protocol has 5 commands:

- **Read**: Read from a register
- **Write**: Write to a register
- **Load** : Set the registers content from flash memory (user or factory area) (see 10.10.2)
- **Save** : Save the registers content to flash memory (user area)

- **Restore** : Restore a user flash memory from the factory area

10.2.2.2. Request Frame

The request frame structure is defined as following:

Field	Start of frame	Command Id	Address	Data (optional)	CRC16
Field size (byte)	1	1	4	4	2

CRC details and calculations are available in **[AD 2]**

The frame size depends on the command as following:

Table 5. Request frame

Command	**Start of frame**	**Command id**	**Address**	**Data**	**CRC**	**Frame size**
Write	“@” (0x40)	0x99	ADDR	DATA	CRC16	12
Read	“@” (0x40)	0x90	ADDR	None	CRC16	8
Load	“@” (0x40)	0xA0	INDEX	None	CRC16	8
Save	“@” (0x40)	0xA8	INDEX	None	CRC16	8
Restore	“@” (0x40)	0xB0	INDEX	None	CRC16	8

Note:

- All field are transmitted MSB first.
- All field are binary data
- CRC is computed according to **[AD 2]** and transmitted MSB first (instead of LSB first on MODBUS).
- CRC is computed on fields SOF, Command, Address and Data

10.2.2.3. Answer Frame

The answer frame structure is defined as below:

Field	Start of frame	Command Id	Data	CRC16
Field size (byte)	1	1	4	2

Each request is acknowledged by the board with either:

- ACK : request succeeded, a data is returned if relevant
- NACK : request failed, the error code is returned

Table 6. Answer frame

Command	**Start of frame**	**Command id**	**Data**	**CRC**	**Frame size**
ACK	“@” (0x40)	0x80	DATA	CRC16	8
NACK	“@” (0x40)	0x88	Error code	CRC16	8

Note:

- All field are transmitted MSB first.
- All field are binary data
- CRC is computed on fields SOF, Command and Data

In case of error one the following error code is returned:

Table 7. Protocol error codes

Code	Meaning	Description
0x00	No error	No error
0x01	CRC error	CRC check of request frame failed
0x02	Command Id error	Command Id not available
0x03	Address error	Address not available
0x04	Access error	Read or write access not available at the specified address
0x05	Permission error	Specified access and address need administrator privilege
0x06	Parameter range error	Out of range of parameter, invalid parameter
0x07	Timeout error	Communication timeout (e.g. with the cooler)
Others	Internal error	*Please contact support in this case*

10.2.2.4. CRC Computation

Typical exchanges are presented below:

1. Host reads address 0x98, / board answers of 0x1699E

System request							
0x40	0x90	0x00	0x00	0x00	0x98	0x6C	0xCF
SOF	*Cmd*	*Address*				*CRC*	

Board answer							
0x40	0x80	0x00	0x01	0x69	0x9E	0x3D	0xF1
SOF	*Cmd*	*Data*				*CRC*	

2. Host writes 0x012345 at 0x98, board answer with acknowledgement ACK

System request											
0x40	0x99	0x00	0x00	0x00	0x98	0x00	0x01	0x23	0x45	0x5A	0x1C
SOF	*Cmd*	*Address*				*Data*				*CRC*	

Board answer							
0x40	0x80	0x00	0x00	0x00	0x00	0x05	0x0F
SOF	*Cmd*	*Data*				*CRC*	

3. Save registers data to flash user data 1

System request							
0x40	0xA8	0x00	0x00	0x00	0x01	0xC3	0xAE
SOF	*Cmd*	*Address*				*CRC*	

Board answer							
0x40	0x80	0x00	0x00	0x00	0x00	0x05	0x0F
SOF	*Cmd*	*Data*				*CRC*	

10.2.3. Frame Sequence

The electronic board is ready to receive the first request from the system at the end of the board startup.

The requests shall be sent in sequence and the system shall wait for the answer from the board before sending a new command.

In case of corrupted transmission :

- receiver ignores any frame not starting with SOF (@)
- returns an error as soon it is able to identify one (unknown command, invalid CRC)

10.2.4. Response Time

The board has been designed to answer quickly to both read and write requests.

Write access may returns before the requested action takes place when this one depends also on other event or state : POWER_CTRL, CLK_CTRL, SYNC_CTRL, FSYNC_RESYNC_CNT, VIDEO_CTRL, UART_SPEED registers postpone some computation after the answer emission.

Some results may be checked with CCE_STATUS. Detector parameters like INT_TIME, FPA_CONF or window coordinates are forwarded to the detector synchronously to the readout.

Warning: It is not guarantee that a register update will be applied to the next frame, especially when the frame period is close to the board response time.

To control precisely the integration time and frame period, the frame synchonization input FSYNCIN shall be used (see section *Section 10.3.5, "Frame Synchronization"*).

Cooler parameters have a longer response that sum proxy board and cooler driver response time.

10.3. Clock and Synchronization

10.3.1. External Synchronization Signals

The following inputs can be optionally used to synchronise the board with the host system.

Table 8. External synchronization signals

Connector Pin	Signal Name	Description
J1.CC3	RESET_N	Differential asynchronous reset input (active low)
J1.CC1	FSYNCIN	External Frame / integration synchronisation input
J1.CC2	DCLKIN	External clock input

10.3.2. Reset

A power-up reset is internally generated when the main power supply is applied.

The asynchronous input J1.CC3 allows the host to reset the board. These signals are active low and can be left floating if not used.

A reset event restarts the board and loads the settings from the flash memory user 1.

10.3.3. Clock

The board has two exclusive clock sources selected with CLK_SRC.

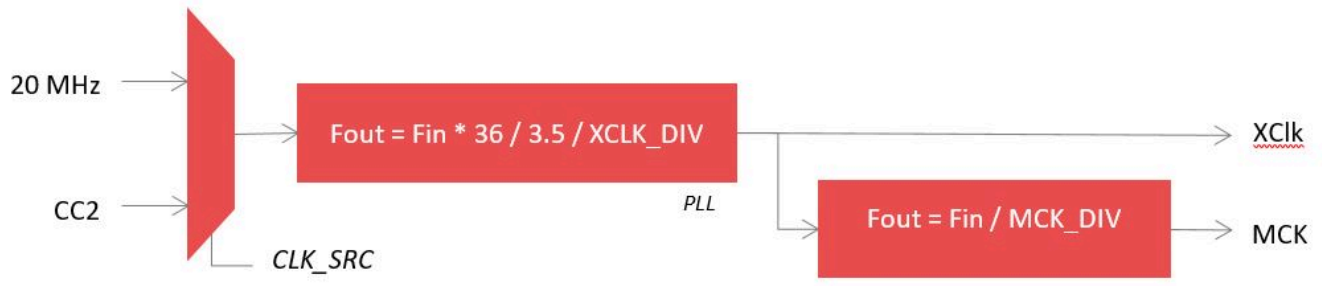
- An internal oscillator of frequency 20 MHz
- The external clock input J1.CC2 (DCLKIN)

The processor has its own oscillator and handles host communication whatever the video clock source is.

10.3.3.1. Video Path Clock Tree

The Camera Link XClk and detector MCK clocks are generated from the main clock source as illustrated in *Figure 10, "Video path clock tree"* Their frequencies are adjusted with XCLK_DIV and MCK_DIV fields of CLK_CTRL register.

Figure 10. Video path clock tree



Updating the clock source or XCLK_DIV unlocks the PLL whereas MCK_DIV update does not. The update request returns before the PLL locks. The user shall check the end of locking process by pooling PLL_LOCKED bit of CCE_STATUS register before going further.

The PLL shall be locked to operate the FPA and video stream output.

10.3.4. Internal Clock Source

Table 9, "MCK and XClk frequencies" summarizes the Camera Link and detector frequencies for several divisor combinations assuming the internal oscillator as clock source.

Table 9. MCK and XClk frequencies

MCK (MHz)		XCLK_DIV						
		4	5	6	7	8	9	10
MCK_DIV	2				14.69	12.86	11.43	10.29
	4	12.86	10.29	8.57	7.35	6.43	5.71	5.14
	8	6.43	5.14	4.29	3.67	3.21	2.86	2.57

	XCLK_DIV						
	4	5	6	7	8	9	10
Xclk (MHz)	51.43	41.14	34.29	29.39	25.71	22.86	20.57

Note:

- MCK frequencies higher than 14.69 MHz or lower than 5.14 MHz are not recommended.
- Above MCK=10.29MHz performance degradation may be observed.
- Typical Camera Link receiver needs an XClk frequency higher than 20 MHz.
- MCK_DIV=2 is forbidden in 4 video channels mode

Table 10, "Maximal frame rates in 2 video channels mode" summarizes the maximum frame rate for the previous configurations and a frame size of 640x512 pixels.

Table 10. Maximal frame rates in 2 video channels mode

Frame rate (Fps)		XCLK_DIV						
		4	5	6	7	8	9	10
MCK_DIV	2				87.6	76.7	68.2	61.5
	4	76.7	61.5	51.3	44.0	38.5	34.2	30.8
	8	38.5	30.8	25.7	22.0	19.3	17.1	15.4

Table 11. Maximal frame rates in 4 video channels mode

Frame rate (Fps)		XCLK_DIV						
		4	5	6	7	8	9	10
MCK_DIV	2	**Not Allowed in 4 video channels mode**						
	4	150.5	120.7	100.8	86.5	75.8	67.4	60.7
	8	75.8	60.7	50.6	43.4	38.0	33.8	30.4

10.3.4.1. External Clock Source

With an external clock source the Camera Link XClk and detector frequencies are defined as following, with F_DCLKIN the external clock frequency:

- F_XCLK = F_DCLKIN * 36 / 3.5 / XCLK_DIV
- F_MCK = F_XCLK / MCK_DIV

Note:

- Xclk frequency should never exceed 51.43 MHz.
- MCK frequencies higher than 14.69 MHz or lower than 5.14 MHz are not recommended.
- Above MCK=10.29 MHz performance degradation may be observed.

10.3.4.2. Detector Clock Constraint

The number of detector video channels (FOUR_OUT) limits the MCK_DIV parameters according to *Table 12, "MCK_DIV constraint"*.

The user shall u pdate FPA_CONF and CLK_CTRL registers in order such as configuration FOUR_OUT=1 and MCK_DIV=2 is never selected otherwise the PARAMETER_RANGE_ERROR will be returned.

Table 12. MCK_DIV constraint

FOUR_OUT	Allowed MCK_DIV
0 (2 channels)	2, 4, 8
1 (4 channels)	4, 8

10.3.5. Frame Synchronization

The frame synchronization is closely linked to the detector integration synchronization.

10.3.5.1. Integration Mode

The integration start and duration settings depend on the selected integration mode.

Table 13. Integration mode

Mode	Integration start	Integration time
Internal	Free-running with period defined by integration period register INT_PERIOD	Defined by integration time register
External trigger	Triggered by external signal FSYNCIN rising edge	Defined by integration time register
External (full)	Triggered by external signal FSYNCIN rising edge	Defined by the external signal FSYNCIN high time

10.3.5.2. FSYNCIN Signal Resynchronization

In the configuration with internal clock source and external frame synchronization, the jitter of the external signal may disturb the video signal if integration starts during the video readout (i.e. in Integrate While Read).

The issue is induced by a coupling between integration and video readout that doesn't start at the same pixel due to jitter. Host image processing like non uniformity correction may apply wrong correction close to the pixel when integration starts.

To overcome this issue, a resynchronization of the FSYNCIN input can be enabled with FSYNC_RESYNC bit of register SYNC_CTRL. Integration will then start during the line dead time next to the FSYNCIN rising edge (see *Table 16, "Camera Link Video Timing for Ncol=640, Nout=2"*).

Robustness of the resynchronization depends on the frame period, integration time and jitter of the external synchronization signal. If the rising edge of the external synchronization is too close to the end of the line, the resynchronization may be postponed to the next line and may produce artifact due to non-uniformity correction.

The FSYNC_RESYNC_CNT register gives the delay between rising edge of the external synchronization and the end of the line. To ensure sufficient margin, the delay should be kept around 1/4 of the width of the current frame. To adjust the value, and with a defined frame period, adjust slightly the integration time.

Enabling FSYNCIN resynchronization may slightly reduce the maximum frame rate by arround 0.5 Fps.

10.4. Video Output

The video stream is provided to the host system through the Camera Link video channel.

10.4.1. Camera Link Mode and Signals

The Camera Link is set in "base mode" configuration. In this mode, 5 LVDS pairs are used to transmit the video signal.

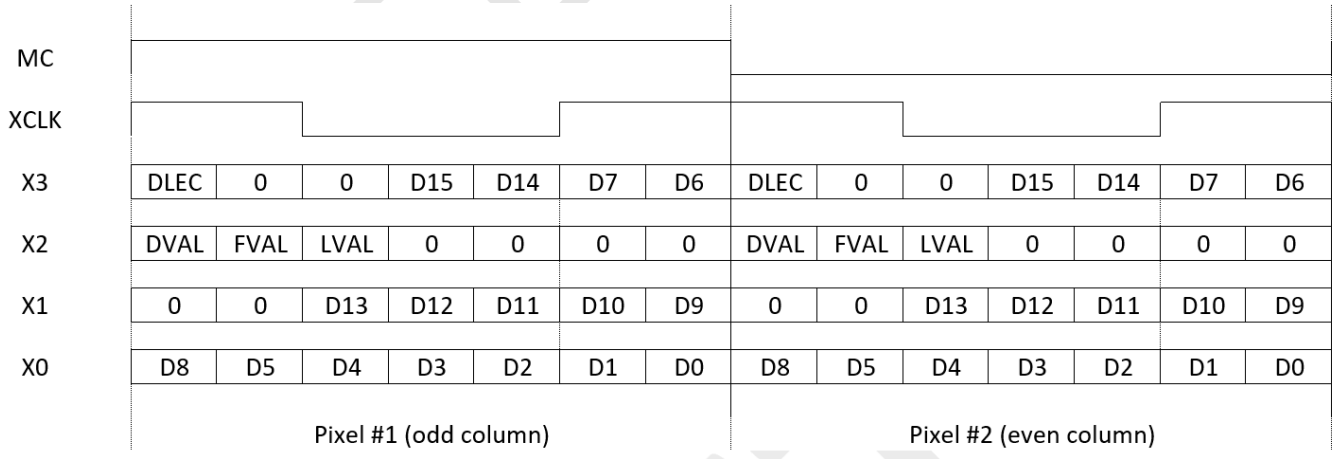
Table 14. Cameralink video signals

Connector Pin	Signal Name	Description
J1.X0	X0	Video data
J1.X1	X1	Video data
J1.X2	X2	Video control (line valid, frame valid and data valid)
J1.X3	X3	Video data
J1.XCLK	XCLK	Clock of channel X

10.4.2. Bit Assignment

Figure 10 defines the multiplex of the video data in the base mode configuration and with MCK_DIV=2.

Figure 11. Camera Link Video Bit Assignment



Note:

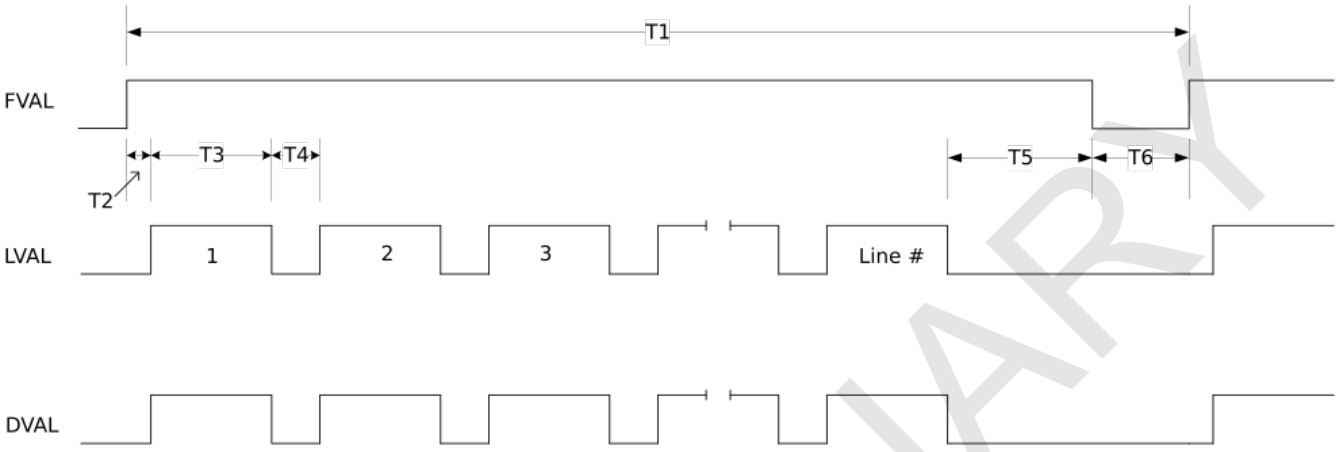
- Columns are count from 1 to 640.
- Video data are transmitted with D[15..0] bits.
- The board has 14 effective bits left aligned. D1 and D0 are fixed to 0.

- DLEC is reserved for future use.

10.4.3. Video Signal Timing

The Camera Link standard defines 3 synchronization signals FVAL, LVAL and DVAL shown in *Figure 12, "Camera Link Video Timing"*. In our case LVAL and DVAL are identical.

Figure 12. Camera Link Video Timing



The parameters T1 to T6 depend on frame rate, frame size and MCK_ DIV as detailed in *Table 15, "Camera Link Video Timing"*.

Table 15. Camera Link Video Timing

Item	Description	Value	Unit
T1	Frame period	INT_PERIOD x MCK period or FSYNCIN period[1]	s
T2	FVAL high to LVAL high	$Ncol^3$*(MCK_DIV/$Nout^2$-1) + 4*MCK_DIV	XClk period
T3	LVAL high time – Line duration	$Ncol^3$	
T4	LVAL low time – Line dead-time	$Ncol^3$*(MCK_DIV/$Nout^2$-1) + 4*MCK_DIV	
T5	Last falling edge LVAL to FVAL low	4	
T6	FVAL low time	T1-[T2+$Nline^4$*T3+($Nline^4$-1)*T4+T5]	

1. Depend on integration mode
2. Number of video channels
3. Number of columns
4. Number of lines

Ncol = Number of columns; Nline = Number of lines; Nout = Number of video channels ; (*): Depend on integration mode

Note: MCK_DIV ≥ Nout is mandatory!

Table 16. Camera Link Video Timing for Ncol=640, Nout=2

Item	Description	MCK_DIV = 2	MCK_DIV = 4	MCK_DIV = 8	Unit
T1	Frame period	INT_PERIOD x MCK period or FSYNCIN period (Note1)			s
T2	FVAL high to LVAL high	8	656	1952	XClk period
T3	LVAL high time – Line duration	640			
T4	LVAL low time – Line dead-time	8	656	1952	
T5	Last falling edge LVAL to FVAL low	4	4	4	
T6	FVAL low time	T1-[T2+Nline*T3+(Nline-1)*T4+T5]			

10.4.4. Video Path Delay

The delay between FSYNCIN rising edge to FVAL rising edge when integration mode is external (trigger or full) is defined in *Table 17, "FSYNCIN to FVAL delay"*. This value depends on the FSYNCIN resynchronization, see *Section 10.3.5.2, "FSYNCIN Signal Resynchronization "*, *Figure 13, "Video path delay without FSYNCIN resynchronization"* and *Figure 14, "Video path delay with FSYNCIN resynchronization"*.

*Table 18, "FSYNCIN to Detector integration delay"*summerizes the delay between external FSYNCIN rising edge and detector integration.

Figure 13. Video path delay without FSYNCIN resynchronization

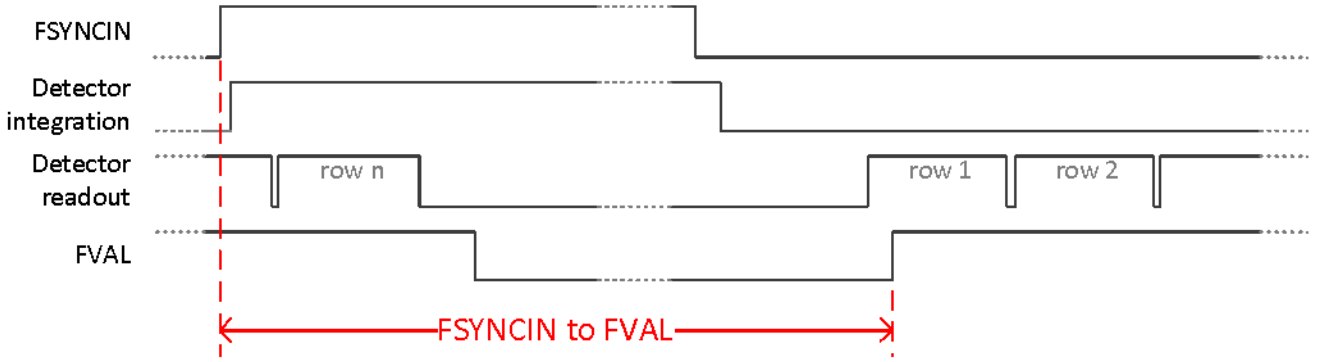


Figure 14. Video path delay with FSYNCIN resynchronization

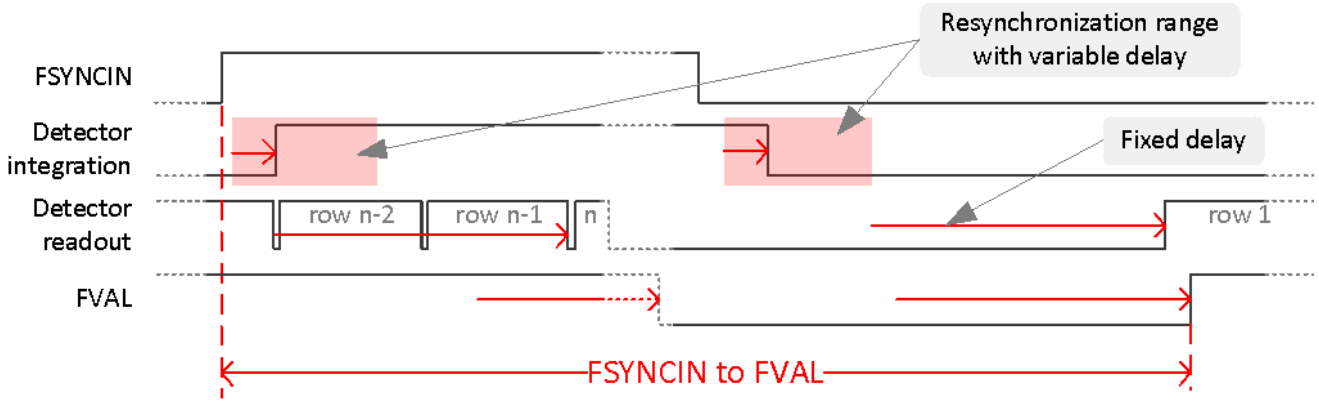


Table 17. FSYNCIN to FVAL delay

Integration mode	FSYNCIN resynchronization	FSYNCIN to FVAL delay (*)	Unit
External trigger	Off	[INT_TIME + (Ncol-1)/Nout + 37] * MCK_DIV + 17	Xclk period
External trigger	On	[INT_TIME + (Ncol-1)/Nout + Ncol + 42] * MCK_DIV + 17	
External	Off	FSYNCIN high time + [(Ncol-1)/Nout + 34] * MCK_DIV + 17	
External	On	FSYNCIN high time + [(Ncol-1)/Nout + NCol + 39] * MCK_DIV + 17	

(*) Measured values may differ slightly due to clock domain crossing uncertainty.

Table 18. FSYNCIN to Detector integration delay

Integration mode	FSYNCIN resynchronization	FSYNCIN to Detector integration delay (*)	Unit
External trigger	Off	8	MCK period
External trigger	On	13 to 13 + Ncol/Nout	
External	Off	5	
External	On	10 to 10 + Ncol/Nout	

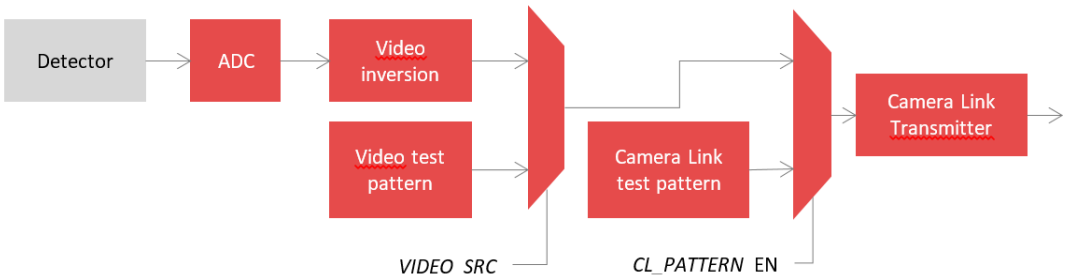
(*) Measured values may differ slightly due to clock domain crossing uncertainty

FSYNCIN to Detector integration delay

10.5. Video Path

The detector video crosses the proximity board through a path illustrated in *Figure 15, "Video Path Diagram"*.

Figure 15. Video Path Diagram



The source of Camera Link video stream is selected between two main sources: the ADC signal or the video test pattern. An additional Camera Link test pattern can generate custom data stream for receiver design purpose.

10.5.1. Video Source Control

The source of the video is controlled by register. The content of the video depends on VIDEO_SRC, FPA_ON fields and FPA temperature. For some sources, the board will switch automatically to the detector output if the FPA temperature is below the FPA temperature threshold FPA_TEMP_THRESHOLD and detector powering is allowed with FPA_ON bit (see *Table 19, "Video Sources Description"*).

Table 19. Video Sources Description

Sources (VIDEO_SRC)	Video Stream Content (hot detector OR FPA_ON unset)	Video stream Content (cold detector AND FPA_ON set)
Detector	“cold” value	Detector video
Test Pattern	Video test pattern	Video test pattern
Automatic	Video test pattern	Detector video
ADC raw	ADC input (Noise, floating level)	Detector video

Note:

- The cold value depends on video inversion:
  - Video not inverted : cold value = 0x0000
  - Video inverted : cold value = 0x3FFF

10.5.2. Detector Video Channel Number

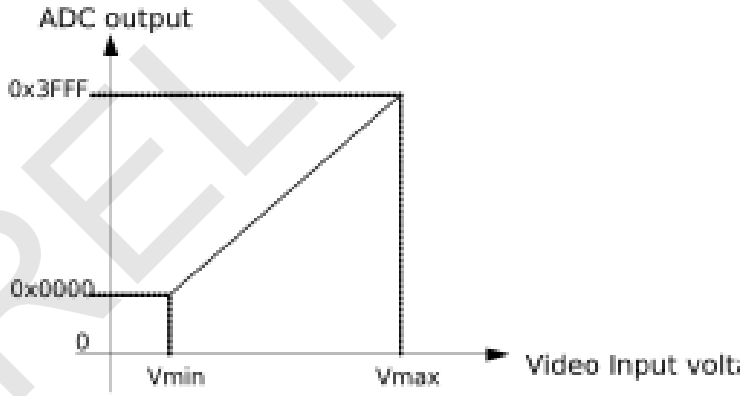
The FPA video output can be configured within 2 or 4 channels using bit FOUR_OUT. 4 channels mode allows the maximum frame rate whereas 2 channels mode lowers the FPA dissipation and thus the over hole power consumption.

The maximal rate of the detector video output constraints both frequency and number of video channels, see section 10.3.3.4 for details

10.5.3. Video Analog to Digital Conversion

The analog video signal from the detector in the range Vmin to Vmax is converted into a 14 bit unsigned value as illustrated in *Figure 16, “Analog Video to Digital Output Conversion”*.

Figure 16. Analog Video to Digital Output Conversion



Note:

- The 14 effective bits are left-shifted in the 16 bit word of Camera Link content. The Camera Link range is then 0x0000 to 0xFFFC with an ADC LSB = 0x0004

10.5.4. Video Inversion

The detector signal can be inverted to have a black or a white cold image:

- Inversion disabled : black cold, cold pixel value = 0x0000 (14 bits), (cameralink 16 bits value = 0x0000)
- Inversion enabled : white cold, cold pixel value = 0x3FFF (14 bits), (cameralink 16 bits value = 0xFFFC)

10.5.5. Video Test Pattern

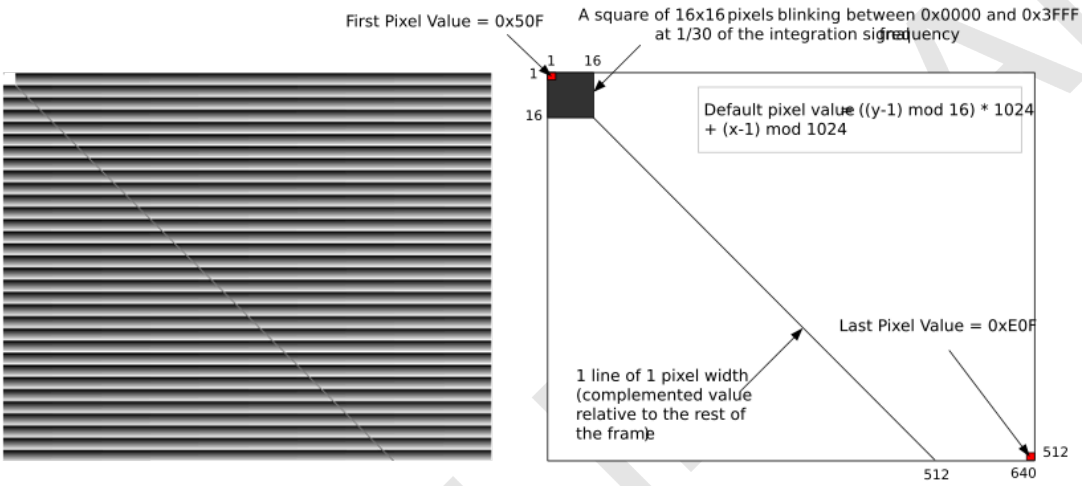
The video test pattern is a video frame (see *Figure 17, "Video Test Pattern Content"*) transmitted in the 14 most significant bits D2 to D15. D1 and D0 are set to 0.

The video test pattern repeats 16 lines of different grey levels. The number of repetitions depends on the size of the frame. An oblique line of one pixel width, with complemented value regarding the rest of the frame, crosses the pattern at 45°.

This video test pattern is enabled by register.

This test pattern is useful to check the video acquisition system.

Figure 17. Video Test Pattern Content



In random windowing, the test pattern is cropped from the full resolution test pattern with :

- Pixel (1,1) located at the top left of the window
- Test pattern content identical to the full frame definition (with less rows and/or columns)
- First and last pixel still have values 0x50F (first pixel) and 0xE0F (last pixel).

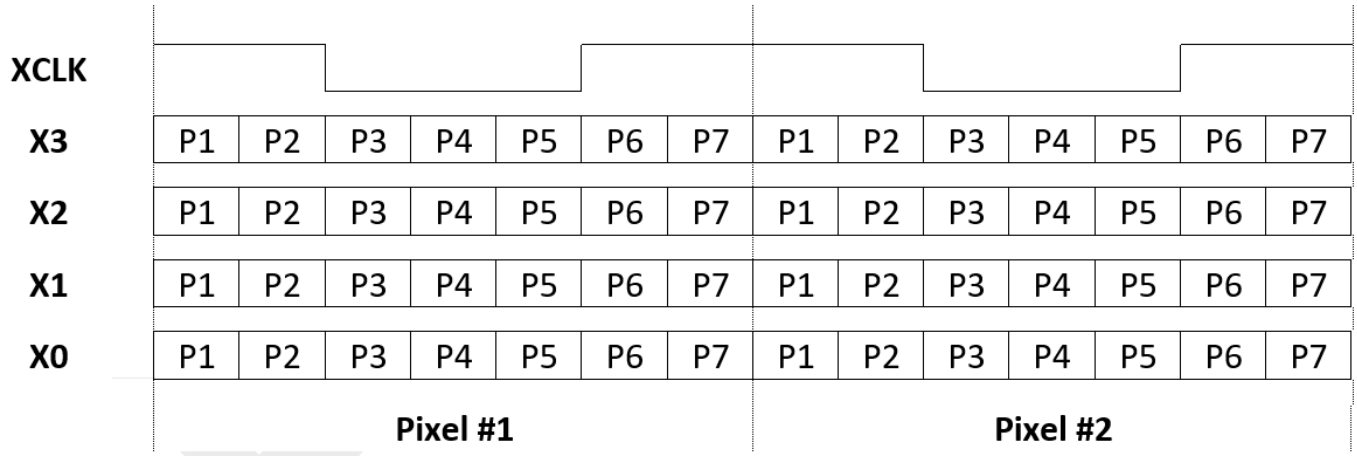
10.5.6. Camera Link Test Pattern

The Camera Link test pattern is a custom data stream used for hardware test purpose. In this case no video synchronization signals like FVAL, LVAL or DVAL are available and no image can be expected.

The Camera Link test pattern is enabled and set by register.

This test pattern is useful for tuning the Camera Link receiver and checking the synchronization of the data bits sampling and clock Xclk.

Figure 18. Camera Link Test Pattern Content



10.5.7. Windowing

The frame size is selected with the WINDOW_MODE field of FPA_CONF register. In case of custom size (“random” mode) the coordinates are defined by CMIN, CMAX, RMIN, RMAX registers. The size is applied on both detector and video pattern.

To avoid transient frame size in random mode, the new coordinates are applied only after a write access to RMAX register, even if RMAX stays unchanged. By setting RMAX lastly, the sequential update of the CMIN, CMAX and RMIN will not generate transient frame size.

The *Table 20, “Window Coordinates Constraints”* presents the constraints required by the detector. A range check is done after the individual coordinate update and the result is available in the acknowledge answer of the write access. The constraints that combine several coordinates are evaluated after the RMAX write access and the result is available in the WINDOW ERROR bits and SERDAT_ERROR of CCE_STATUS register.

WINDOWS_ERROR is always available whereas SERDAT_ERROR is meaningful only when the FPA is powered.

Table 20. Window Coordinates Constraints

Constraint	Check Update	Error Status Reported by
1≤ Cmin ≤ 640 Cmin mod 4 = 1	CMIN register write	Access acknowledge with *Parameter error*
1≤ Cmax ≤ 640 Cmax mod 4 = 0	CMAX register write	Access acknowledge with *Parameter error*
Cmin ≤ Cmax Cmax – Cmin + 1 ≥ 160	RMAX register write	WINDOW_ERROR / SERDAT_ERROR in CCE_STATUS
1≤ Rmin ≤ 512 Rmin mod 2 = 1	RMIN register write	Access acknowledge with *Parameter error*
1≤ Rmax ≤ 512 Rmax mod 2 = 0	RMAX register write	Access acknowledge with *Parameter error*
Rmin ≤ Rmax Rmax – Rmin + 1 ≥ 2	RMAX register write	WINDOW_ERROR / SERDAT_ERROR in CCE_STATUS

10.6. FPA Temperature Measurement

The board monitors the FPA temperature using a diode located close to the FPA. This diode is biased with a constant current and the corresponding temperature is periodically measured and available in register FPA_TEMP.

A second diode close to the FPA is dedicated to the cooler driver.

10.6.1. Measurement

The measurement of the FPA temperature has a dedicated ADC with following timings:

- Update rate = 12.3579 Hz / 8 ~ 1.545 Hz (647 ms)

- Filter type: moving average on last 4 samples

- Filter initialization: first sample

10.6.2. Sensor integrity

The sensor integrity is monitored. Any diode voltage outside a safety range is detected as a failure. In case of failure, the returned temperature is forced to the unrealistic 500K value and bit FPA_TEMP_ERROR of regiser BIT_STATUS is set.

The valid diode voltage range is 0.2 to 1.14 V, bounds included.

10.7. Power Management

The **POWER_CTRL** register controls the power management of the proxy board and the cooler driver to adjust the overall power consumption. The configurations are defined in *Table 21, "Board Power Management States"*.

This power state select the cooler set point 1 or 2, whose values are defined in registers COOLER_SETPOINTx.

The detector and cooler powering are also controlled by bits FPA_ON (register VIDEO_CTRL) and COOLER_ON (register COOLER_CTRL). Both POWER_CTRL register and control bit shall be properly set to power-up the detector or the cooler.

In sleep mode, any access to cooler registers will fail with a timeout error. In this mode, the FPA temperature is only measured by the proxy board and availble in FPA_TEMP register.

Table 21. Board Power Management States

Power state	Detector	Video path and output	FPA temperature monitoring	Cooler	Cooler Set point	Cooler Communication	Power Consumption
Normal	Power allowed	On	On	Power allowed	Set point 1	Allowed	Nominal
Low Power	Power allowed	On	On	Power allowed	Set point 2	Allowed	Low 1
Standby	Power Off	Off	On	Power allowed	Set point 2	Allowed	Low 2
Sleep	Power Off	Off	On	Power Off	N/A	Off	Lowest

10.8. Self Diagnostic

10.8.1. Built-in-Test

The board is able to detect a failure of a subsystem. The test is done on demand when reading the BIT_STATUS register. The following items are tested.

Table 22. Built-in-Test Description

Item	BIT_STATUS bit	Test description
FPA temperature sensor	FPA_TEMP_ERROR	Fails if diode voltage is out of range 0.2 to 1.14 V
FPA detector	FPA_DATAVALID_ERROR	Fails if detector DATAVALID signal is not toggling
Video chain	VIDEO_VGREY_ERROR	Fails if video line blanking value of first rows is out of range
FPA power supplies	VDD_ERROR VDDA_VDDO_ERROR	Fails if DC/DC converters supplying ROIC has an issue

Flash memory	FACTORY_FLASH_CRC_ERROR USER_FLASH_1_CRC_ERROR USER_FLASH_2_CRC_ERROR CAL_FLASH_CRC_ERROR	Fails if the integrity of the settings in flash memory is not guarantee
EEPROM memory	EEPROM_CRC_ERROR	Fails if the integrity of the logging data in EEPROM memory is not guarantee
Main power supply	PSYS_ERROR	Fails if the main power supply (of J1 connector) if out of range
Internal power supplies	P4V4_ERROR P3V3_ERROR P2V5_ERROR P1V8_ERROR P1V2_ERROR AP2V5_VOLTAGE	Fails if an internal power supply is out of range
Cooler	COOLER_INIT_ERROR	Fails if cooler driver parameters was not updated at power-up or after loading a configuration

10.8.2. Diagnostic Led

A led is located on top of the proxy board. It should never light or blink otherwise this indicates a failure during board start-up. In this case contact the support.

10.8.3. Watchdog

The board has a watchdog timer periodically reloaded by the software. In case of software failure or loss of FPGA bitstream, the watchdog will reset the processor and the bootloader will not start the application. The diagnostic led will blink indicating the error code 2 and bootloader will wait any communication request from the host.

Power cycling the board will clear the watchdog event and will restart the application. Watchdog reset should never happen. It case of such failure, contact the customer support.

Note:

- Poor board power supply (low voltage, long wires…) may lead to a loss of FPGA bitstream when the ROIC is powered-up.

10.9. Logging

The board logs the following parameters accessible to the user. Theses counters are initialized during manufacturing and cannot be reset by the user.

10.9.1. Ambient Temperature

The ambient temperature is estimated with an onboard sensor. Its maximal and minimal values are logged in AMBIENT_MIN/MAX registers.

10.9.2. Operating Time Histogram

The operating time is recorded as a function of the ambient temperature to form a histogram. Values are available in OPTIME_x registers. Theses counters are updated when the board is running regardless of power management mode.

10.9.3. Cooldown

The number of cooldown, defined by crossing the FPA temperature threshold from a high to low value, is logged in COOLDOWN_CNT register.

The cooled time, defined by the accumulated time with a FPA temperature under the temperature threshold, is logged in COOLED_TIME register.

Cooldown and cooled state are not affected by reloading the configuration from the flash, enabling/disabling the detector power nor changing the power management mode.

10.10. Board State Diagram

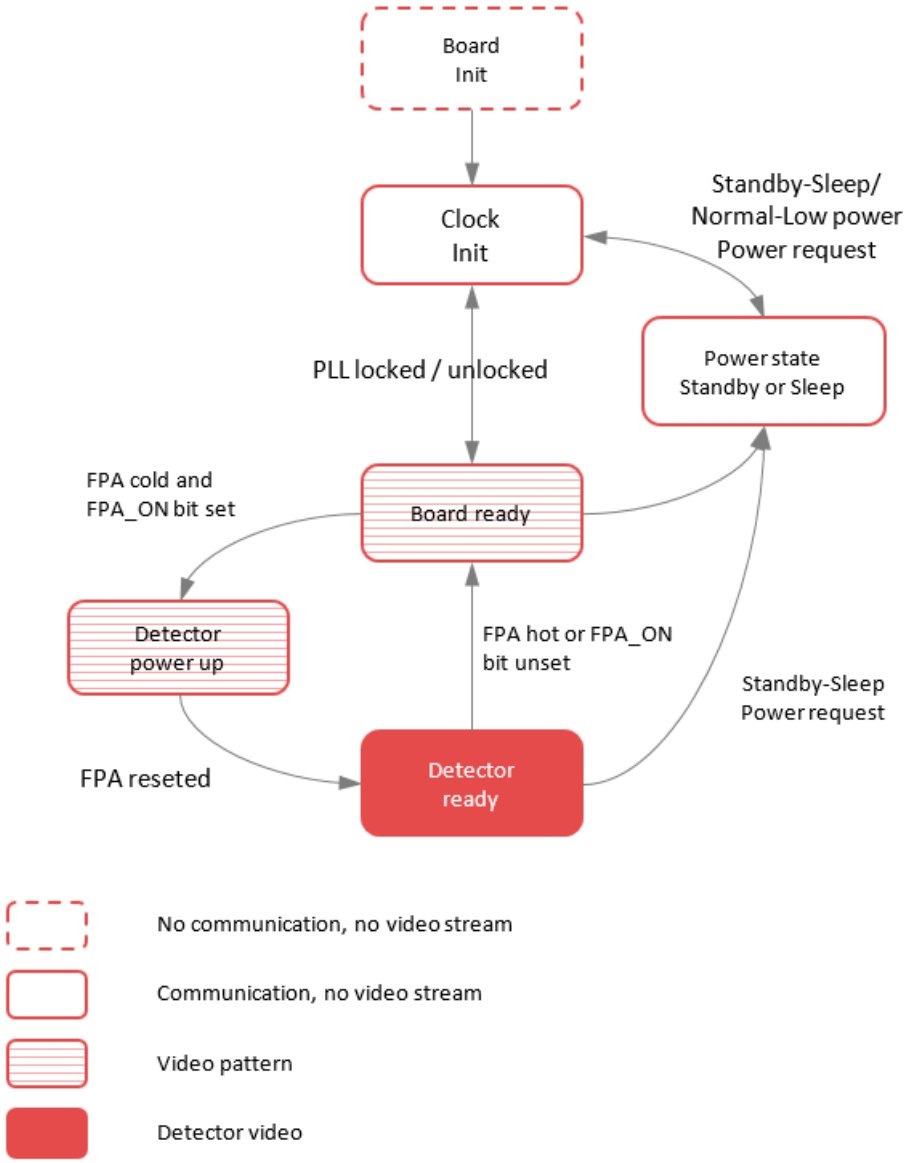
Figure 18 summarizes the main states and transitions of the board and detector according to:

- Main clock source availability
- Power management control
- FPA temperature

The video source is assumed set to “Automatic”.

The bit DETECTOR_READY is set when the board is in “detector ready” state.

Figure 19. Board state diagram



10.11. Cooler

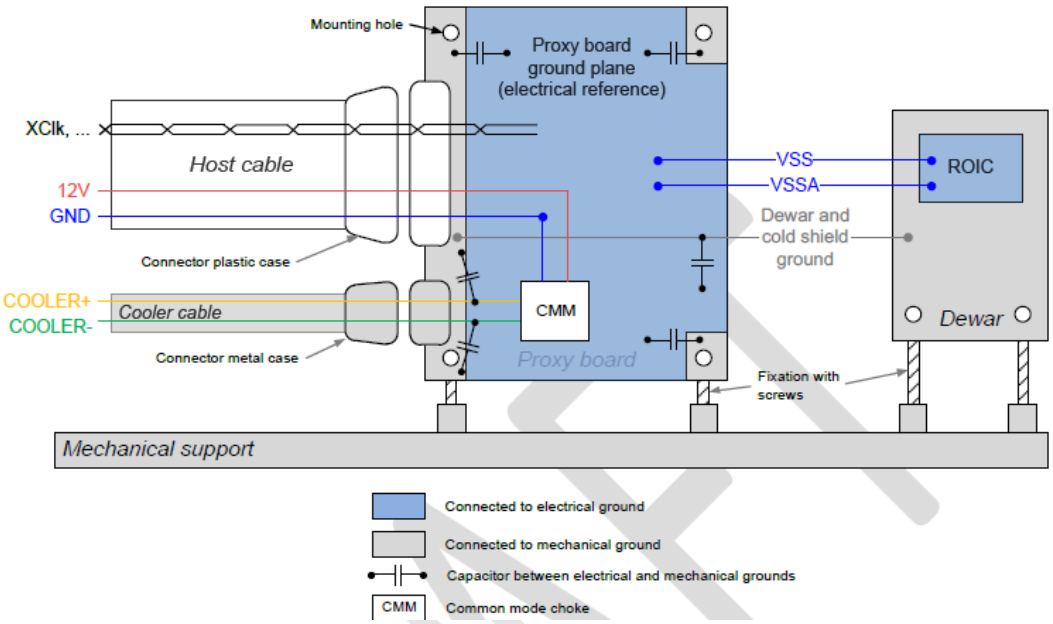
The proxy board control the cooler driver (temperature stepoints, status etc …)

10.12. Grounds Connection

Parameter	Condition / Comment	Min.	Typ.	Max.	Units
Insulation Resistance	Between Electrical and mechanical ground, under 50VDC	100	--	--	MOhm

The electrical and mechanical grounds are connected together though several capacitors of 10 nF distributed near each fixation point.

Figure 20. Grounds connection



10.13. Settings registers

The proximity board is controlled by reading and writing registers. Their content is lost at power-off.

10.13.1. Registers Access and Permission

All registers are 32 bits aligned and stored in little-endian format such that LSByte has the lowest address.

Registers have an access property (“Acc.” column of detailed description):

- R : read only
- W : write only
- RW : read / write

Registers have also a protection property (“Pro.” column of detailed description)

- N : not protected
- WP : write is protected (read is not protected if relevant)

Protected access is only allowed in administrator mode.

10.13.2. Registers Backup, Flash Transfers

The registers content can be saved into a non-volatile flash memory. 3 areas are available and identified by an index:

Table 23. Flash area index

Index	Description	User access
0	Factory area	Read-only
1	User area 1 (register default at reset)	Read / write
2	User area 2	Read / write

The integrity of the 3 areas is check at power-up and available in **BIT_STATUS** register.

The protocol commands have an index parameter to select the flash area. User can store two different configurations.

The *Table 24, "Flash transfers by protocol"*and*Figure 21, " Available transfers between registers and flash"* summarize the available transfers.

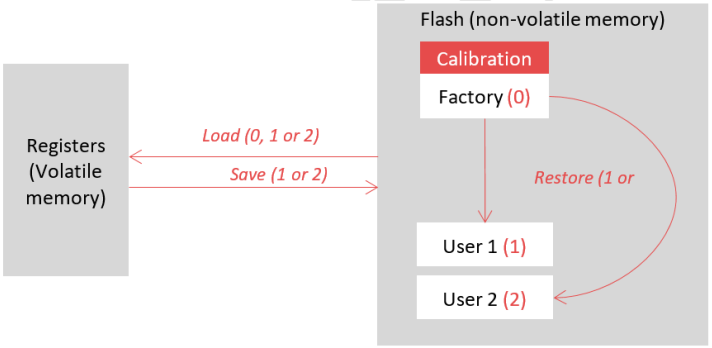
Table 24. Flash transfers by protocol

Protocol	Command	Register to user flash	User flash to register	Factory flash to register	Factory flash to user flash
32 bits	Load		X	X	
32 bits	Save	X			
32 bits	Restore				X

Note:

- Factory data used in load and restore operations are default values of FACT_SET_REF settings set customized with calibration results proper to each detector and stored in calibration area.

Figure 21. Available transfers between registers and flash



10.13.3. Registers Initialization

After the power-up or a reset, the registers are initialized with the content of user area 1.

In case of user area 1 integrity failure, the factory area is loaded (see *Section 10.13.2, "Registers Backup, Flash Transfers"*). In case of factory area integrity failure, default settings of the firmware are loaded.

10.13.4. Factory default value

See the sbf programming file release note for up-to-date values according to factory settings reference number.

Please refer to *Table 25, "Registers mapping"* for register description

Chapter 11. Product identification

11.1. IDDCA Labelling

Please refer to product specification **[AD 5]**

11.2. Proximity board Labelling

Following informations are available on proximity board labelling :

- Article reference
- Revision
- Serial number

Chapter 12. General Handling Procedure

12.1. Introduction

All components (proximity board, dewar, cooler compressor and cooler board) need to be manipulated with precautions, due to the associated risks to damage them. Especially, cold pipe of cooler (between compressor and cold head) is sensitive to handling.

12.2. Packaging

The package is not designed to guarantee long duration storage of the content. It is therefore of the user responsibility to ensure the unpacking and the correct storage conditions (see below).

12.3. Storage

12.3.1. Short duration storage

For short term storage if waiting for system integration, the whole IDDCA can be left in its transportation box for some weeks.

Place the transportation box in a humidity-controlled storage area.

Recommended storage temperature: 23°C ± 10°C.

12.3.2. Long duration storage

For long term storage (> several months), the IDDCA should not be left in the transportation box because the foam is not designed for long duration storage.

Unpack the detector from its transportation package within a few weeks after receipt and place it in a humidity-controlled storage area.

Recommended storage temperature: 23°C ± 10°C.

12.4. Cautions for Mechanical Interface

12.4.1. Handling and integration

LYNRED recommends to manipulate products with cleanroom gloves.

LYNRED recommendations regarding regarding optical interfaces handling and cleaning are descrribed in **[AD 3]** (§5.3)

12.5. Cautions for Electrical Interface

12.5.1. Cautions against electrostatic discharges

Such as any electronic component, the IDDCA is sensitive to electrostatic discharges. The following cautions are therefore specified:

- Handling the detector on a static free work station equipped with grounded carpet;
- No handling without properly worn and grounded wrist strap;
- Grounding the electronic equipment before plugging it onto the proximity board.

12.5.2. General electrical precautions

The proximity board is taking care of generating all necessary biases to drive the detector; therefore the customer is not in charge of applying the electrical precautions described in the ICD document of the IDDCA.

The board electrical interface presented in this document shall be respected.

If the recommended bias values are not respected and correctly applied on the I/O of the board, the board could be damaged or destroyed.

Short-circuit the IDDCA connector with proper conductive material when it is disconnected from the board. The specific short-circuit card delivered with the dewar detector assembly shall be kept aside for this purpose.

Chapter 13. APPENDIX

13.1. Registers Mapping and Description

The following table illustrates the register mapping.

Table 25. Registers mapping

Address	Access	Protection	Name
0x000	R	N	BOARD_ID
0x004	R	N	FPGA _VER
0x008	R	N	MCU_VER
0x00C	R	N	CCE_SN
0x010	RW	WP	CCE_REF
0x014	RW	WP	FACT_SET_REF
0x018	R	N	FACT_SET_CRC
0x020	R	N	CCE_STATUS
0x024	RW	N	POWER_CTRL
0x028	RW	N	CLK_CTRL
0x02C	RW	N	SYNC_CTRL
0x030	RW	N	VIDEO_CTRL
0x034	RW	N	UART_SPEED
0x038	RW	N	CL_PATTERN_CTRL
0x040	R	N	BIT_STATUS
0x044	R	N	CCE_PSYS_VOLTAGE
0x048	R	N	CCE_P4V4_VOLTAGE
0x04C	R	N	CCE_P3V3_VOLTAGE
0x050	R	N	CCE_P2V5_VOLTAGE
0x054	R	N	CCE_P1V8_VOLTAGE
0x058	R	N	CCE_P1V2_VOLTAGE
0x05C	R	N	CCE_AP2V5_VOLTAGE
0x060	R	N	PIXEL_CNT
0x070	R	N	FPA_TEMP
0x074	RW	WP	FPA_TEMP_THRESHOLD
0x078	RW	WP	LYNRED RESERVED
0x07C	RW	WP	LYNRED RESERVED
0x080	RW	WP	LYNRED RESERVED
0x084	RW	WP	LYNRED RESERVED
0x088	RW	WP	LYNRED RESERVED
0x08C	R	N	LYNRED RESERVED
0x090	RW	N	GPOL
0x094	RW	N	INT_PERIOD
0x098	RW	N	INT_TIME
0x0B0	RW	N	FPA_CONF
0x0B4	RW	N	FPA_BM
0x0B8	RW	N	FPA_PM

0x0BC	RW	N	LYNRED RESERVED
0x0C0	RW	N	CMIN
0x0C4	RW	N	RMIX
0x0C8	RW	N	CMAX
0x0CC	RW	N	RMAX
0x0D0	R	N	ROIC_ID
0x0D4	R	N	ROIC_ERROR
0x0D8	RW	WP	LYNRED RESERVED
0x0F0	W	N	LYNRED RESERVED
0x100	RW	WP	COOLDOWN_CNT
0x104	RW	WP	COOLED_TIME
0x110	R	N	AMBIENT_TEMP
0x114	RW	WP	AMBIENT_MIN
0x118	RW	WP	AMBIENT_MAX
0x120	RW	WP	OPTIME_M40_M30
0x124	RW	WP	OPTIME_M30_M20
0x128	RW	WP	OPTIME_M20_M10
0x12C	RW	WP	OPTIME_M10_0
0x130	RW	WP	OPTIME_0_P10
0x134	RW	WP	OPTIME_P10_P20
0x138	RW	WP	OPTIME_P20_P30
0x13C	RW	WP	OPTIME_P30_P40
0x140	RW	WP	OPTIME_P40_P50
0x144	RW	WP	OPTIME_P50_P60
0x148	RW	WP	OPTIME_P60_P70
0x14C	RW	WP	OPTIME_P70_P80
0x150	RW	WP	OPTIME_P80_P90
0x154	RW	WP	OPTIME_P90_P100
0x158	RW	WP	OPTIME_P100_P110
0x15C	RW	WP	OPTIME_P110_P125
0x200	R	N	LYNRED RESERVED
0x204	R	N	LYNRED RESERVED
0x208	R	N	LYNRED RESERVED
0x20C	R	N	LYNRED RESERVED
0x210	RW	WP	LYNRED RESERVED
0x240	R	N	FSYNC_RESYNC_CNT
0x250	RW	N	USER_DATA_1
0x254	RW	N	USER_DATA_2
0x258	RW	N	USER_DATA_3
0x25C	RW	N	USER_DATA_4
0x300	RW	WP	LYNRED RESERVED

0x304	RW	WP	LYNRED RESERVED
0x308	RW	WP	LYNRED RESERVED
0x30C	RW	WP	LYNRED RESERVED
0x310	RW	WP	LYNRED RESERVED
0x314	RW	WP	LYNRED RESERVED
0x318	RW	WP	LYNRED RESERVED
0x31C	RW	WP	LYNRED RESERVED
0x320	RW	WP	LYNRED RESERVED
0x324	RW	WP	LYNRED RESERVED
0x328	RW	WP	LYNRED RESERVED
0x32C	RW	WP	LYNRED RESERVED
0x330	RW	WP	CAL_GPOL
0x334	RW	WP	LYNRED RESERVED
0x400	RW	N	COOLER_CTRL
0x404	R	N	LYNRED RESERVED
0x408	W	N	LYNRED RESERVED
0x40C	RW	WP	LYNRED RESERVED
0x410	RW	N	COOLER_SETPOINT_1
0x414	RW	N	COOLER_SETPOINT_2
0x420	RW	WP	LYNRED RESERVED
0x424	RW	WP	LYNRED RESERVED
0x428	RW	WP	LYNRED RESERVED
0x430	RW	N	LYNRED RESERVED
0x434	RW	N	LYNRED RESERVED
0x438	RW	N	LYNRED RESERVED
0x440	RW	WP	LYNRED RESERVED
0x444	RW	N	LYNRED RESERVED
0x450	R	N	COOLER_INT_STATUS
0x454	R	N	LYNRED RESERVED
0x458	R	N	LYNRED RESERVED
0x460	R	N	LYNRED RESERVED
0x464	R	N	LYNRED RESERVED
0x470	R	N	LYNRED RESERVED
0x474	R	N	LYNRED RESERVED
0x480	R	N	LYNRED RESERVED
0x484	R	N	LYNRED RESERVED
0x490	RW	WP	LYNRED RESERVED
0x4A0	R	N	LYNRED RESERVED
0x4A4	R	N	LYNRED RESERVED
0x4A8	R	N	COOLER_SN1
0x4AC	R	N	COOLER_SN2
0xE00	RW	WP	LYNRED RESERVED
0XE10	R	N	LYNRED RESERVED

0XE14	R	N	LYNRED RESERVED
0XE18	R	N	LYNRED RESERVED
0XE1C	R	N	LYNRED RESERVED

BOARD_ID

Address	Name	Acc.	Pro.	Description
0x000	BOARD_ID	R	N	Board identification number

Bits	Field	Description	Value	Unit
[31:0]	BOARD_ID	Board hardware identification number	18 : V1 21 : V2	

FPGA_VER and MCU_VER

Address	Name	Acc.	Pro.	Description
0x004	FPGA_VER	R	N	FPGA version
0x008	MCU_VER	R	N	MCU version

Bits	Field	Description	Value	Unit
[31:0]	FPGA_VER or MCU_VER	FPGA bitstream version or MCU firmware version	4 unsigned integer in the form “F.M.m.p”	

CCE_SN

Address	Name	Acc.	Pro.	Description
0x00C	CCE_SN	R	N	Proxy serial number

Bits	Field	Description	Value	Unit
[31:0]	CCE_SN	Proxy serial number	Unsigned integer	

CCE_REF

Address	Name	Acc.	Pro.	Description
0x010	CCE_REF	RW	WP	Proxy reference number / part number

Bits	Field	Description	Value	Unit
[31:0]	CCE_REF	Proxy reference / part number	ASCII encoded string (little-endian byte order)	

FACT_SET_REF

Address	Name	Acc.	Pro.	Description
0x014	FACT_SET_REF	RW	WP	Factory settings reference

Bits	Field	Description	Value	Unit
[31:0]	FACT_SET_REF	Factory settings reference	ASCII encoded string (little-endian byte order)	

FACT_SET_CRC

Address	Name	Acc.	Pro.	Description
0x018	FACT_SET_CRC	R	N	Factory settings crc

Bits	Field	Description	Value	Unit
[31:0]	FACT_SET_CRC	Factory settings crc	Unsigned integer	

CCE_STATUS

Address	Name	Acc.	Pro.	Description
0x020	CCE_STATUS	R	N	Proxy general status

Bits	Field	Description	Value	Unit
31	DETECTOR_READY	Detector ready status	0: No 1: Yes	
[30:15]	Lynred Reserved	Lynred Reserved	-	
[11:14]	Unused			
[10:9]	POWER_STATE	Power management state	00b: Normal 01b: Low_power 10b: Standby 11b: Sleep	
8	ADMIN_MODE	Administrator mode	0: User 1: Admin	
[7:6]	Unused			
5	WINDOW_ERROR	Window coordinates error	0: None 1: Error	
4	SERDAT_ERROR	Error in ROIC_ERROR register or with the SERDAT signal	0: None 1: Error	
3	FPA_POWERED	FPA power supplied enabled	0: FPA Off 1: FPA On	
2	FPA_TEMP_STABLE	FPA temperature stable	0: Unstable 1: Stable	
1	FPA_TEMP_LOW	FPA temperature under threshold	0: FPA hot 1: FPA cooled	
0	PLL_LOCKED	Pll lock status	0: Unlocked 1: Locked	

POWER_CTRL

Address	Name	Acc.	Pro.	Description
0x024	POWER_CTRL	RW	N	Power management control

Bits	Field	Description	Value	Unit
[31:2]	Unused			
[1:0]	POWER_MODE	Power management mode	00b: Normal 01b: Low power 10b: Standby 11b: Sleep	

CLK_CTRL

Address	Name	Acc.	Pro.	Description
0x028	CLK_CTRL	RW	N	Clock control

Bits	Field	Description	Value	Unit
[15:8]	XCLK_DIV	Camera Link Xclk divisor	Unsigned integer >=5	

		XClk = clk_src * (36/3.5) / XCLK_DIV		
[7:6]	Unused			
[5:4]	MCK_DIV	FPA clock divisor MCK = XClk / MCK_DIV	00b: 2 01b: 4 10b: 8 11b: Unused	
[3:1]	Unused			
0	CLK_SRC	Main clock source (clk_src)	0: Internal (20 MHz) 1: External (DCLKIN)	

Note:

- Update of this register may lead to unlock the PLL and reset of video path and detector. The request answer is returned before the clock is restarted. PLL_LOCKED bit shall be monitored and the locked status must be waited before going further.
- See *Section 10.3.4.2, "Detector Clock Constraint "* for constraint between MCK_DIV and FOUR_OUT fields

SYNC_CTRL

Address	Name	Acc.	Pro.	Description
0x02C	SYNC_CTRL	RW	N	Frame synchronization control

Bits	Field	Description	Value	Unit
[15:5]	Unused			
4	FSYNC_RESYNC	External FSYNCIN signal resynchronization within line blanking	0: Disable 1: Enable	
[3:2]	Unused			
[1:0]	INT_MODE	Integration signal source and mode	00b: Internal 01b: External trig 10b: External (full)	

FSYNC_RESYNC_CNT

Address	Name	Acc.	Pro.	Description
0x240	FSYNC_RESYNC_CNT	R	N	FSYNC rising edge to DATAVALID falling edge delay

Bits	Field	Description	Value	Unit
[8:0]	FSYNC_RESYNC_CNT	FSYNC rising edge to DATAVALID falling edge delay	Unsigned integer	MCK period

VIDEO_CTRL

Address	Name	Acc.	Pro.	Description
0x030	VIDEO_CTRL	RW	N	Video path control

Bits	Field	Description	Value	Unit
[15:4]	Unused			
3	FPA_VIDEO_INV	Black / white video inversion of FPA video signal. (Not applied to video pattern)	0: Disable 1: Enable	
2	FPA_ON	FPA power supplies enable	0: Disable 1: Enable	
[1:0]	VIDEO_SRC	Video source	00b: Detector 01b: Video pattern	

			10b: Automatic 11b: ADC raw	

UART_SPEED

Address	Name	Acc.	Pro.	Description
0x034	UART_SPEED	RW	N	UART speed control

Bits	Field	Description	Value	Unit
[8:3]	Unused	Unused		
[2:0]	UART_SPEED	UART baudrate	000b: 4800 Bd 001b: 9600 Bd 010b: 19200 Bd 011b: 38400 Bd 100b: 57600 Bd 101b: 115200 Bd 110b: 230400 Bd 111b: 460800 Bd	

Note:

- When changing the UART speed, the answer to the request which updates the UART is returned with the old baud rate. The baudrate switch is done after the answer emission.

CL_PATTERN_CTRL

Address	Name	Acc.	Pro.	Description
0x038	CL_PATTERN_CTRL	RW	N	Camera Link pattern control

Bits	Field	Description	Value	Unit
8	Unused	Unused		
7	CL_PATTERN_EN	Camera Link pattern enable	0: Disable 1: Enable	
[6:0]	CL_PATTERN_DATA	Camera Link pattern data [P7 to P1]	Unsigned integer	

BIT_STATUS

Address	Name	Acc.	Pro.	Description
0x040	BIT_STATUS	R	N	Built in test status

Bits	Field	Description	Value	Unit
[31:23]	Unused			
22	AP2V5_ERROR	Internal AP2V5 voltage error	0: None 1: Error	
21	P1V2_ERROR	Internal P1V2 voltage error	0: None 1: Error	
20	P1V8_ERROR	Internal P1V8 voltage error	0: None 1: Error	
19	P2V5_ERROR	Internal P2V5 voltage error	0: None 1: Error	
18	P3V3_ERROR	Internal P3V3 voltage error	0: None 1: Error	
17	P4V4_ERROR	Internal P4V4 voltage error	0: None 1: Error	

16	PSYS_ERROR	External PSYS voltage error	0: None 1: Error	
15	COOLER_INIT_ERROR	Cooler initialization error	0: None 1: Error	
[14:13]	Unused			
12	CAL_FLASH_CRC_ERROR	Wrong calibration flash crc	0: None 1: Error	
11	EEPROM_CRC_ERROR	EEPROM crc error	0: None 1: Error	
10	USER_FLASH_2_CRC_ERROR	Wrong user flash 2 crc	0: None 1: Error	
9	USER_FLASH_1_CRC_ERROR	Wrong user flash 1 crc	0: None 1: Error	
8	FACTORY_FLASH_CRC_ERROR	Wrong factory flash crc	0: None 1: Error	
[7:6]	Unused			
5	VDDA_VDDO_ERROR	FPA VDDA and VDDO supplies error	0: None 1: Error	
4	VDD_ERROR	FPA VDD supply error	0: None 1: Error	
3	Unused			
2	VIDEO_VGREY_ERROR	FPA line blanking vgrey error	0: None 1: Error	
1	DATAVALID_ERROR	FPA Datavalid signal toggling error	0: None 1: Error	
0	FPA_TEMP_ERROR	FPA temperature sensor integrity error	0: None 1: Error	

CCE_x_VOLTAGE

Address	Name	Acc.	Pro.	Description
0x044	CCE_PSYS_VOLTAGE	R	N	Main power supply voltage
0x048	CCE_P4V4_VOLTAGE	R	N	P4V4 supply voltage
0x04C	CCE_P3V3_VOLTAGE	R	N	P3V3 supply voltage
0x050	CCE_P2V5_VOLTAGE	R	N	P2V5 supply voltage
0x054	CCE_P1V8_VOLTAGE	R	N	P1V8 supply voltage
0x058	CCE_P1V2_VOLTAGE	R	N	P1V2 supply voltage
0x05C	CCE_AP2V5_VOLTAGE	R	N	AP2V5 supply voltage

Bits	Field	Description	Value	Unit
[15:0]	xxx_VOLTAGE	xxx supply voltage with xxx = PSYS, P4V4, P3V3, P2V5, P1V8, P1V2, AP2V5	Unsigned integer	mV

PIXEL_CNT

Address	Name	Acc.	Pro.	Description
0x060	PIXEL_CNT	R	N	Pixel counter

Bits	Field	Description	Value	Unit
[23:0]	PIXEL_CNT	Pixel Counter (nb pixels sampled by frame)	Unsigned integer	

FPA_TEMP

Address	Name	Acc.	Pro.	Description
0x070	FPA_TEMP	R	N	FPA Temperature

Bits	Field	Description	Value	Unit
[15:0]	FPA_TEMP	FPA temperature	Unsigned integer	10 mK

FPA_TEMP_THRESHOLD

Address	Name	Acc.	Pro.	Description
0x074	FPA_TEMP_THRESHOLD	RW	WP	FPA Temperature threshold

Bits	Field	Description	Value	Unit
[15:0]	FPA_TEMP_THRESHOLD	FPA temperature threshold	Unsigned integer	10 mK

Note:

- The user can adjust the threshold within the range 130 to 170 K.

GPOL

Address	Name	Acc.	Pro.	Description
0x090	GPOL	RW	N	GPOL bias voltage

Bits	Field	Description	Value	Unit
[15:0]	GPOL	FPA GPOL bias voltage	Unsigned integer 1.5 ≤ value ≤ 3.6V	mV

INT_PERIOD

Address	Name	Acc.	Pro.	Description
0x094	INT_PERIOD	RW	N	Integration / Frame period

Bits	Field	Description	Value	Unit
[23:0]	INT_PERIOD	Integration / frame period (not relevant in external synchronization)	Unsigned integer 1 ≤ value	MCK period

INT_TIME

Address	Name	Acc.	Pro.	Description
0x098	INT_TIME	RW	N	Integration time

Bits	Field	Description	Value	Unit
[23:0]	INT_TIME	Integration time	Unsigned integer 1 ≤ value	MCK period

Note:

- If INT_TIME ≥ INT_PERIOD the video stream will freeze. Sequence the INT_TIME and INT_PERIOD updates such that INT_TIME < INT_PERIOD is always verified.

FPA_CONF

Address	Name	Acc.	Pro.	Description

Address	Name	Acc.	Pro.	Description
0x0B0	FPA_CONF	RW	N	FPA general configuration

Bits	Field	Description	Value	Unit
[15:9]	Unused			
8	Lynred Reserved	Lynred Reserved	1	
[7:6]	WINDOW_MODE	FPA Window mode	00b: 640x512 01b: 512x512 10b: 640x480 11b: Random	
[5]	FOUR_OUT	FPA 4 video outputs enable	0: Disable 1: Enable	
4	Lynred Reserved	Lynred Reserved	0	
3	Lynred Reserved	Lynred Reserved	1	
2	Lynred Reserved	Lynred Reserved	0	
1	INV_ROW	FPA Rows inversion	0: Disable 1: Enable	
0	INV_COL	FPA Columns inversion	0: Disable 1: Enable	

Note:

- See *Section 10.3.4.2, "Detector Clock Constraint "* for constraint between MCK_DIV and FOUR_OUT fields

FPA_BM

Address	Name	Acc.	Pro.	Description
0x0B4	FPA_BM	RW	N	FPA bias management

Bits	Field	Description	Value	Unit
[7:4]	BMGREY	FPA Video grey voltage	0: 1.800 V 1: 1.875 V 2: 1.950 V 3: 2.025 V 4: 2.100 V 5: 2.175 V 6: 2.250 V 7: 2.325 V 8: 2.400 V 9: 2.475 V 10: 2.550 V 11: 2.625 V 12: 2.700 V 13: 2.775 V 14: 2.850 V 15: 2.925 V	
[3:0]	BMAB	FPA Anti blooming voltage	0: 1.800 V 1: 1.875 V 2: 1.950 V 3: 2.025 V 4: 2.100 V 5: 2.175 V 6: 2.250 V 7: 2.325 V 8: 2.400 V	

			9: 2.475 V 10: 2.550 V 11: 2.625 V 12: 2.700 V 13: 2.775 V 14: 2.850 V 15: 3.600 V	

Note:

- A BMGREY value higher than 11 (i.e. 2.625V) will saturate the video input of the proxy.
- If BMGREY satures the video input, VIDEO_VGREY_ERROR status will be incorrect.

FPA_PM

Address	Name	Acc.	Pro.	Description
0x0B8	FPA_PM	RW	N	FPA power management

Bits	Field	Description	Value	Unit
[7:4]	PMOUT	FPA Output amplifiers power mode	0: 0.111 1: 0.222 2: 0.333 3: 0.444 4: 0.556 5: 0.667 6: 0.778 7: 0.889 8: 1.000 9: 1.111 10: 1.222 11: 1.333 12: 1.444 13: 1.556 14: 1.667 15: 1.778	
[3:0]	PMCOL	FPA Column amplifiers power mode	0: 0.25 1: 0.50 2: 0.75 3: 1.00 4: 1.25 5: 1.50 6: 1.75 7: 2.00 8: 2.25 9: 2.50 10: 2.75 11: 3.00 12: 3.25 13: 3.50 14: 3.75 15: 4.00	

CMIN, CMAX, RMIN, RMAX

Address	Name	Acc.	Pro.	Description
0x0C0	CMIN	RW	N	Window column min

0x0C8	CMAX	RW	N	Window column max

Bits	Field	Description	Value	Unit
[15:10]	Unused			
[9:0]	CMIN or CMAX	Window column coordinate (MIN or MAX)	unsigned integer 1≤value≤640	Pixel

Address	Name	Acc.	Pro.	Description
0x0C4	RMIN	RW	N	Window row min
0x0CC	RMAX	RW	N	Window row max

Bits	Field	Description	Value	Unit
[15:10]	Unused			
[9:0]	RMIN or RMAX	Window row coordinate (MIN or MAX)	unsigned integer 1≤value≤512	Pixel

Note:

- Window coordinates are applied after the RMAX register is updated.
- Window coordinates CMIN, CMAX and RMIN are individually checked after their update. The remaining checks, which combine several coordinates, are done after RMAX update.
- To avoid transient frame size or transient check error when changing the window, set RMAX lastly.

ROIC_ID

Address	Name	Acc.	Pro.	Description
0x0D0	ROIC_ID	R	N	FPA ROIC identification number

Bits	Field	Description	Value	Unit
[15:0]	ROIC_ID	FPA ROIC identification number	Unsigned integer	

ROIC_ERROR

Address	Name	Acc.	Pro.	Description
0x0D4	ROIC_ERROR	R	N	FPA Serdat return error bits

Bits	Field	Description	Value	Unit
9	ROIC_ERROR_1	Rmin ≤ Rmax check status	0: OK 1: Error	
8	ROIC_ERROR_2	Rmax ≤ 512 check status	0: OK 1: Error	
7	ROIC_ERROR_3	1 ≤ Cmin check status	0: OK 1: Error	
6	ROIC_ERROR_4	Rmax – Rmin+1 ≥ 2 check status	0: OK 1: Error	
5	ROIC_ERROR_5	(Rmin mod 2 =1) AND (Rmax mod 2 = 0) check status	0: OK 1: Error	
4	ROIC_ERROR_6	Cmin ≤ Cmax check status	0: OK 1: Error	
3	ROIC_ERROR_7	Cmax ≤ 640 check status	0: OK 1: Error	

2	ROIC_ERROR_8	1 ≤ Cmin check status	0: OK 1: Error	
1	ROIC_ERROR_9	Cmax – Cmin +1 ≥ 160 check status	0: OK 1: Error	
0	ROIC_ERROR_10	(Cmin mod 4 =1) AND (Cmax mod 4=0) check status	0: OK 1: Error	

COOLDOWN_CNT

Address	Name	Acc.	Pro.	Description
0x100	COOLDOWN_CNT	RW	WP	Cooldown counter

Bits	Field	Description	Value	Unit
[23:0]	COOLDOWN_CNT	Cooldown counter. Number of FPA_TEMP_THRESHOLD crossing from high to low temperature	Unsigned integer	

COOLED_TIME

Address	Name	Acc.	Pro.	Description
0x104	COOLED_TIME	RW	WP	Cooled time counter

Bits	Field	Description	Value	Unit
[23:0]	COOLED_TIME	Accumulated time with FPA temperature under FPA_TEMP_THRESHOLD.	Unsigned integer	min

AMBIENT_TEMP

Address	Name	Acc.	Pro.	Description
0x110	AMBIENT_TEMP	R	N	Ambient temperature

Bits	Field	Description	Value	Unit
[7:0]	AMBIENT_TEMP	Ambient temperature	Signed integer	°C

AMBIENT_MIN/MAX

Address	Name	Acc.	Pro.	Description
0x114	AMBIENT_MIN	RW	WP	Minimal ambient temperature
0x118	AMBIENT_MAX	RW	WP	Maximal ambient temperature

Bits	Field	Description	Value	Unit
[7:0]	AMBIENT_MIN or AMBIENT_MAX	Minimal or maximal ambient temperature	Signed integer	°C

OPTIME_x

Address	Name	Acc.	Pro.	Description
0x120	OPTIME_M40_M30	RW	WP	Operating time between below -30°C
0x124	OPTIME_M30_M20	RW	WP	Operating time between -30 to -20°C
0x128	OPTIME_M20_M10	RW	WP	Operating time between -20 to -10°C
0x12C	OPTIME_M10_0	RW	WP	Operating time between -10 to 0°C
0x130	OPTIME_0_P10	RW	WP	Operating time between 0 to 10°C
0x134	OPTIME_P10_P20	RW	WP	Operating time between 10 to 20°C

0x138	OPTIME_P20_P30	RW	WP	Operating time between 20 to 30°C
0x13C	OPTIME_P30_P40	RW	WP	Operating time between 30 to 40°C
0x140	OPTIME_P40_P50	RW	WP	Operating time between 40 to 50°C
0x144	OPTIME_P50_P60	RW	WP	Operating time between 50 to 60°C
0x148	OPTIME_P60_P70	RW	WP	Operating time between 60 to 70°C
0x14C	OPTIME_P70_P80	RW	WP	Operating time between 70 to 80°C
0x150	OPTIME_P80_P90	RW	WP	Operating time between 80 to 90°C
0x154	OPTIME_P90_P100	RW	WP	Operating time between 90 to 100°C
0x158	OPTIME_P100_P110	RW	WP	Operating time between 100 to 110°C
0x15C	OPTIME_P110_P125	RW	WP	Operating time between above 110°C

Bits	Field	Description	Value	Unit
[16:0]	OPTIME_x	Total operating time in the ambient temperature range x	Unsigned integer	min

USER_DATA_x

Address	Name	Acc.	Pro.	Description
0x250	USER_DATA_1	RW	N	User data 1
0x254	USER_DATA_2	RW	N	User data 2
0x258	USER_DATA_3	RW	N	User data 3
0x25C	USER_DATA_4	RW	N	User data 4

Bits	Field	Description	Value	Unit
[31:0]	USER_DATA_x	Free space to allow user storing custom data	Unsigned integer	

CAL_GPOL

Address	Name	Acc.	Pro.	Description
0x330	CAL_GPOL	RW	WP	GPOL bias voltage (factory calibration)

Bits	Field	Description	Value	Unit
[15:0]	CAL_GPOL	FPA GPOL bias voltage (factory calibration)	Unsigned integer 1.5 ≤ value ≤ 3.6V	mV

COOLER_CTRL

Address	Name	Acc.	Pro.	Description
0x400	COOLER_CTRL	RW	N	Cooler general control

Bits	Field	Description	Value	Unit
4	COOLER_ON	Cooler enable	0: Disable 1: Enable	
[3:1]	Unused			
[0]	COOLER_UART_MODE	UART to cooler power mode	0: Auto power off 1: Always On	

COOLER_INT_STATUS

Address	Name	Acc.	Pro.	Description
0x450	COOLER_INT_STATUS	R	N	Cooler internal status

Bits	Field	Description	Value
[26:12]	Unused		
11	COOLER_STATUS_COOLDOWN	Cooldown indicator	0: In progress 1: Done
[10:9]	COOLER_STATUS_SETPOINT	Set point selected	00: Unused 01: Unused 10: Set point 2 11: Set point 1
8	COOLER_STATUS_COOLING	Cooling, cooler power supply status	0: Disable 1: Enable
[7:0]	Unused		

COOLER_SETPOINTx

Address	Name	Acc.	Pro.	Description
0x410	COOLER_SETPOINT_1	RW	N	FPA temperature set point 1
0x414	COOLER_SETPOINT_2	RW	N	FPA temperature set point 2

Bits	Field	Description	Value	Unit
[15:0]	COOLER_SETPOINT_x	FPA temperature set point x value	Unsigned integer	-

The following table gives an example of Register cooler_setpoint impact on TFPA. It is recommended to keep COOLER_SETPOINT between 900 & 940.

Approximated TFPA T° set (K)	Register COOLER_SETPOINT
145	940
150	930
155	920
160	911
165	902

COOLER_SNx

Address	Name	Acc.	Pro.	Description
0x4A8	COOLER_SN1	R	N	Cooler driver serial number 1
0x4AC	COOLER_SN2	R	N	Cooler driver serial number 2

Bits	Field	Description	Value	Unit
[31:0]	COOLER_SNx	Cooler driver serial number x	ASCII encoded string (little-endian byte order)	

- “12345678” is stored as
  - COOLER_SN1 = 0x34333231 (“1234”)
  - COOLER_SN2 = 0x38373635 (“5678”)

13.2. Lynred products compatibility

Product	LEO	DAPHNIS	GALATEA-HHTI	Plug Up Platform
Connector	Proxy : QSH Cooler :Depends on cooler	Proxy : QSH Cooler :Depends on cooler	Proxy : QSH Cooler : Depends on cooler	Proxy : QSH Cooler : No cooler connector
Power supply	Proxy : 5V Cooler :Depends on cooler	Proxy : 6V Cooler :Depends on cooler	Proxy : 5V Cooler : 12V	12V
communication protocol	CAMERA LINK® UART 8 bits	CAMERA LINK® UART with adjustable message size (specific)	CAMERA LINK® UART 8 bits & 32 bits	CAMERA LINK® UART 32 bits
CAMERA LINK® video protocol	Base mode			

End of document