



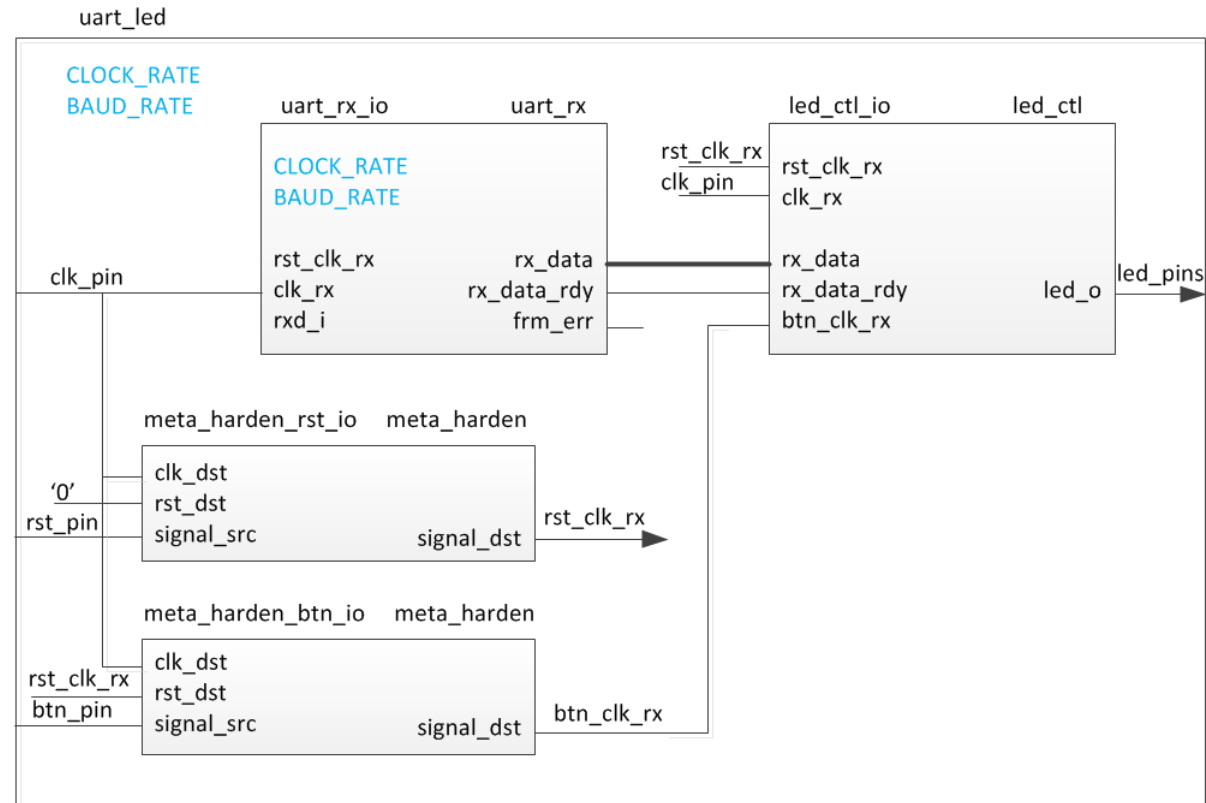
Lab2 Intro

Synthesizing a RTL Design

Introduction

- ▶ This lab uses a simple uart-led design. The design takes an input via a terminal operating at 115200 baud and displays the binary equivalent of the ASCII character the user has typed on the 8 LEDs. If the BTNU is pressed, then the upper and lower nibbles of the binary number gets swapped
- ▶ You will synthesize the design with the default settings as well as with some settings changed and observe the effect

The Design



Procedure

- ▶ Create a project using Vivado IDE using the provided HDL files and timing constraints
- ▶ Elaborate the design and view noise report and the schematic
- ▶ Synthesize the design with the default settings
- ▶ Open the synthesized design and view schematic
- ▶ View various reports including the timing summary, resource utilization, and power
- ▶ Write a checkpoint
- ▶ Synthesize the design with one of the settings changed
- ▶ Compare the generated schematic, timing summary, power and resource utilization
- ▶ Write another checkpoint
- ▶ Read previously written checkpoints and perform the same analysis

Summary

- ▶ In this lab you applied the timing constraints and synthesized the design. You viewed various post-synthesis reports. You wrote checkpoints and read it back to perform the analysis you were doing during the design flow. You saw the effect of changing synthesis settings.



Thank You

Disclaimer and Attribution

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale. GD-18

© Copyright 2022 Advanced Micro Devices, Inc. All rights reserved. Xilinx, the Xilinx logo, AMD, the AMD Arrow logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

