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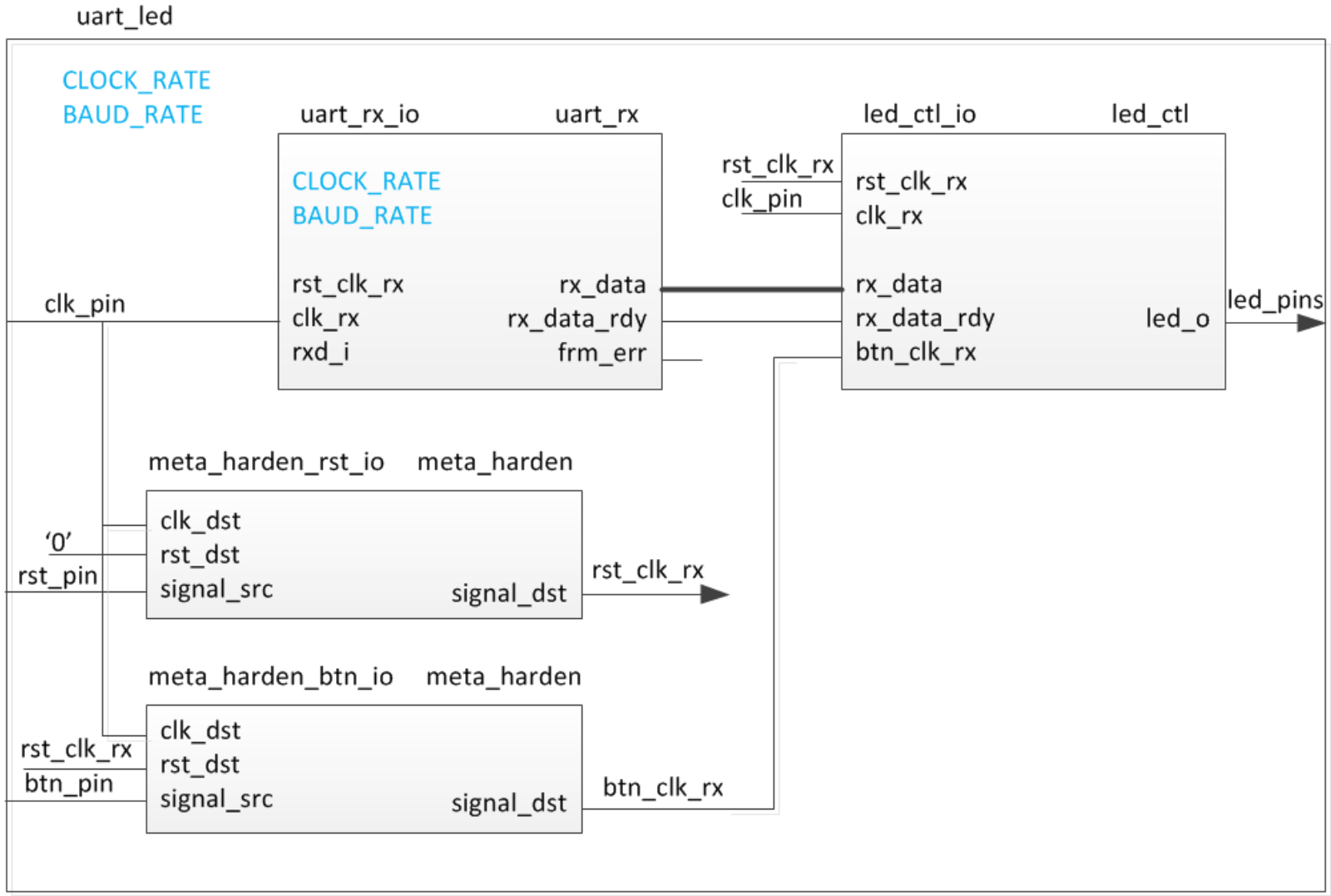
Lab5 Intro
Xilinx Design Constraints

Introduction

- In this lab you will use the uart_led design that was introduced in the previous labs. You will start the project with I/O Planning type, enter pin locations, and export it to the rtl. You will then create the timing constraints and perform the timing analysis

The Design



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Procedure

- Create a Vivado I/O Planning project
- Assign various pins and source files
- Synthesize and enter timing constraints
- Implement and perform timing analysis
- Generate the bitstream and verify (optional)

Summary

- In this lab, you learned how to create an I/O Planning project and assign the pins via the Device view, Package Pins tab, and the Tcl commands. You then exported to the rtl project where you added the provided source files. Next you created timing constraints and performed post-synthesis and post-implementation timing analysis.

Thank You

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