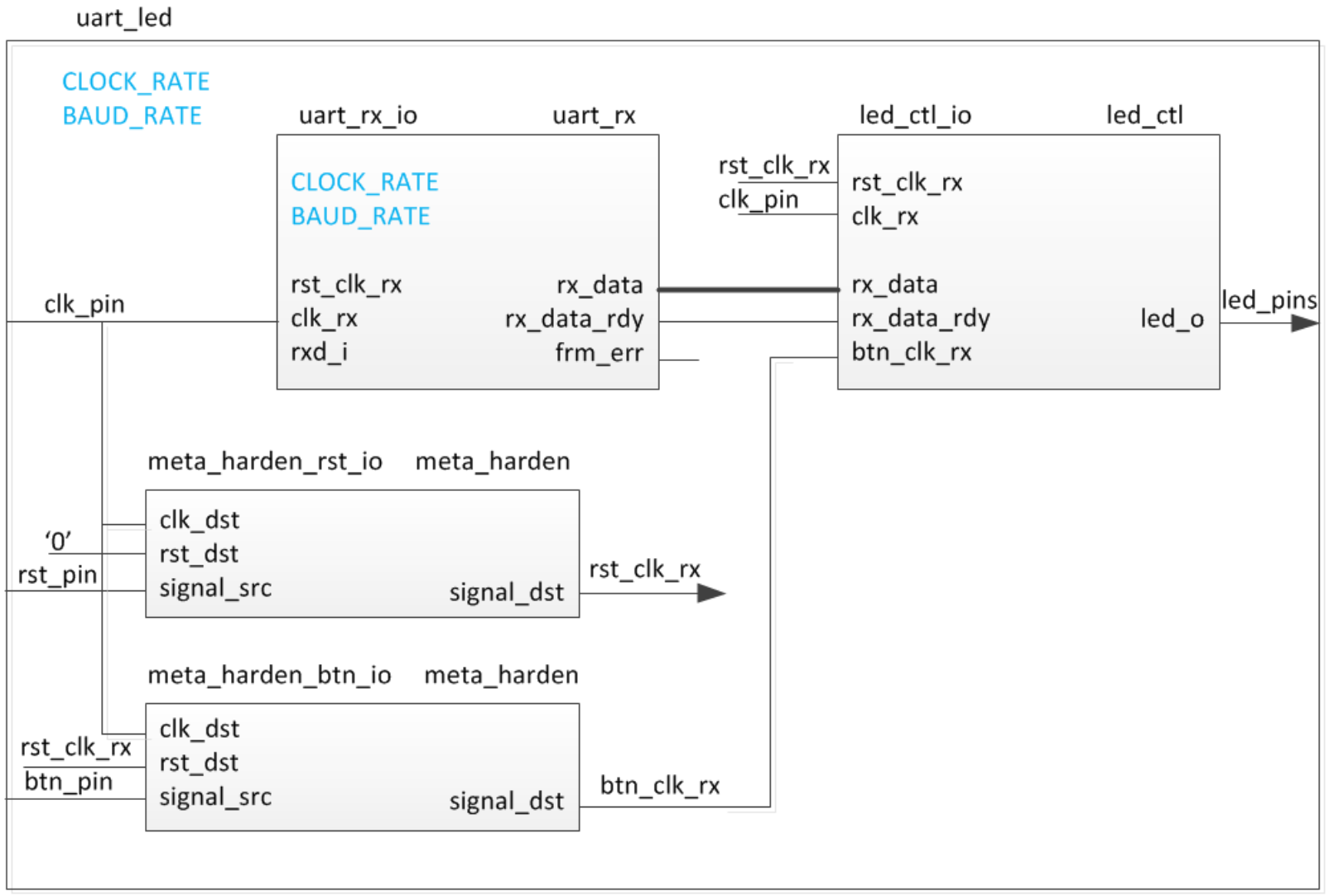
AMD
XILINX

Lab3 Intro
Implement and Verify the Design in Hardware

Introduction

- This lab continues with the previous lab. You will perform static timing analysis. Then you will open a hardware session and program the FPGA.

The Design



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Procedure

- Open the project you created in previous lab
- Set the synthesis to its default values
- Implement the design
- Perform the static timing analysis
- Generate the bitstream
- Configure the board and verify the functionality

Summary

- In this lab, you learned about many of the reports available to designers in the Vivado IDE. You also had the opportunity to learn basic design analysis using tools that are connected to the display of timing-critical paths, including the Schematic viewer, delay path properties and reports, Device view, and selecting primitive parents. You also learned about the basic timing report options that are at your disposal. You verified the functionality in hardware by typing characters on the host machine and seeing the LED pattern changes.

Thank You

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