University of Southern California
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EE 348L - Electronic Circuits
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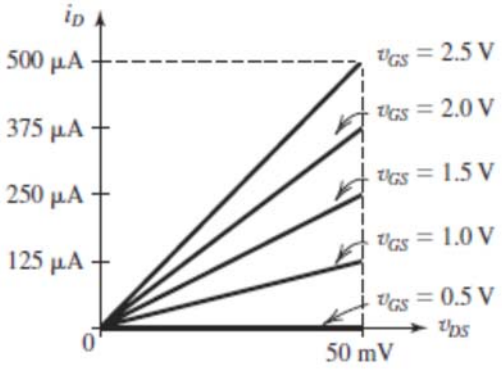
Homework 4 Solutions

5.6 $k_n = 5\ \text{mA/V}^2$, $V_{tn} = 0.5\ \text{V}$,

small v_{DS}

$$i_D = k_n(v_{GS} - V_t)v_{DS} = k_n v_{OV} v_{DS}$$

$$g_{DS} = \frac{1}{r_{DS}} = k_n v_{OV}$$



V_{GS} (V)	V_{OV} (V)	g_{DS} (mA/V)	r_{DS} (Ω)
0.5	0	0	∞
1.0	0.5	2.5	400
1.5	1.0	5.0	200
2.0	1.5	7.5	133
2.5	2.0	10	100

5.10 $L_{\min} = 0.25\ \mu\text{m}$

$t_{ox} = 6\ \text{nm}$

$$\mu_n = 460\ \frac{\text{cm}^2}{\text{V}\cdot\text{s}} = 460 \times 10^{-4}\ \frac{\text{m}^2}{\text{V}\cdot\text{s}}$$

(a) $$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{34.5\ \text{pF/m}}{6\ \text{nm}}$$

$$= 5.75 \times 10^{-3}\ \frac{\text{F}}{\text{m}^2}\left(\frac{\text{pF}}{\mu\text{m}^2}\right)$$

$$k_n' = \mu_n C_{ox} = 265\ \mu\text{A/V}^2$$

(b) For $\frac{W}{L} = \frac{20}{0.25}$, $k_n = 21.2\ \text{mA/V}^2$

$$\therefore 0.5\ \text{mA} = I_D = \frac{1}{2}\ k_n V_{OV}^2$$

$$V_{OV} = 0.22\ \text{V}$$

$$V_{GS} = 0.72\ \text{V}$$

$$V_{DS} \geq 0.22\ \text{V}$$

(c) $$g_{DS} = \frac{1}{100\ \Omega} = k_n V_{OV}$$

$$\therefore V_{OV} = 0.47\ \text{V}.$$

$$V_{GS} = 0.97\ \text{V}.$$

5.15

L (μm)	0.5	0.25	0.18	0.13
t_{ox} (nm)	10	5	3.6	2.6
$C_{ox}\left(\frac{\text{fF}}{\mu\text{m}^2}\right)$ $\epsilon_{ox} = 34.5$ pF/m	3.45	6.90	9.58	13.3
$k_n'\left(\frac{\mu\text{A}}{\text{V}^2}\right)$ ($\mu_n = 500\ \text{cm}^2/\text{V}\cdot\text{s}$)	173	345	479	665
$k_n\left(\frac{\text{mA}}{\text{V}^2}\right)$ for $\frac{W}{L} = 10$	1.73	3.45	4.79	6.65
$A(\mu\text{m}^2)$ for $\frac{W}{L} = 10$	2.50	0.625	0.324	0.169
V_{DD}(V)	5	2.5	1.8	1.3
V_t(V)	0.7	0.5	0.4	0.4
I_D(mA) for $V_{GS} = V_{DS} = V_{DD}$, $I_D = \frac{1}{2}k_n(V_{DD} - V_t)^2$	16	6.90	4.69	2.69
P(mW) $P = V_{DD}I_D$	80	17.3	8.44	3.50
$\frac{P}{A}\left(\frac{\text{mW}}{\mu\text{m}^2}\right)$	32	27.7	26.1	20.7
$\frac{\text{Devices}}{\text{Chip}}$	n	$4n$	$7.72n$	$14.8n$

5.17 For triode-region operation with v_{DS} small,

$$i_D \simeq k_n(v_{GS} - V_t)v_{DS}$$

Thus

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = \frac{1}{k_n(v_{GS} - V_t)}$$

$$1 = \frac{1}{k_n(1.2 - 0.8)} = \frac{1}{0.4\, k_n}$$

$$\Rightarrow k_n = 2.5 \text{ mA/V}$$

$$r_{DS} = \frac{1}{2.5(V_{GS} - 0.8)} \quad (\text{k}\Omega)$$

$$0.2 = \frac{1}{2.5(V_{GS} - 0.8)}$$

$$\Rightarrow V_{GS} = 2.8 \text{ V}$$

For a device with twice the value of W, k_n will be twice as large and the resistance values will be half as large: 500 Ω and 100 Ω, respectively.

5.19 For $V_{GS} = V_{DS} = 1$ V, the MOSFET is operating in saturation,

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2$$

$$0.4 = \frac{1}{2}k_n(1 - V_t)^2 \qquad (1)$$

$$0.1 = \frac{1}{2}k_n(0.8 - V_t)^2 \qquad (2)$$

Dividing Eq. (1) by Eq. (2) and taking square roots gives

$$2 = \frac{1 - V_t}{0.8 - V_t}$$

$$\Rightarrow V_t = 0.6 \text{ V}$$

Substituting in Eq. (1), we have

$$0.4 = \frac{1}{2}k_n \times 0.4^2$$

$$\Rightarrow k_n = 5 \text{ mA/V}^2$$

5.24 **(a)** Refer to Fig. P5.24. For saturation-mode operation of an NMOS transistor, $v_{DG} \geq -V_{tn}$; thus $v_{DG} = 0$ results in saturation-mode operation. Similarly, for a p-channel MOSFET, saturation-mode operation is obtained for $v_{GD} \geq -|V_{tp}|$, which includes $v_{GD} = 0$. Thus, the diode-connected MOSFETs of Fig. P5.24 have the i–v relationship

$$i = \frac{1}{2}k'\left(\frac{W}{L}\right)(v - |V_t|)^2 \qquad (1)$$

where k' represents k'_n in the NMOS case and k'_p in the PMOS case.

5.27 $V_{DS} = V_D - V_S \quad V_{GS} = V_G - V_S$

$V_{OV} = V_{GS} - V_t = V_{GS} - 1.0$

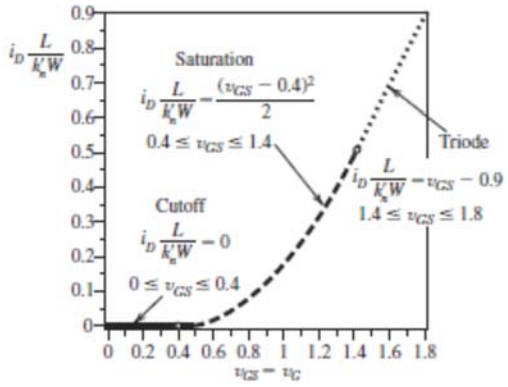
According to Table 5.1, three regions are possible.

Case	V_S	V_G	V_D	V_{GS}	V_{OV}	V_{DS}	Region of operation
a	+1.0	+1.0	+2.0	0	–1.0	+1.0	Cutoff
b	+1.0	+2.5	+2.0	+1.5	+0.5	+1.0	Sat.
c	+1.0	+2.5	+1.5	+1.5	+0.5	+0.5	Sat.
d	+1.0	+1.5	0	+0.5	–0.5	–1.0	Sat.*
e	0	+2.5	1.0	+2.5	+1.5	+1.0	Triode
f	+1.0	+1.0	+1.0	0	–1.0	0	Cutoff
g	–1.0	0	0	+1.0	0	+1.0	Sat.
h	–1.5	0	0	+1.5	+0.5	+1.5	Sat.
i	–1.0	0	+1.0	+1.0	0	+2.0	Sat.
j	+0.5	+2.0	+0.5	+1.5	+0.5	0	Triode

* With the source and drain interchanged.

5.28 The cutoff–saturation boundary is determined by $v_{GS} = V_t$, thus $v_{GS} = 0.4$ V at the boundary.

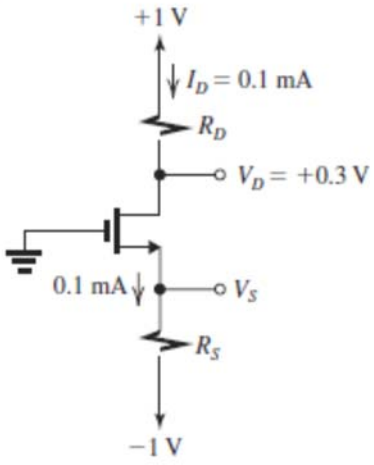
The saturation–triode boundary is determined by $v_{GD} = V_t$, and $v_{DS} = V_{DD} = 1$ V, and since $v_{GS} = v_{GD} + v_{DS}$, one has $v_{GS} = 0.4 + 1.0 = 1.4$ V at the boundary.



5.40 PMOS with $V_{tp} = -1$ V

Case	V_S	V_G	V_D	V_{SG}	$\lvert V_{OV} \rvert$	V_{SD}	Region of operation
a	+2	+2	0	0	0	2	Cutoff
b	+2	+1	0	+1	0	2	Cutoff–Sat.
c	+2	0	0	+2	1	2	Sat.
d	+2	0	+1	+2	1	1	Sat–Triode
e	+2	0	+1.5	+2	1	0.5	Triode
f	+2	0	+2	+2	1	0	Triode

5.44



Since $V_{DG} > 0$, the MOSFET is in saturation.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$0.1 = \frac{1}{2} \times 0.4 \times \frac{5}{0.4} \times V_{OV}^2$$

$$\Rightarrow V_{OV} = 0.2 \text{ V}$$

$$V_{GS} = V_t + V_{OV} = 0.5 + 0.2 = 0.7$$

$$V_S = 0 - V_{GS} = -0.7 \text{ V}$$

$$R_S = \frac{V_S - (-1)}{I_D} = \frac{-0.7 + 1}{0.1} = 3 \text{ k}\Omega$$

$$R_D = \frac{1 - V_D}{I_D} = \frac{1 - 0.3}{0.1} = \frac{0.7}{0.1} = 7 \text{ k}\Omega$$

5.55 (a) Refer to Fig. P5.55(a): Assuming saturation-mode operation, we have

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

$$2 = \frac{1}{2} \times 4 \, V_{OV}^2$$

$$\Rightarrow V_{OV} = 1 \text{ V}$$

$$V_{GS} = |V_t| + V_{OV} = 1 + 1 = 2 \text{ V}$$

$$V_1 = 0 - V_{GS} = -2 \text{ V}$$

$$V_2 = 5 - 2 \times 2 = +1 \text{ V}$$

Since $V_{DG} = +1$ V, the MOSFET is indeed in saturation.

Refer to Fig. P5.55(b): The transistor is operating in saturation, thus

$$I_D = \frac{1}{2} k_n V_{OV}^2$$

$$2 = \frac{1}{2} \times 4 \times V_{OV}^2 \Rightarrow V_{OV} = 1 \text{ V}$$

$$V_{GS} = 2 \text{ V}$$

$$\Rightarrow V_3 = 2 \text{ V}$$

Refer to Fig. P5.55(c): Assuming saturation-mode operation, we have

$$I_D = \frac{1}{2} k_p |V_{OV}|^2$$

$$2 = \frac{1}{2} \times 4 \times |V_{OV}|^2$$

$$\Rightarrow |V_{OV}| = 1 \text{ V}$$

$$V_{SG} = |V_t| + |V_{OV}| = 1 + 1 = 2 \text{ V}$$

$$V_4 = V_{SG} = 2 \text{ V}$$

$$V_5 = -5 + I_D \times 1.5$$

$$= -5 + 2 \times 1.5 = -2 \text{ V}$$

Since $V_{DG} < 0$, the MOSFET is indeed in saturation.

Refer to Fig. P5.55(d): Both transistors are operating in saturation at equal $|V_{OV}|$. Thus

$$2 = \frac{1}{2} \times 4 \times |V_{OV}|^2 \Rightarrow |V_{OV}| = 1 \text{ V}$$

$$V_{SG} = |V_t| + |V_{OV}| = 2 \text{ V}$$

$$V_6 = 5 - V_{SG} = 5 - 2 = 3 \text{ V}$$

$$V_7 = +5 - 2 \, V_{SG} = 5 - 2 \times 2 = 1 \text{ V}$$

(b) Circuit (a): The 2-mA current source can be replaced with a resistance R connected between the MOSFET source and the -5-V supply with

$$R = \frac{V_1 - (-5)}{2\text{ mA}} = \frac{-2+5}{2} = 1.5\text{ k}\Omega$$

Circuit (b): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{5 - V_3}{2\text{ mA}} = \frac{5-2}{2} = 1.5\text{ k}\Omega$$

Circuit (c): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{5 - V_4}{2\text{ mA}} = \frac{5-2}{2} = 1.5\text{ k}\Omega$$

Circuit (d): The 2-mA current source can be replaced with a resistance R,

$$R = \frac{V_7}{2\text{ mA}} = \frac{1}{2} = 0.5\text{ k}\Omega$$

We use the nearest 1% resistor, which is 499 Ω.

5.59 (a) Refer to the circuit in Fig. P5.59(a). Since the two NMOS transistors are identical and have the same I_D, their V_{GS} values will be equal. Thus

$$V_{GS} = \frac{3}{2} = 1.5 \text{ V}$$

$$V_2 = 1.5 \text{ V}$$

$$V_{OV} = V_{GS} - V_t = 1.0 \text{ V}$$

$$I_1 = I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2$$

$$= \frac{1}{2} \times 270 \times \frac{3}{1} \times 1$$

$$= 405 \text{ μA}$$

(b) Refer to the circuit in Fig. P5.59(b). Here Q_N and Q_P have the same $I_D = I_3$. Thus

$$I_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OVN}^2 \quad (1)$$

$$I_3 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)V_{OVP}^2 \quad (2)$$

Equating Eqs. (1) and (2) and using $\mu_n C_{ox} = 3\mu_p C_{ox}$ gives $3V_{OVN}^2 = V_{OVP}^2$:

$$|V_{OVP}| = \sqrt{3}\, V_{OVN}$$

Now,

$$V_{GSN} = V_{OVN} + V_t = V_{OVN} + 0.5$$

$$V_{SGP} = |V_{OVP}| + |V_t| = \sqrt{3}\, V_{OVN} + 0.5$$

But

$$V_{SGP} + V_{GSN} = 3$$

$$(\sqrt{3} + 1)V_{OVN} + 1 = 3$$

$$\Rightarrow V_{OVN} = 0.732 \text{ V}$$

$$V_{OVP} = 1.268 \text{ V}$$

$$V_{GSN} = 1.232 \text{ V}$$

$$V_{SGP} = 1.768 \text{ V}$$

$$V_4 = V_{GSN} = 1.232 \text{ V}$$

$$I_3 = \frac{1}{2} \times 270 \times \frac{3}{1} \times 0.732^2 = 217 \text{ μA}$$

(c) Refer to Fig. P5.59(c). Here the width of the PMOS transistor is made 3 times larger than that

of the NMOS transistor. This compensates for the factor 3 in the process transconductance parameter, resulting in $k_p = k_n$, and the two transistors are matched. The solution will be identical to that for (a) above with

$$V_5 = \frac{3}{2} = 1.5 \text{ V}$$

$$I_6 = 405 \ \mu\text{A}$$