NXP DEVKIT-ZVL128

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Revisions			
Rev	Description	Designer	Date
X1	Initial Draft A070 Release	Alejandro Cervantes	07/07/15
A	Prototype release	Alejandro Cervantes	07/29/15

C A U T I O N :

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User notes are given throughout the schematics.

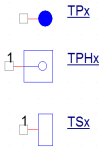
Specific PCB LAYOUT notes are detailed in ITALICS

3 Different test points used in design:

TPx - Test point pad

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TSx - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx.
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always position 1-2.
  2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

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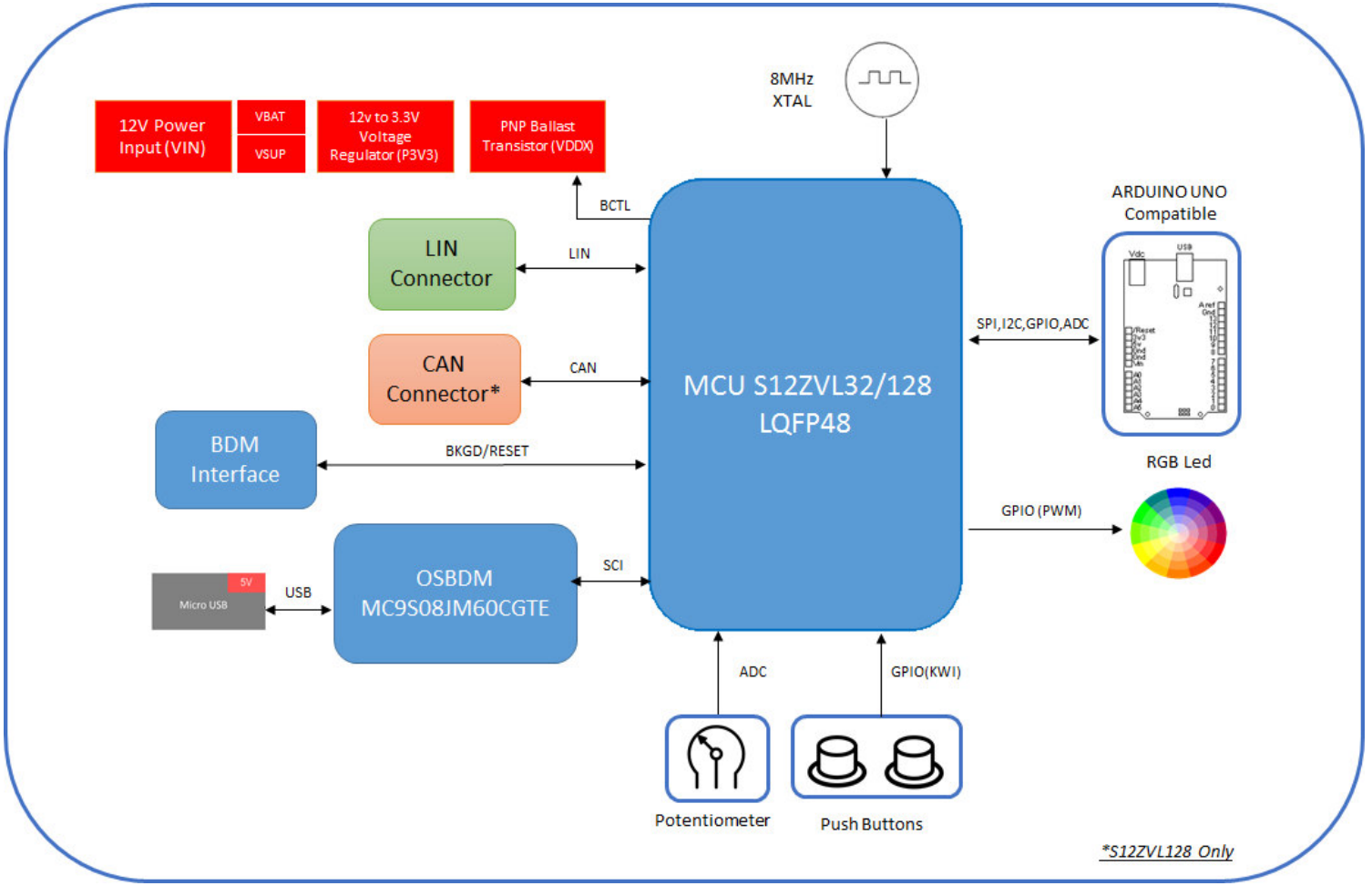
Approved: Jesus Sanchez	Size B	Document Number SCH-29227 PDF: SPF-29227	Rev A
	Date: Monday, March 07, 2016	Sheet 1 of 6	



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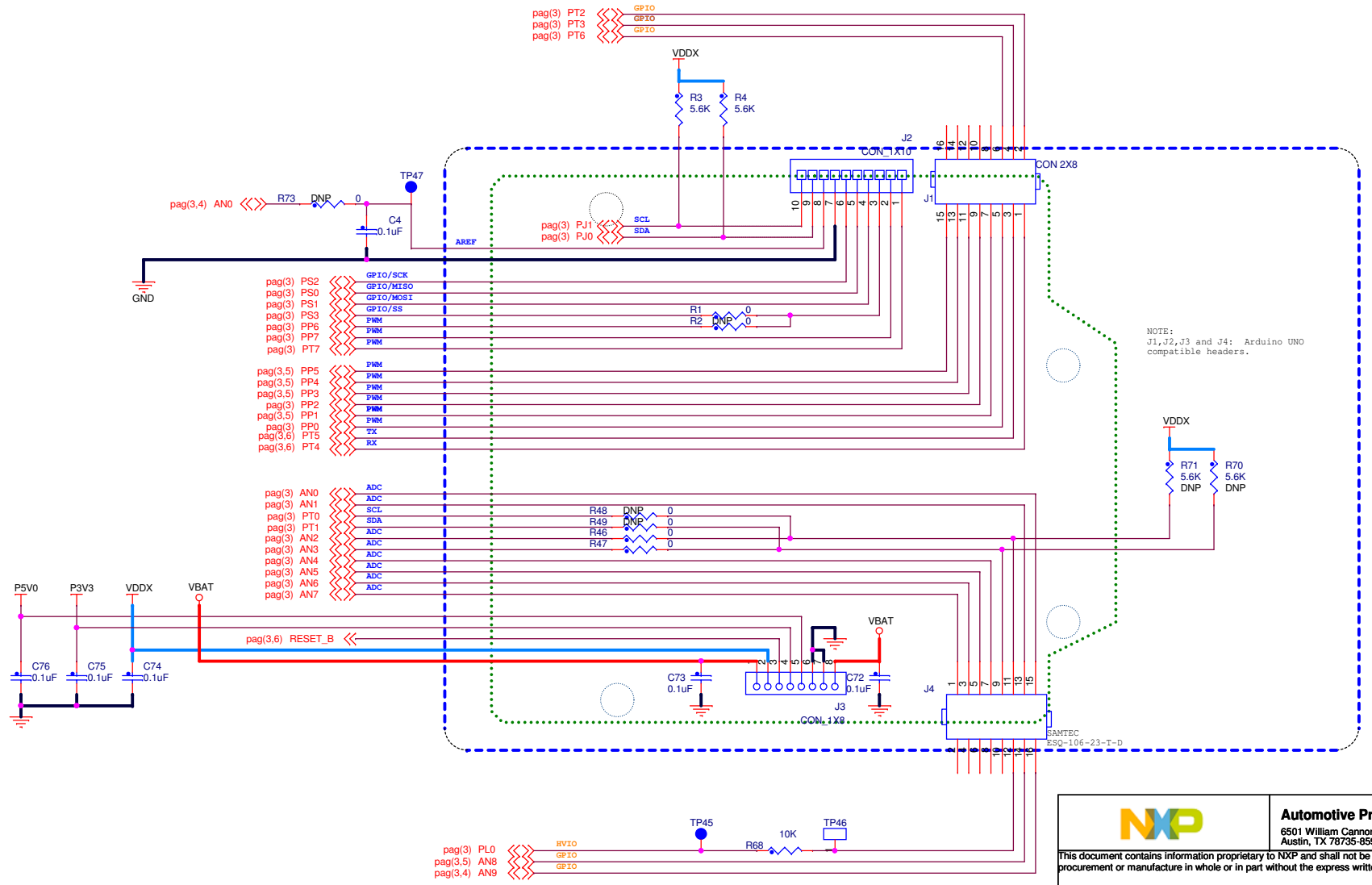

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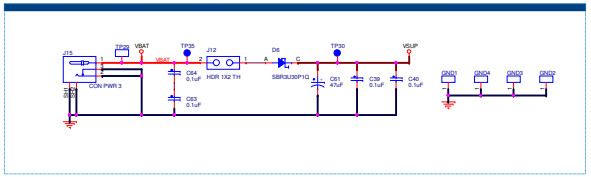

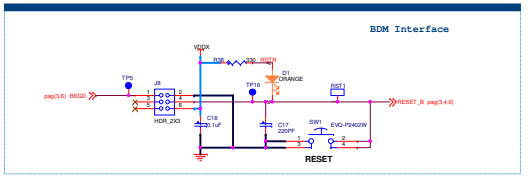

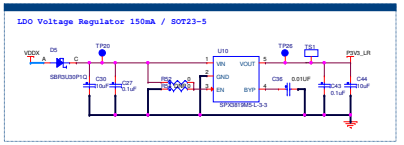

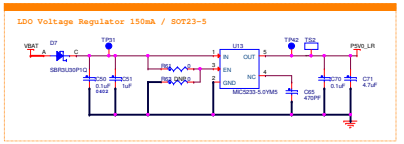

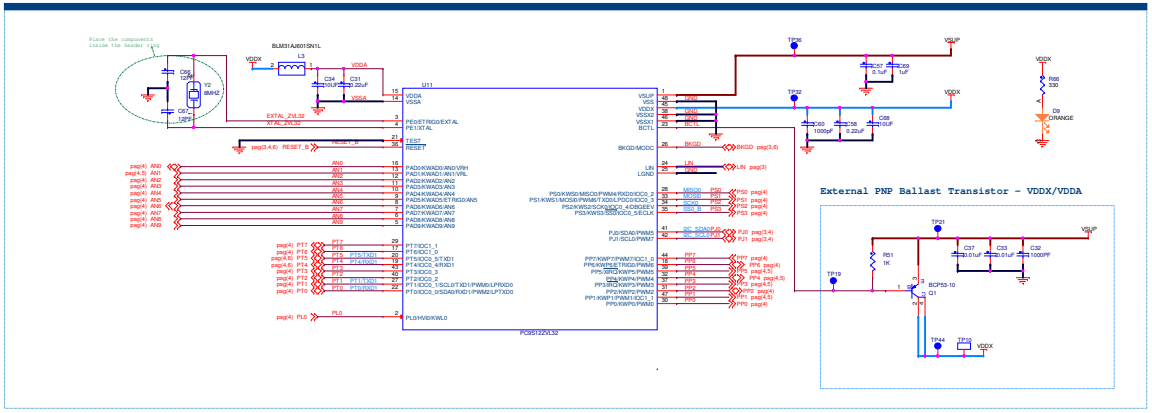

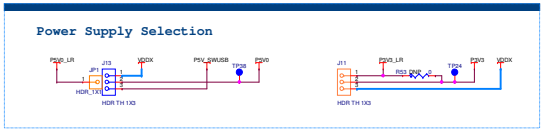

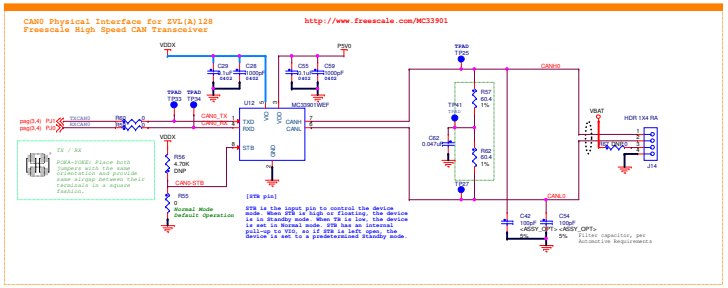

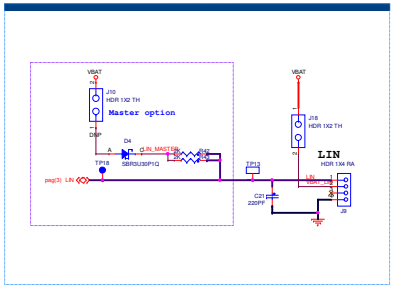

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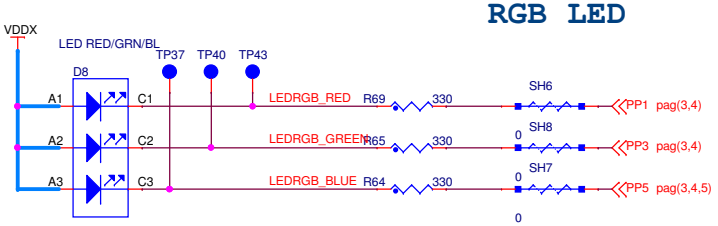
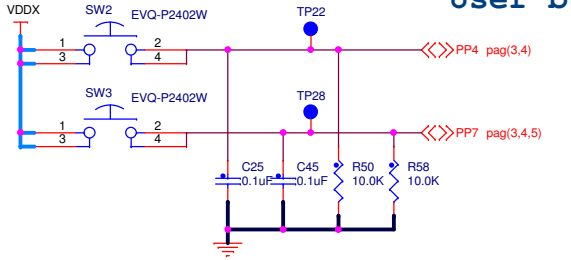
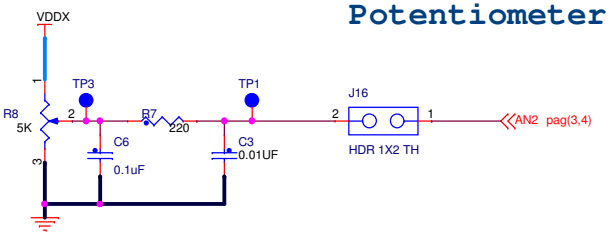
RGB LED



User buttons



Potentiometer



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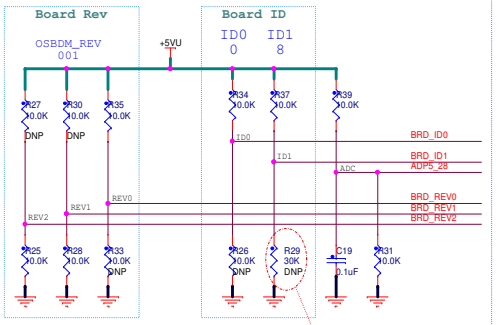
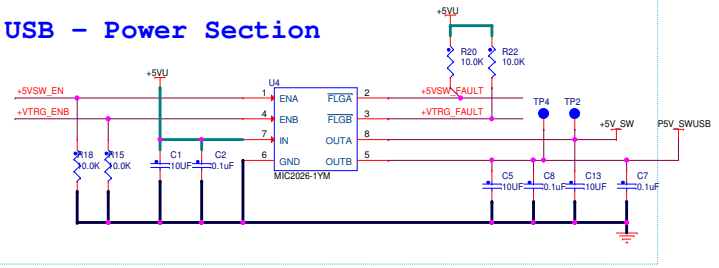
OSBDM Interface

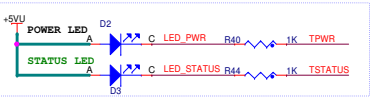
BOARD ID RESISTANCE SELECTION TABLE

#	Pull-Up	Pull-Down
0	10K	0
1	10K	1.3K
2	10K	3.3K
3	10K	5.6K
4	10K	10K
5	10K	18K
6	10K	30K
7	10K	62K
8	**10K**	**(NC)**



USB - Power Section

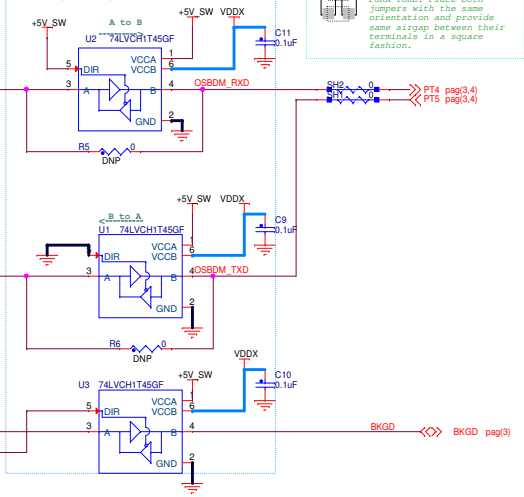


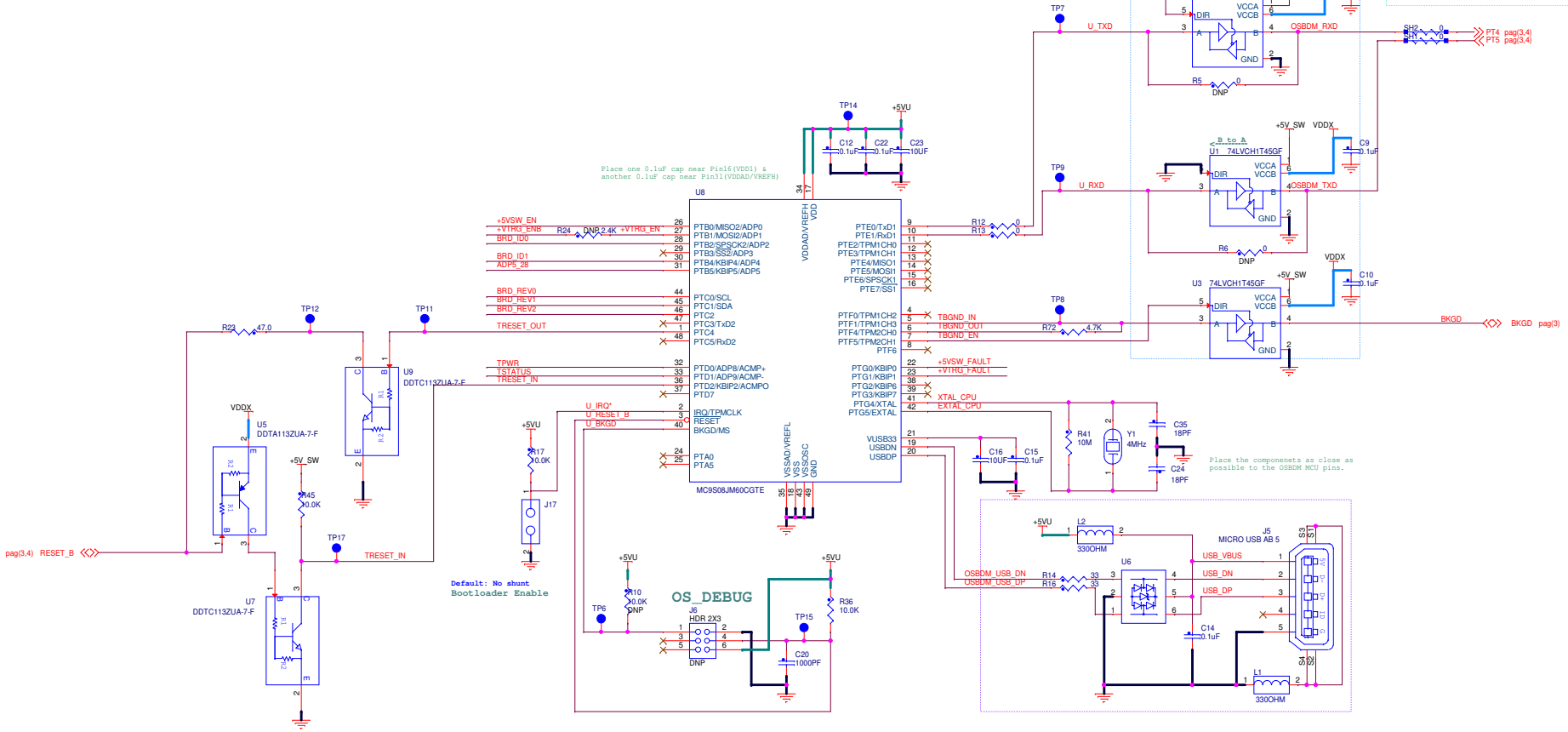


MCU-OSBDM VOLTAGE TRANSLATORS

TX / RX [R456 and R457]

POKA-YOKE: Place both jumpers with the same orientation and provide same airgap between their terminals in a square fashion.





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