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Application Note

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Hardware Design Guidelines for the S12ZVL Microcontrollers

MagniV mixed-signal MCUs for LIN applications

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Contents

1 Introduction

1.1 Purpose and scope

This document contains hardware guidelines for designing with the S12ZVL family of S12 MagniV Mixed-Signal MCU for LIN applications from NXP Semiconductors.

The purpose of this application note is to describe possible hardware considerations for developing hardware design solutions. It covers topics such as clock generation, decoupling, and voltage regulator and power considerations. Detailed reference design schematics and descriptions of the main components are also contained within this document.

NOTE

Electrical parameters mentioned in this application note are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.

2 S12ZVL device family overview

The MC9S12ZVL-Family is an automotive 16-bit microcontroller family using the 180nm NVM + UHV technology that offers the capability to integrate 40 V analog components. This family reuses many features from the existing S12 portfolio. The particular differentiating features of this family are the enhanced S12Z core and the integration of “high-voltage” analog modules, including the voltage regulator (VREG) and a Local Interconnect Network (LIN) physical layer.

The MC9S12ZVL-Family includes error correction code (ECC) on RAM, FLASH and EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12ZVL-Family delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12ZVL-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12 families. The MC9S12ZVL-Family is available in 48-pin, 32-pin LQFP and 32-pin QFN-EP. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12ZVL-Family is a general-purpose family of devices suitable for a wide range of applications. The MC9S12ZVL-Family is targeted at generic automotive applications requiring LIN connectivity. Typical examples of these applications include switch panels and body endpoints for sensors.

2.1 MC9S12ZVL-family block diagram

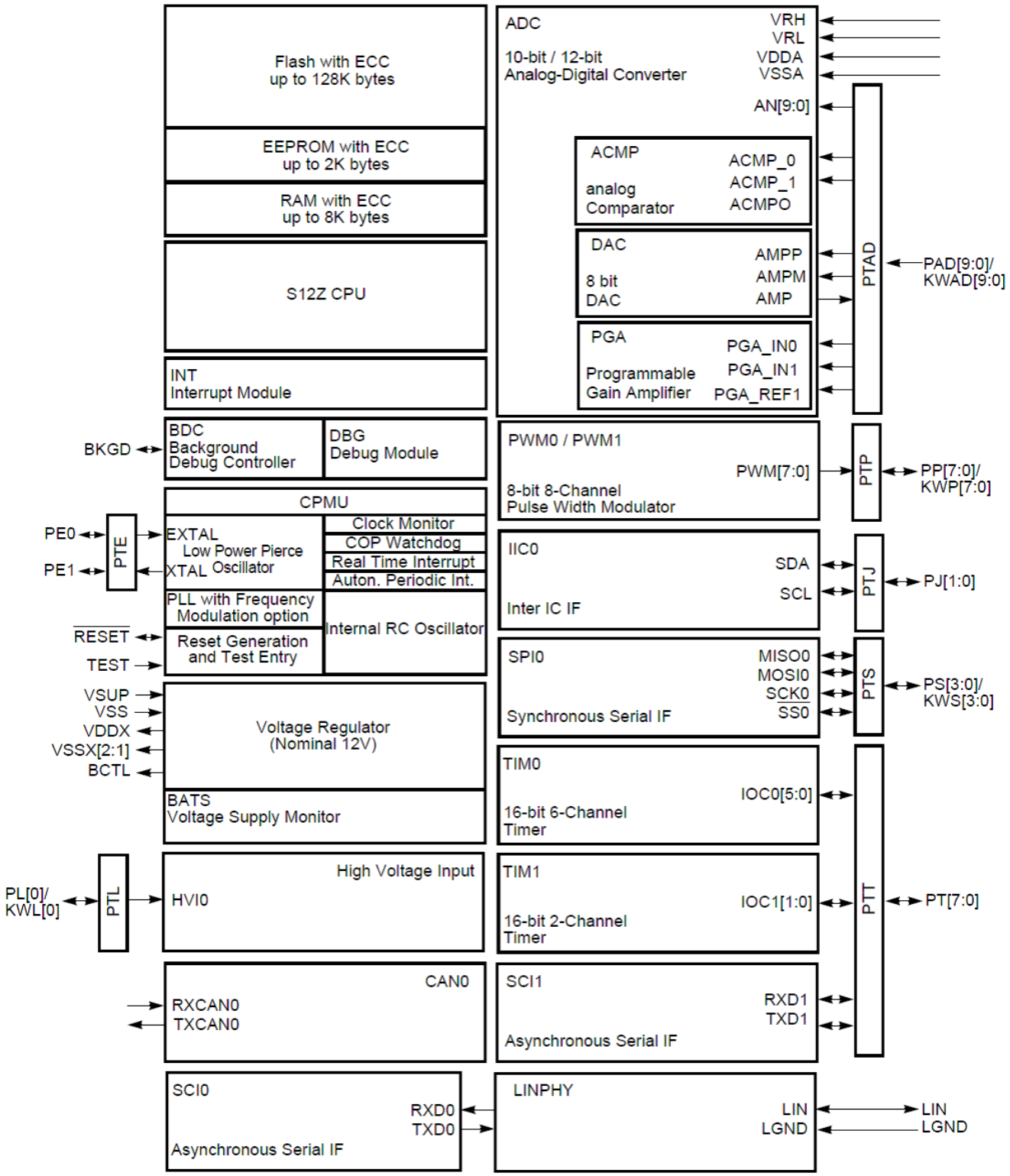


Figure 1. Block diagram of the MC9S12ZVL(A)128/96/64-Family

2.2 MC9S12ZVL-family comparison

Table 1. MC9S12ZVL-Family Comparison

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
Flash memory (ECC) [KB]	128	96	64	32	16	8	32	16
EEPROM (ECC) [Byte]	2048		1024	128				
RAM (ECC) [Byte]	8192		4096	1024	1024	512	1024	
max bus clock	32 MHz			32 MHz			32 MHz	
HVI	1			1			1	
LIN physical layer	1			1			1	
Vreg current capability[1] - 70 mA (VDDX) - 170 mA ballast option (BCTL) - tolerance - 3.3 V VDDX support	 yes yes 3% / 2%[2] yes			 yes yes 3% no			 yes yes 3% no	
ASIL SEooC target	A			A				
Package	48-pin / 32-pin LQFP / 32-pin QFN-EP[2]			48-pin / 32-pin LQFP			32-pin QFN-EP	
ADC channels - 10-bit - 12-bit	 10[3] / 6 10[2, 3] / 6[, 2]			 10[3] / 6 -			 6 -	
PWM	8 16 bit channels			8 channels (up to 4 16 bit)			8 channels (up to 4 16 bit)	
DAC	1[42]			-			-	
PGA[5]	1[2]			-			-	
ACMP	1[2]			-			-	
Timer	6 + 2 channel			6 + 2 channel			6 + 2 channel	
SCI[6]	2			2			2	
SPI	1			1			1	
IIC	1			1			1	
MSCAN	1			-			-	
max SRAM_ECC access width	4 Byte			2 Byte			2 Byte	
Supported ADC option bits	yes			no			no	
General purpose I/O	34[3] / 19			34[3] / 19			18	

Table continues on the next page...

Table 1. MC9S12ZVL-Family Comparison (continued)

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
- pin to support 25 mA driver strength to VSSX - pin to support 20 mA driver strength from VDDX (EVDD)	3[3] / 1 1			3[3] / 1 1			3 1	
Interrupt capable pins[7] 5V / 12V	22[3] / 16 / 1			22[3] / 16 / 1			14 / 1	

1. Total current capability for MCU and MCU - external loads (on same PCB - board)
2. MC9S12ZVLA device only
3. Available in 48-pin packages only
4. To internally feed the ACMP or bonded out in 48-LQFP
5. only 5V operation mode supported
6. one SCI routed to the LINPHY
7. $\overline{IRQ}$ / $\overline{XIRQ}$ and KWx pins

3 Power management

The power and ground pins are described in subsequent sections. Use bypass capacitors with low inductance characteristics and place them as close to the MCU as possible to account for fast signal transitions, which place high but short-duration current demands on the power supply.

3.1 VSUP – Main power supply pin

VSUP is the 12 V/18 V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection, as shown in Figure 2.

The designer could choose to add Bulk/Bypass capacitor as a charge tank to provide power when losing battery. The value of this capacitor depends on the current consumption and the amount of time the MCU needs to perform house-keeping activities before shutting down.

3.2 Digital I/O and analog supplies pins

3.2.1 VDDX, VSSX — Pad supply pins

VDDX is the supply domain for the digital Pads. An off-chip stability and decoupling capacitor between VDDX and VSSX are required. This supply domain is monitored by the Low Voltage Reset circuit. VDDX has to be connected externally to VDDA.

3.2.2 VDDA, VSSA — Regulator reference supply pins

VDDA and VSSA pins are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. An off-chip decoupling capacitor between VDDA and VSSA is required and can improve the quality of this supply.

NOTE

All VDDX and VDDA pins of the microcontroller (VDDX1 and VDDX2 and VDDA) must be connected together.

3.2.3 BCTL — Base control pin for external PNP

The device supports the use of an external PNP to supplement the VDDX supply, for reducing on chip power dissipation. In this configuration, most of the current flowing from VBAT to VDDX, through the external PNP. The BCTL pin is the ballast connection for the on chip voltage regulator for the VDDX/VDDA power domains. It provides the base current of an external PNP Ballast transistor. An additional resistor between emitter and base of the BJT is required.

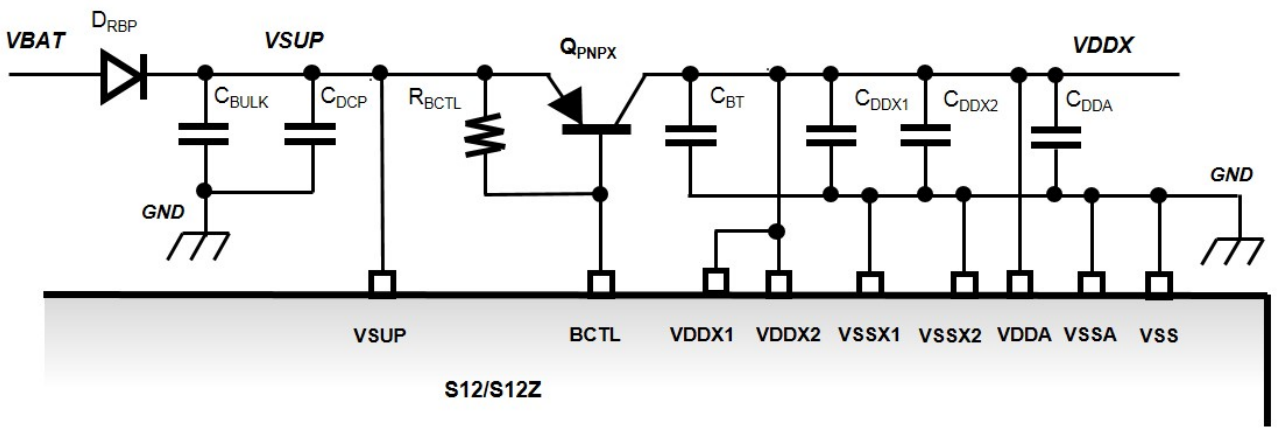


Figure 2. VDDX/VDDA Supply pins

NOTE

All GROUND pins of the microcontroller (VSSX1, VSSX2, VSSA, and VSS) must be connected together.

Table 2. VDDX/VDDA - Component description and recommended values

Symbol	Characteristic	Value
D_{RBP}	Reverse Current/Battery diode Protection	
C_{BULK}	Bulk/Bypass capacitor	
C_{DCP}	Decoupling Capacitor.	
Q_{PNPX}	PNP Ballast transistor	
R_{BCTL}	Metal Film resistor	1 kΩ
C_{BT}	Stability Capacitor. X7R Ceramic or Tantalum	4.7 uF – 10 uF
C_{DDX1}, C_{DDX2}	Decoupling Capacitor for VDDX. X7R Ceramic	100 nF - 220 nF
C_{DDA}	Decoupling Capacitor for VDDA. X7R Ceramic	100 nF - 220 nF

3.3 Selecting the PNP external ballast transistor.

The maximum VREG current capability [$IVREG_{MAX}$] using a PNP External Ballast transistor [QPNP], must be determined by the allowed maximum power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- package type
- dissipation mounting pad area on the PCB
- ambient temperature

Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn't be exceeded. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified to +25°C; and above this temperature, the power derates to the maximum Junction Temperature (+150°C). The Rth_{JA} depends considerably of the package transistor and the mounting pad area. The final product thermal limits should be tested and quantified in order to ensure acceptable performance and reliability.

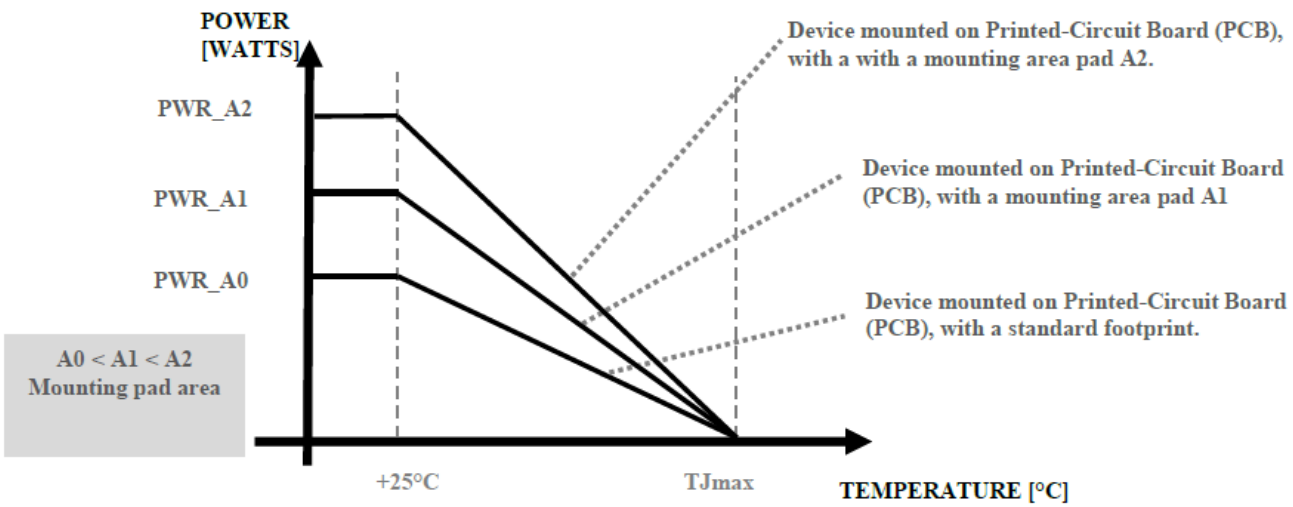


Figure 3. Maximum power dissipation versus temperature

The maximum power dissipation PWR_{MAX} by the device is given by:

$$PWR_{MAX} = \frac{TJ_{MAX} - T_{AMB}}{Rth_{JA}}$$

Equation 1

where T_{AMB} is ambient temperature, TJ_{MAX} is maximum junction temperature and Rth_{JA} is the Junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

3.3.1 Static thermal analysis

It is extremely important to consider the derating of the power device above of +25°C (typical value for transistors). This guarantees that the junction temperature will be lower than the maximum operating junction temperature specification. The following static thermal analysis using PSPICE Simulator demonstrates how the maximum power dissipation and the maximum supply current can be estimated for different voltage levels of VDDX.

NOTE

The data used in the next examples are fictional and should not be taken as specifications for particular systems. For specific calculations, please refer to the device datasheet.

1. Example (a)

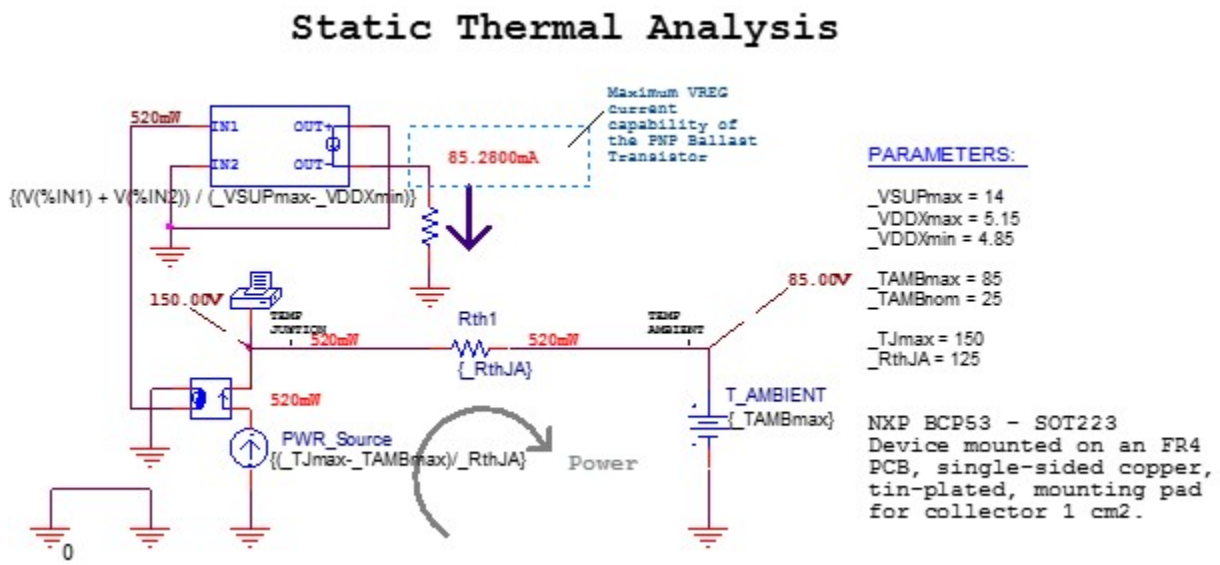


Figure 4. Static thermal analysis with PSPICE for $VDDX_{NOM}$=5V

2. Example (b)

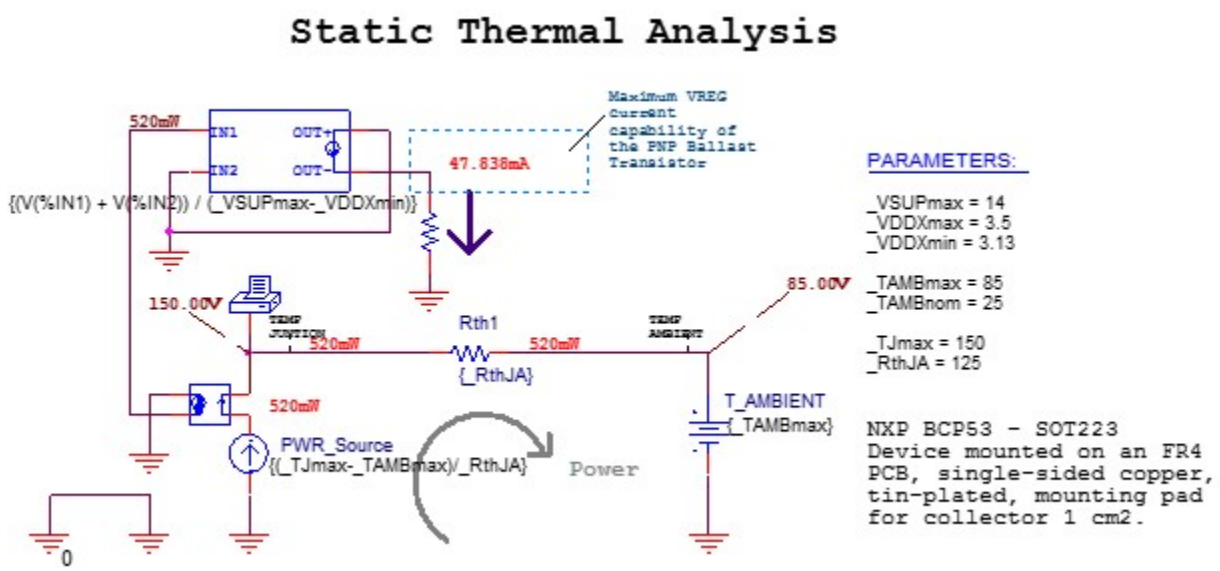


Figure 5. Static thermal analysis with PSPICE for $VDDX_{NOM}$=3.3V

Based on these examples, the maximum power dissipation of the ballast transistor is 520 mW, and the maximum storage temperature of the device is +150 °C, therefore the device can provide 85.28 mA for $VDDX_{MIN}$= 4.85 V, and 47.838 mA for $VDDX_{MIN}$=3.13 V, as the maximum IDDX current capability.

3.3.2 Recommended ballast transistor

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C). The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

Table 3. Recommended ballast transistor

Part Number	Package type	Manufaturer
BCP53	SOT-223	**NXP**
PBSS5360PAS	DFN2020D-3 [SOT1061D]	**NXP**

The designer must follow and verify all layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

Make sure that the traces for decoupling capacitors are as short as possible. Shortening the capacitor traces to/from the ground/power plane is the most important concern for making a low inductance connection. In order to implement an appropriate decoupling for applications with LIN, CAN, SPI and IIC interfaces, consider the pairing of the power and ground planes close to each other (less than 10 mils). This creates an effect interplane capacitance, greatly reduces noise and increases power supply stability at the pins because of the extremely low inductance of this kind of capacitance in the layers.

The number of discrete capacitance can be reduced because the effective capacitors are greatly increased and the impedance of the power distribution network is reduced across a very broad frequency range.

4 Programmming interface

The BDM connector requires connection to the RESET pin, voltage (VDDX) and ground. It is recommended to add a ceramic capacitor to VDDX near the connector to reduce noise that could be injected by the programming circuitry to the power supply, a decoupling capacitor is recommended.

4.1 BKGD

The background debug controller (BDC) is a single-wire, background debug system implemented in on chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC. The S12ZVL maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface. The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

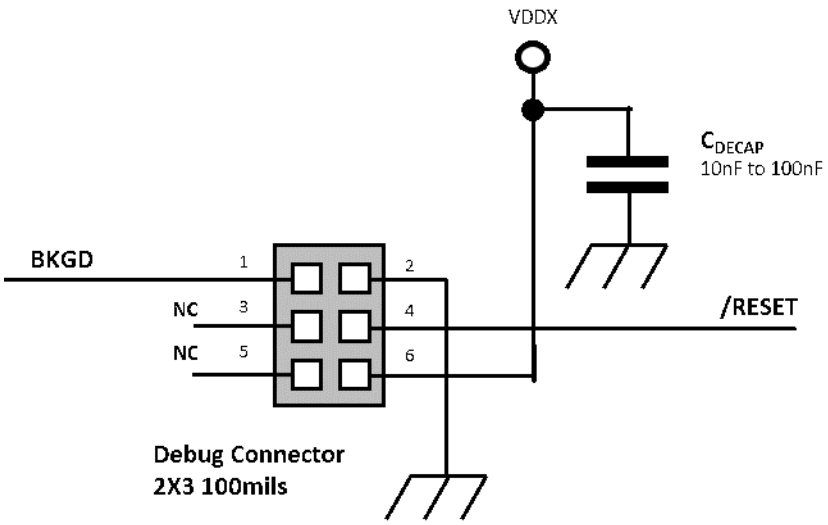


Figure 6. Debug connector configuration

4.2 Reset

The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The RESET pin has an internal pull-up device.

Upon detection of any reset source, an internal circuit drives the RESET pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the RESET pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

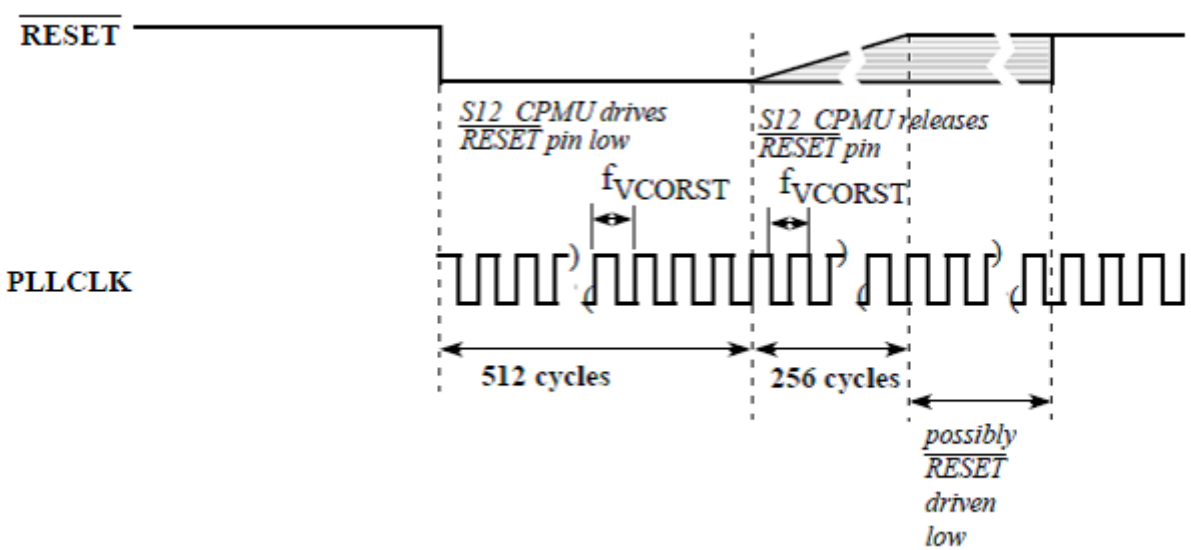


Figure 7. Reset timing

4.3 TEST pin

This pin should always be grounded in all applications.

5 External and internal RC oscillator

The S12ZVL devices have an internal 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range. There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies. The S12ZVL includes an oscillator control module capable of supporting either Loop Controlled Pierce (LCP) or Full Swing Pierce (FSP) oscillator configurations. The oscillation mode is selectable by software.

5.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

The Pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S12ZVL supports crystals or resonators from 4MHz to 20MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

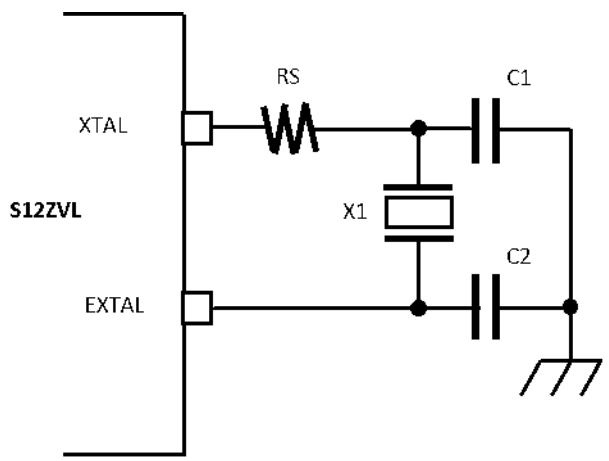


Figure 8. Reference oscillator circuit

Table 4. Components of the oscillator circuit

Symbol	Description
RS	Bias Resistor
X1	Quartz crystal/ Ceramic oscillator
C1	Stablizing Capacitor
C2	Stablizing Capacitor

The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

5.2 Suggestions for the PCB layout of oscillator circuit.

The crystal oscillator is an analog circuit and must be designed carefully and according to analog-board layout rules:

- External feedback resistor [Rf] is not needed because it's already integrated.
- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding CXTAL and CEXTAL capacitors. The data sheet includes recommendations for the tank capacitors CXTAL and CEXTAL. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the S12ZVL pins, the crystal and, the external capacitors must be as short as possible, without using any via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS of the S12ZVL with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to CEXTAL to CXTAL to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitors' ground connections should always be as close together as possible.
- With 2-layer boards, do not route any digital-signal lines on the opposite side of the PCB under the crystal area. In any case, it is good design practice to fill the opposite side of the PCB with clean ground and also connect this ground to VSS of the S12ZVL.

The following figure shows the recommended placement and routing for the oscillator layout.

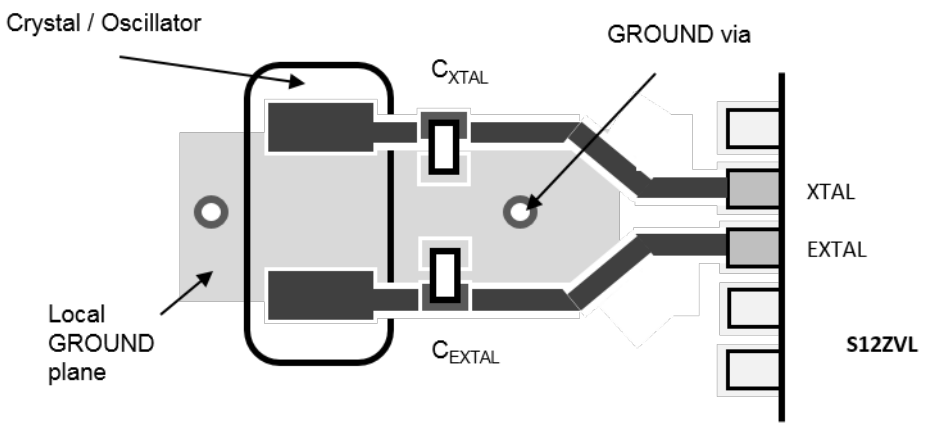


Figure 9. Suggested crystal oscillator layout

6 High voltage inputs (HVI)

The high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to VHVI
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wake-up from stop (pin interrupts in run mode not available). Open input detection.

6.1 Open input detection on HVI

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type, an external pull down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

An external resistor REXT_HVI must be always connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

6.2 External pulldown device

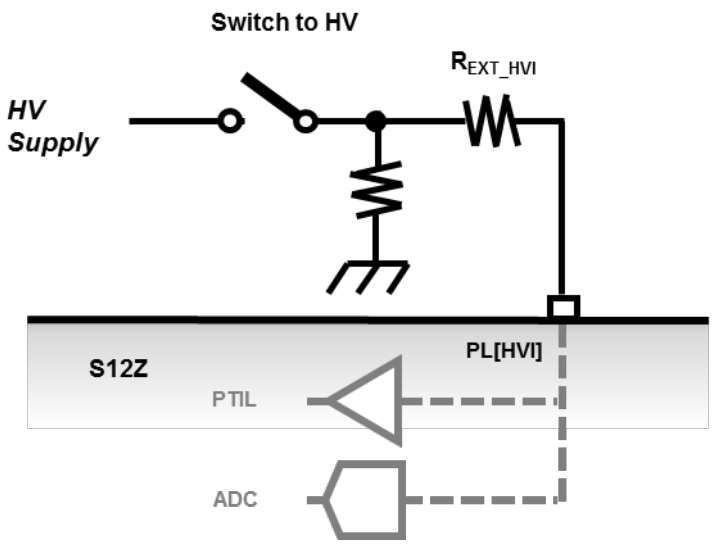


Figure 10. Digital input read with Pull-up enabled

6.3 External pullup device

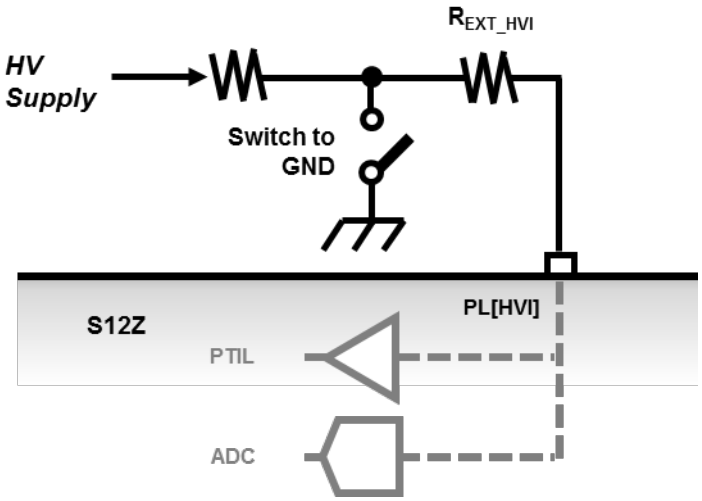


Figure 11. Digital input read with Pull-down enabled

7 Programmable Gain Amplifier (PGA)

The S12ZVLA128/96/64 family integrates an on-chip PGA (programmable gain amplifier) for a wide range of measurements. The PGA will be operated from the analog 5V power domain VDDA.

The PGA has the following features:

- Amplification of analog input signal with selectable gain of 10x, 20x, 40x, 80x
- Offset compensation
- Internal VDDA / 2 reference voltage generation or external signal as reference voltage
- Amplifier output connected to an ADC channel.

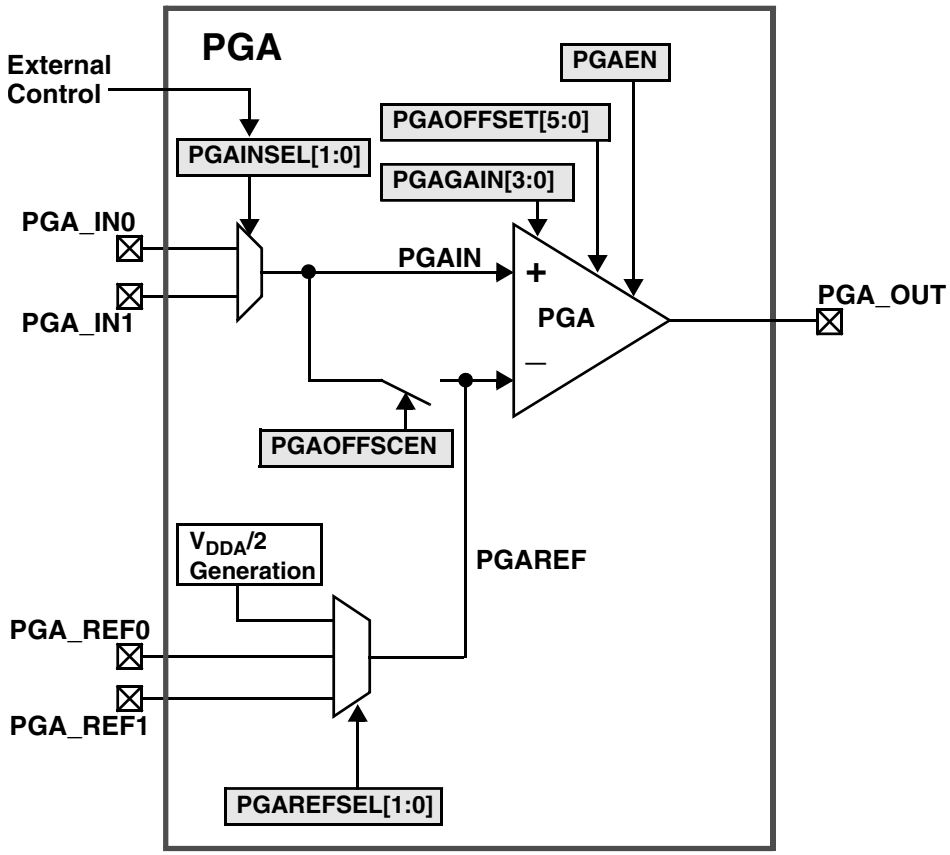


Figure 12. PGA block diagram

Table 5. PGA signals description

PGA input	Description
PGA_IN0	This analog pin is used as amplifier plus input voltage if the associated control register bit is set.
PGA_IN1	This analog pin is used as amplifier plus input voltage if the associated control register bit is set.
PGA_REF0	This analog pin is used as reference voltage and amplifier minus input voltage if the associated control register bit is set.
PGA_REF1	This analog pin is used as reference voltage and amplifier minus input voltage if the associated control register bit is set.
PGA_OUT	This analog pin provides the analog amplifier output voltage of the PGA as a function of the gain, offset and the reference voltage.

The output voltage for PGA_OUT as a function of PGAIN, PGAREF, gain and offset is calculated as follows:

$$VPGA\_OUT = VPGAREF + APGA * (VPGA\_IN - VPGA\_REF + Voffset)$$

Equation 2

If the PGA offset is well compensated and negligible in size compared to V_{PGAIN} - V_{PGAREF} the equation can be approximated by:

$$VPGA\_OUT = VPGAREF + APGA * (VPGA\_IN - VPGA\_REF)$$

Equation 3

After a change in the PGA inputs, the ADC conversion can be started after the settling time *tPGA_settling*.

7.1 Application example for differential voltage measurement

For sensor applications it is often required to measure a small differential voltage Vdiff. The PGA is not capable of amplifying a differential voltage, but an algorithm to calculate the differential voltage can be implemented. The PGA contains two input pins PGA_IN0 and PGA_IN1 which can be multiplexed by the ADC command list. By subtracting the ADC readings of the two pins the amplified differential voltage can be calculated.

For this algorithm two requirements must be met:

- The minimum time for the input signal multiplexing is given by PGA to ADC settling time *tPGA_settling*. The rate of signal change within *tPGA_settling* must be small.
- The common mode input voltage range of the differential input signals must be limited that for a given gain APGA a reference voltage Vref can be selected so that both amplified signals do not saturate.

While the chopper noise components are internally filtered, a minimal residual amount of high-frequency switching noise appears at the signal outputs. An external, passive, low-pass filter after the output stage is recommended to remove this switching noise; Figure 13 shows two examples. This filter can also be used to isolate or decouple the charge switching pulses of an ADC input.

$$V_{DIFF} = (V_{IN1} - V_{IN2}) * (1 \pm E_A)$$

Equation 4

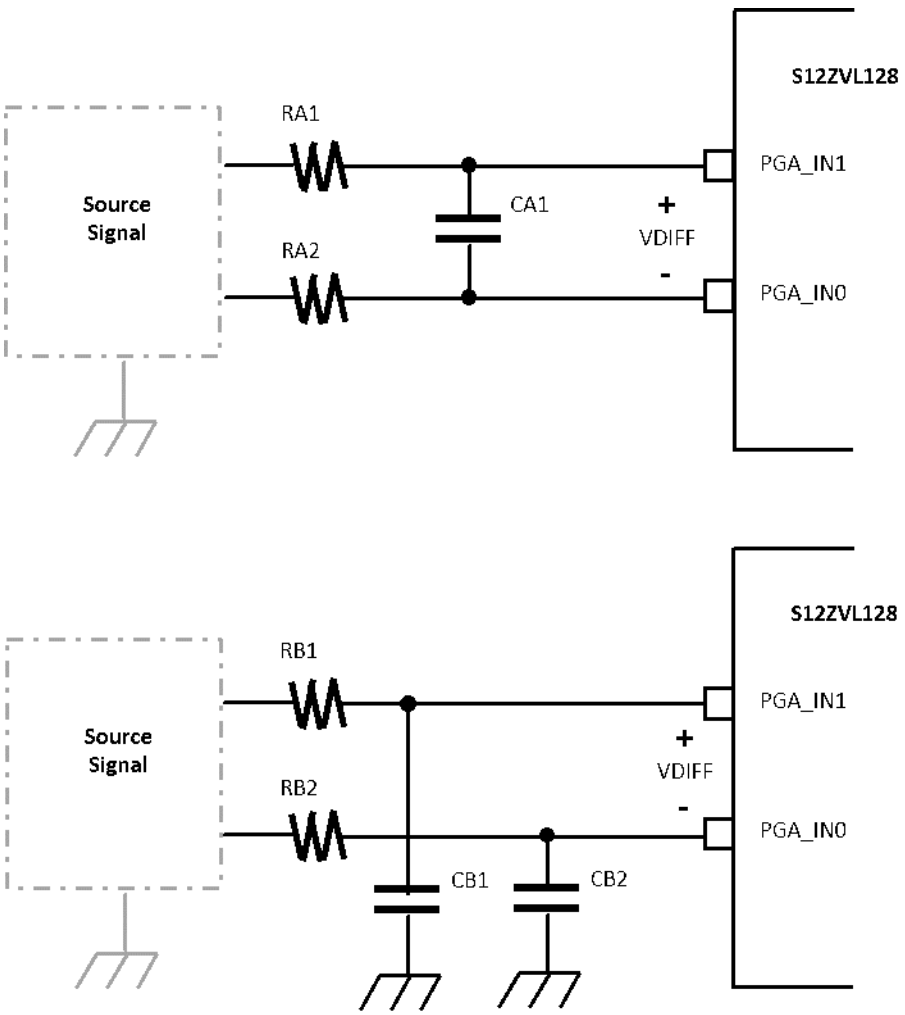


Figure 13. Examples of recommended Input filters for differential voltage measurement

For layout, the PGA traces and the digital domains must be separated, for example one could use extra grounded traces when physically possible. When that is not possible, try to use extra shielding between digital and the PGA tracks.

8 Analog Comparator (ACMP)

The S12ZVL(A)128/96/64 family integrates an on-chip ACMP, this module compares two analog voltages. The comparator circuit is designed to operate across the full range between 0V and VDDA supply voltage (rail-to-rail operation).

The ACMP has the following features:

- 0V to VDDA supply rail-to-rail inputs
- Low offset
- Up to 4 inputs selectable as inverting and non-inverting comparator inputs:
  - 2 low-impedance inputs with selectable low pass filter for external pins
  - 2 high-impedance inputs with fixed filter for SoC-internal signals
- Selectable hysteresis
- Selectable interrupt on rising edge, falling edge, or rising and falling edges of comparator output
- Option to output comparator signal on an external pin with selectable polarity
- Support for triggering timer input capture events
- Operational over supply range from 3 V-5% to 5 V+10%
- Temperature range (TJ): -40°C to 150°C.

The ACMP compares the analog voltage between inverting and non-inverting inputs. It generates a digital output signal and a related interrupt if enabled. The comparator output is high when the voltage at the non-inverting input is greater than the voltage at the inverting input, and is low when the non-inverting input voltage is lower than the inverting input voltage. The size of the ACMP hysteresis can be adapted to the specific application to prevent unintended rapid switching. One out of four hysteresis levels can be selected by setting ACMPC0[ACHYS]. The input delay of the ACMP_0 and ACMP_1 input depends on the selected filter characteristic by ACMPC0[ACDLY].

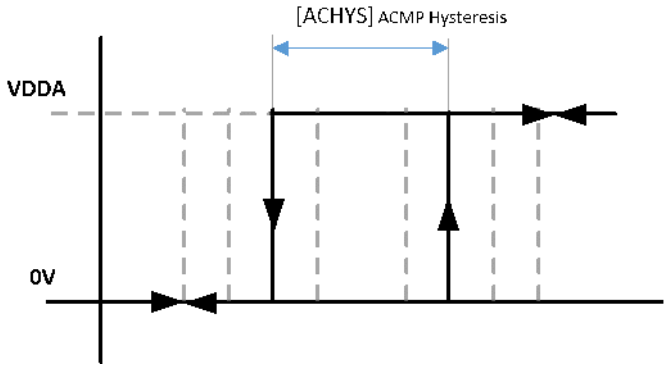


Figure 14. Hysteresis transfer curve

9 Inter-Integrated Circuit IIC

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 15). When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open collector in order to perform the wired-AND function.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

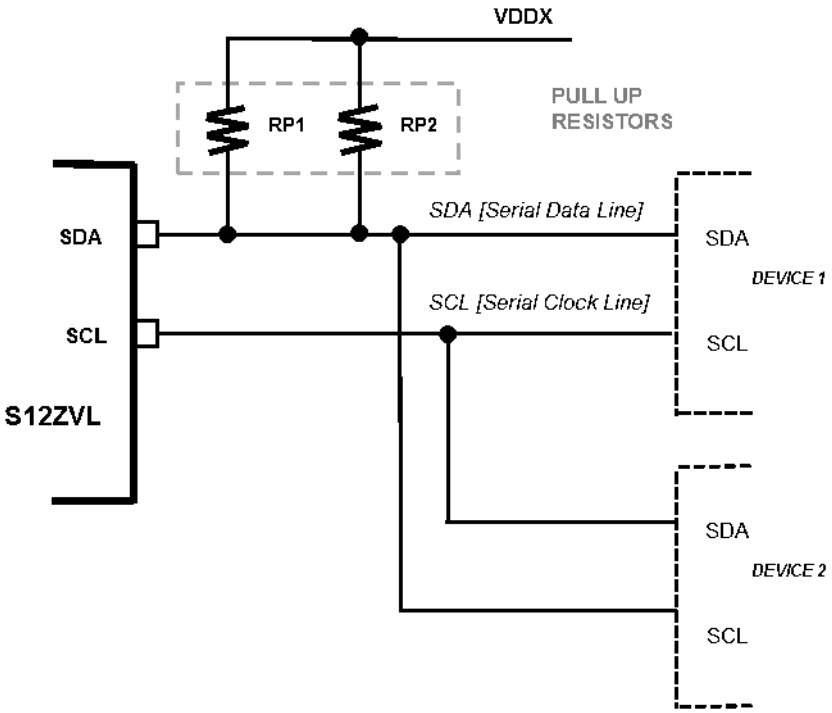


Figure 15. Connection of I2C-bus devices to the I2C-bus

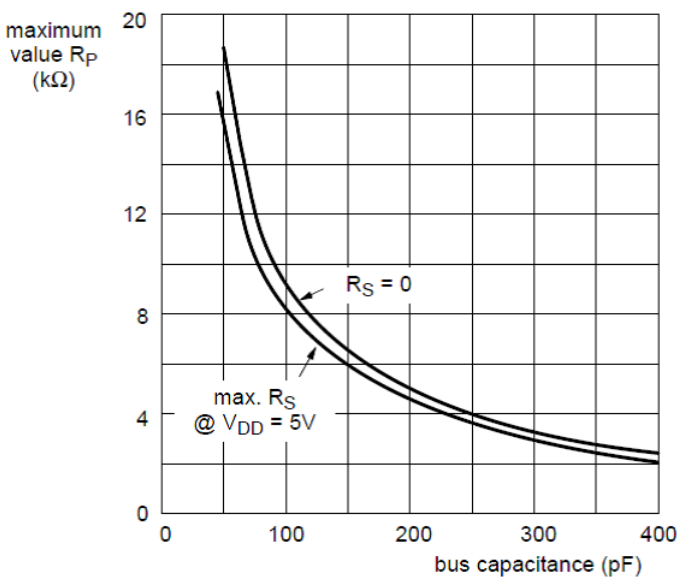


Figure 16. Maximum value of RP as a function of bus capacitance for a standard-mode I2C-bus LIN physical layer

10 MSCAN Interface

The S12ZVL(A)128/96/64 family includes the MSCAN module. The module is a communication controller implementing the CAN 2.0A/B protocol as defined in the Bosch specification dated September 1991. Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. A typical CAN system with MSCAN is shown in below figure.

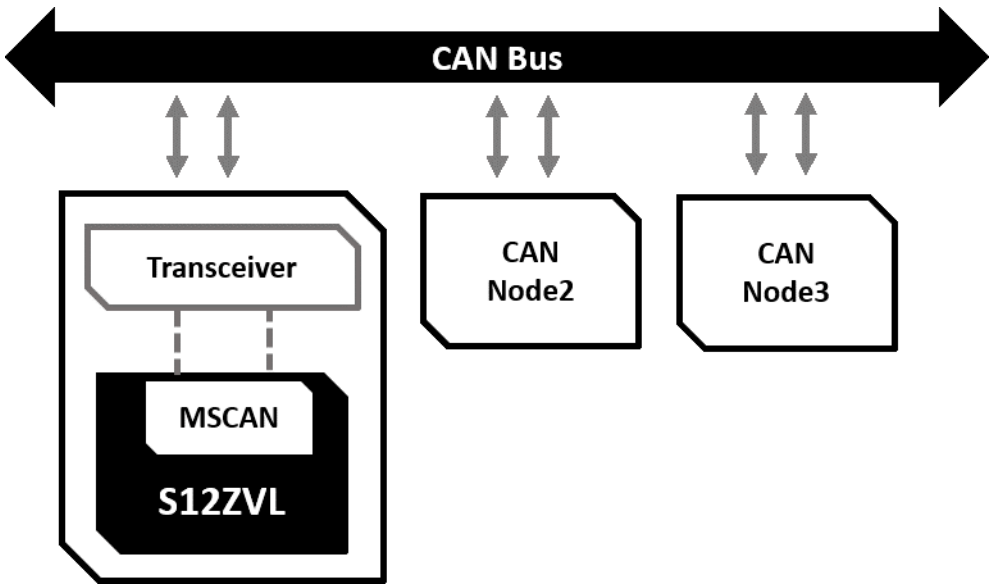


Figure 17. CAN system

11 LIN Interface Circuit

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification.
- Compliant with the SAE J2602-2 LIN standard.
- Standby mode with glitch-filtered wake-up.
- Slew rate selection optimized for the baud rates: 10.4 Kbit/s, 20 Kbit/s and Fast Mode (up to 250 Kbit/s).
- Switchable 34 kΩ/330 kΩ pull up resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge.
- Overcurrent protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.

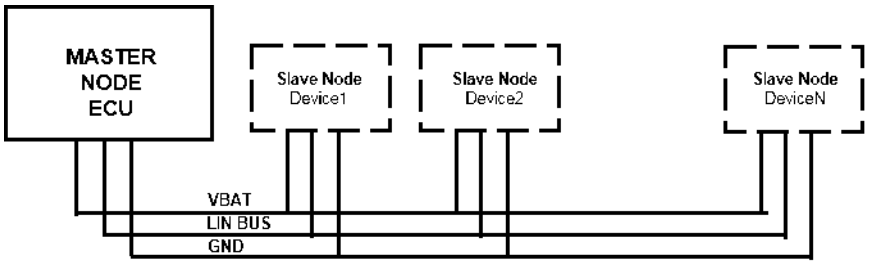


Figure 18. LIN bus topology

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull up resistor with a serial diode structure is integrated, so no external pull up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

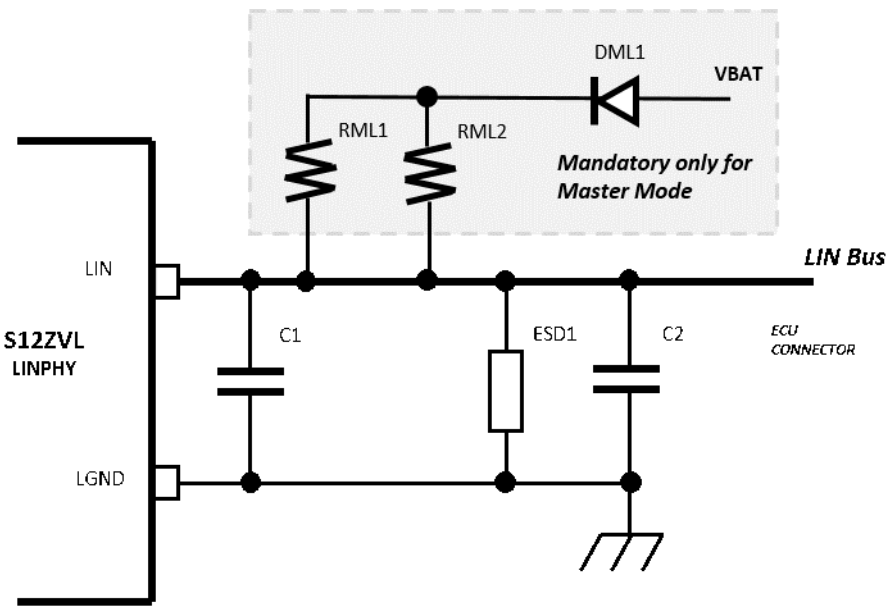


Figure 19. Circuit diagram for LIN interface

11.1 13.1 LIN Components Data

Table 6. LIN components

Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RML1 and RML2	Resistor: 2k Ω Power Loss: 250mW Tolerance: 1% Package Size: 1206	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values have to be chosen in a way that the overall resistance RM of 1kΩ and the minimum

Table continues on the next page...

Table 6. LIN components (continued)

	Requirement: Min Power rating of the complete master termination has to be ≥ 500mW		power loss of the complete master termination has to be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout
C1	Capacitor: Slave ECU: typically 220pF Master ECU: from 560pF up to approximately ten times that value in the slave node [CSLAVE], so that the total line capacitance is less dependent on the number of slave nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50V	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.
ESD1	ESD Protection Package Size: 0603 -0805	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

12 Unused pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents. The EXTAL and XTAL pins default reset condition is to have pull-downs enabled. These pins should be connected to ground if not used.

The voltage regulator controller pin BCTL should be left unconnected if not used, and the VDDX voltage regulator must be configured to operate with the internal power transistor by setting the appropriate register (CPMUVREGCTL register, bit EXTXON = 0, bit INTXON = 1). If the VDDC regulator is not used, the VDDC pin must be shorted with VDDX, and the BCTLC pin must be left unconnected.

13 General Board Layout Guidelines

13.1 Traces Recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in the below figure.

Figure 20. Poor and correct way of bending traces in right angles

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

13.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

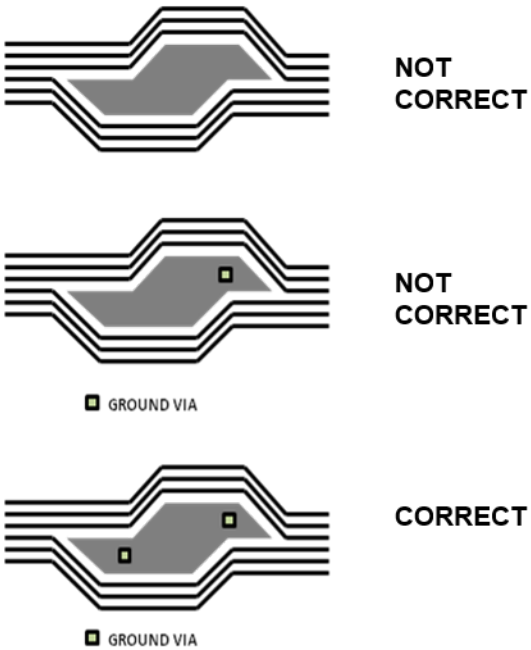


Figure 21. Eliminating floating metal/shape

13.2.1 Dealing with two-layer board

If the project does not afford the cost of four-layer board, then for a two-layer board you need to use Multi-Point-ground. You need to make every effort to reduce coupled noise. Provide as much ground area as possible, instead of running several traces, use shorter and wider traces. As the (return) current always flows back to source, avoid large loops. They are quick to couple noise from the electromagnetic radiations.

Separate high/medium-speed signals (e.g., clock signals) from PWM signals and digital from analog signals; the placement is important.

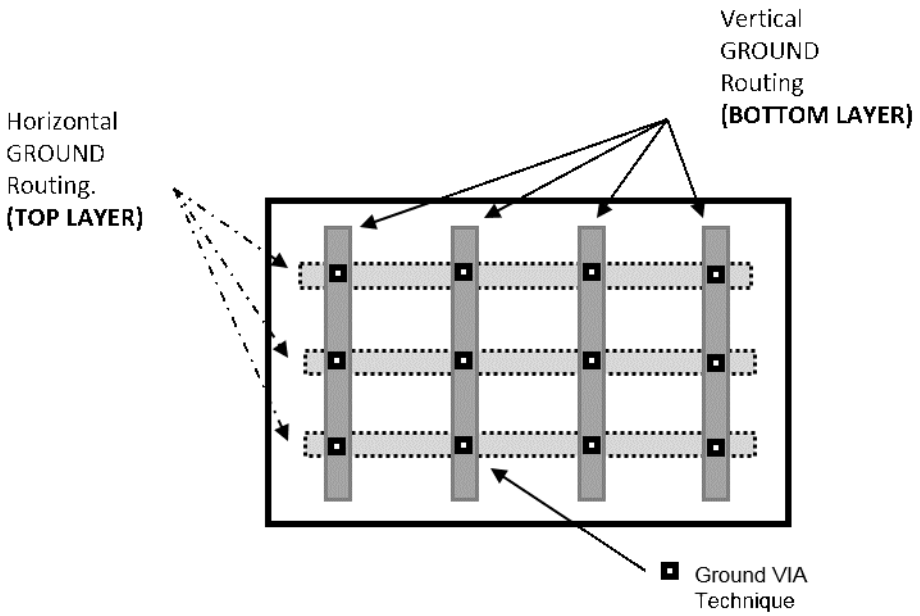


Figure 22. Layout considerations for PCBs of two layers

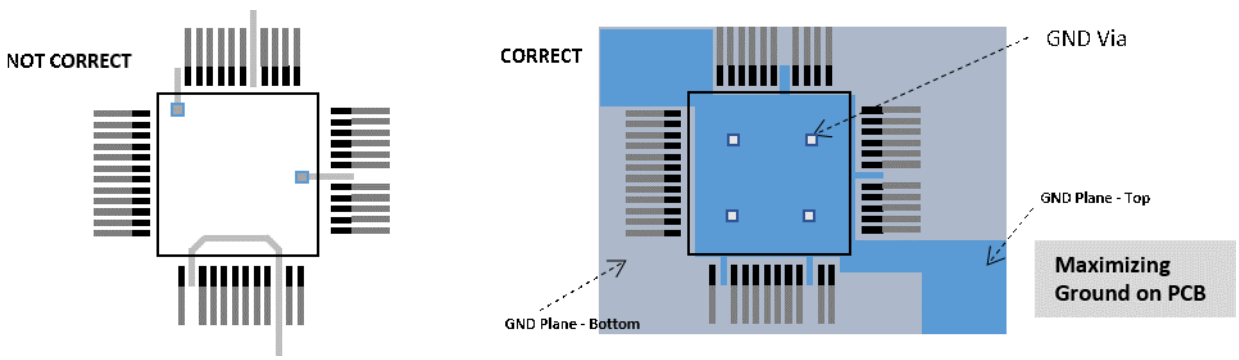


Figure 23. Layout considerations for the GND plane of the microcontroller

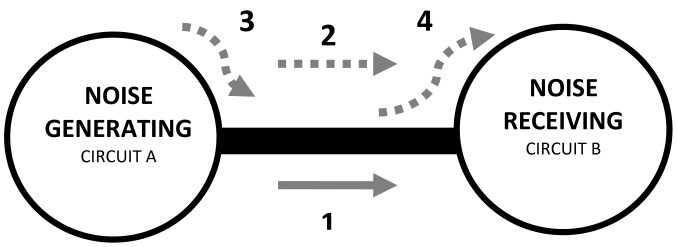
NOTE

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

13.3 EMI/EMC and ESD Considerations for Layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 24. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated & conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables, etc. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

14 References

- AN2727
- AN3208
- AN3335
- AN4219

- AN2536
- Basic ThermalWP

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