

## Digital Logic Design (EE1005)

## Sessional-II Exam

Course Instructor(s):

Ms. Mehreen Javaid, Mr. Muhammad Sohail Abbas

Section(s): DS-(A,B), AI(A,B,C)

Total Time (Hrs): 1

Total Marks: 45

Total Questions: 6

Date: Apr 8, 2025

Roll No

Course Section

Student Signature

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Attempt all the questions.

1. Attempt all questions on this question paper. You may take extra sheet for rough work but it will not be marked.

[CLO 3: Design combinational and sequential logic circuits]

Q1: Design the circuit to detect if a 3-bit binary number is a multiple of 3 or 5. You must follow all steps of design procedure to get complete marks. [10 marks]

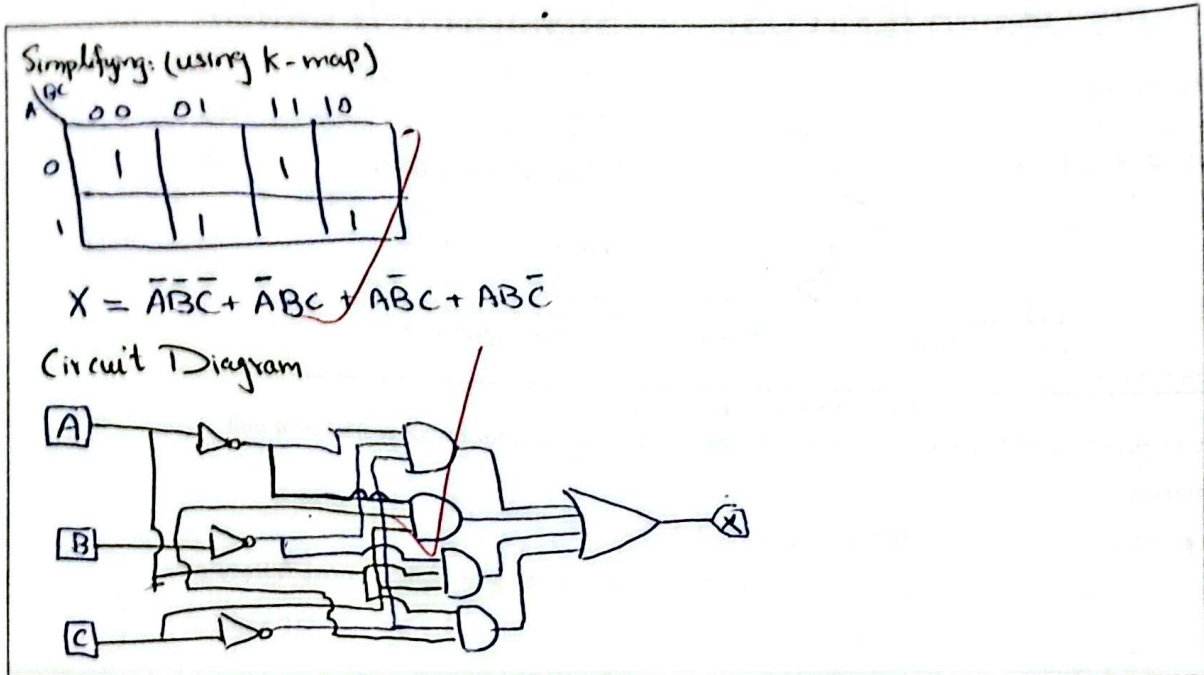
Total inputs = 8

Total outputs = 4

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

CLO 3 = 13  
CLO 2 = 0

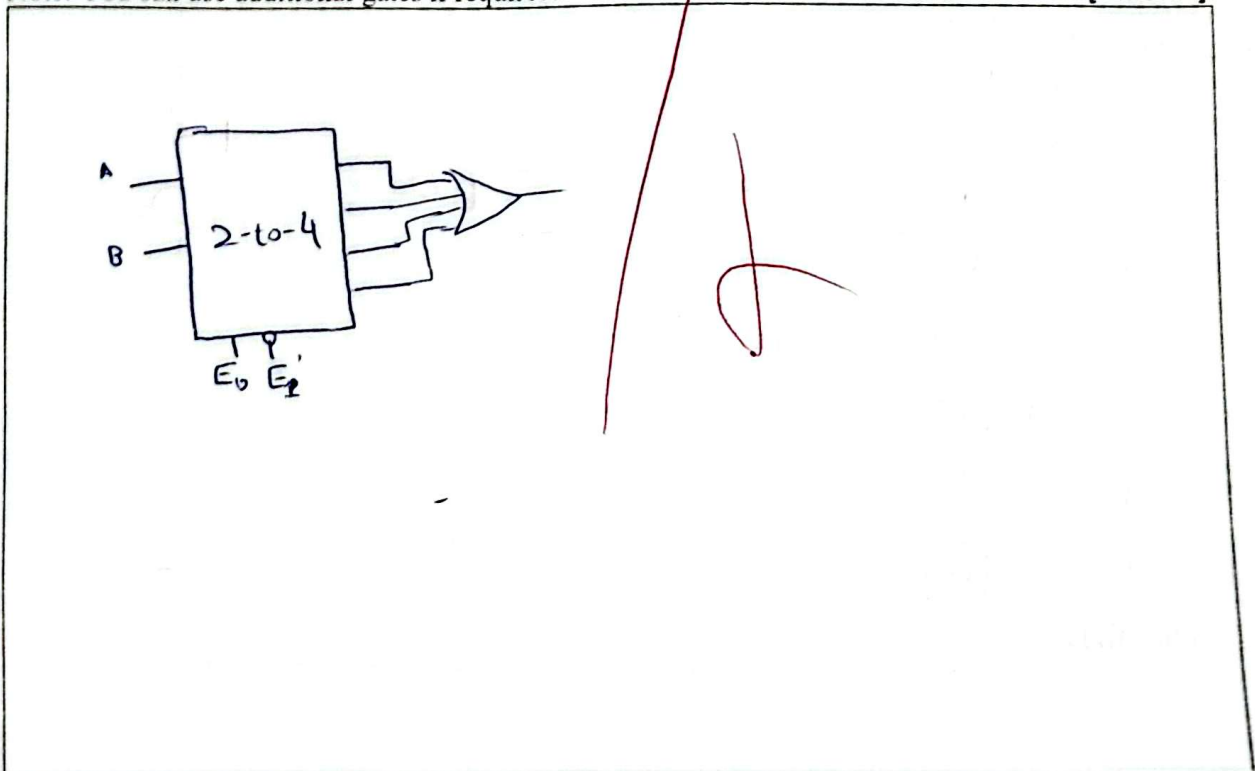


[CLO 3: Design combinational and sequential logic circuits]

**Q2:** Using 2-to-4 decoder, design a system that detects prime numbers between 0 and 7. Assume outputs are active low and 2 enable pins (one is active high and one is active low).

Note: You can use additional gates if required.

[5 marks]



[CLO 2: Analyze combinational and sequential logic circuits]

Q3: Derive equations of output A and B using k-map of 4x2 low priority encoder.

[5 marks]

$D_3 D_2$	00	01	11	10
00	✓	⊙	×	⊙
01	✓	⊙	×	×
11	✓	✓	×	×
10	⊙	×	×	×

$D_3 D_2$	00	01	11	10
00	×	⊙	×	1
01	⊙	×	×	×
11	×	×	✓	×
10	1	×	×	×

Output A

$$A = (D_3 + D_2 + D_1 + \bar{D}_0)(D_3 + D_2 + \bar{D}_1 + D_0)$$

$$B = (D_3 + \bar{D}_2 + D_1 + D_0)(D_3 + D_2 + D_1 + \bar{D}_0)$$

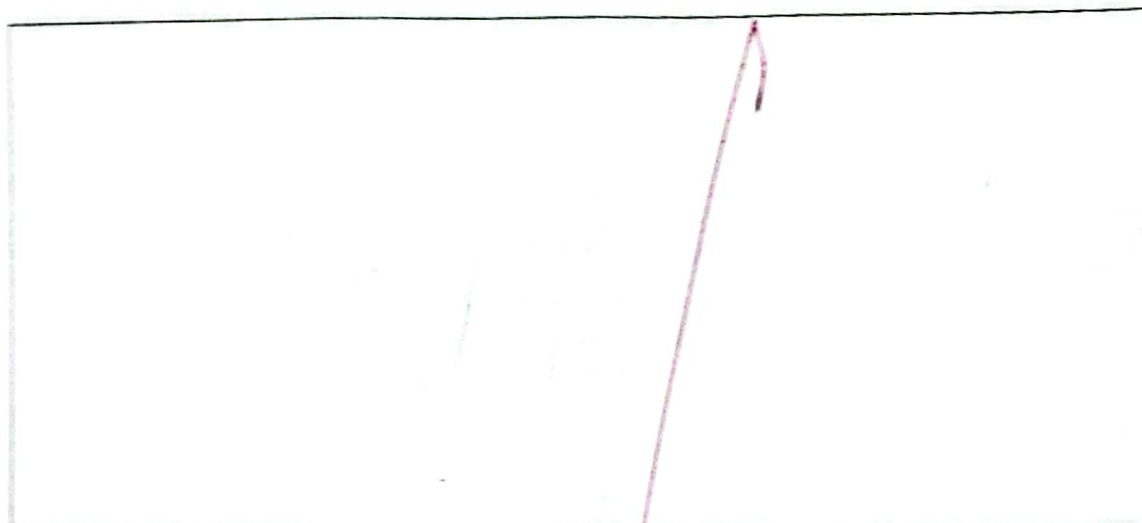
Zero

[CLO 2: Analyze combinational and sequential logic circuits]

Q4: How do we resolve the delay in carry? Assume that you are adding 2 numbers of 3-bit each. Explain with the help of equations. Your equations should be in variables of inputs or CO only. [8 marks]

We can resolve using carry look ahead adder. Normally: -

With CLA adder:-



[CLO 2: Analyze combinational and sequential logic circuits]

Q5: Let say we have following equation to check if  $A > B$ . What is wrong with this equation and how to fix it. Why is fixing required? A0-A4 and B0-B4 are 4-bit numbers.

[5 marks]

$$A_0 \cdot \overline{B_0} + A_1 \cdot \overline{B_1} + A_2 \cdot \overline{B_2} + A_3 \cdot \overline{B_3}$$

zero

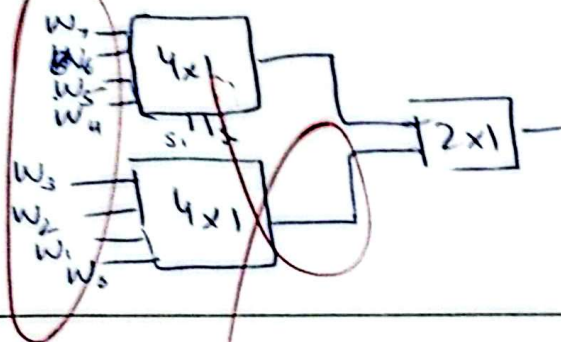
There is nothing wrong with this equation but it is not an optimal solution.

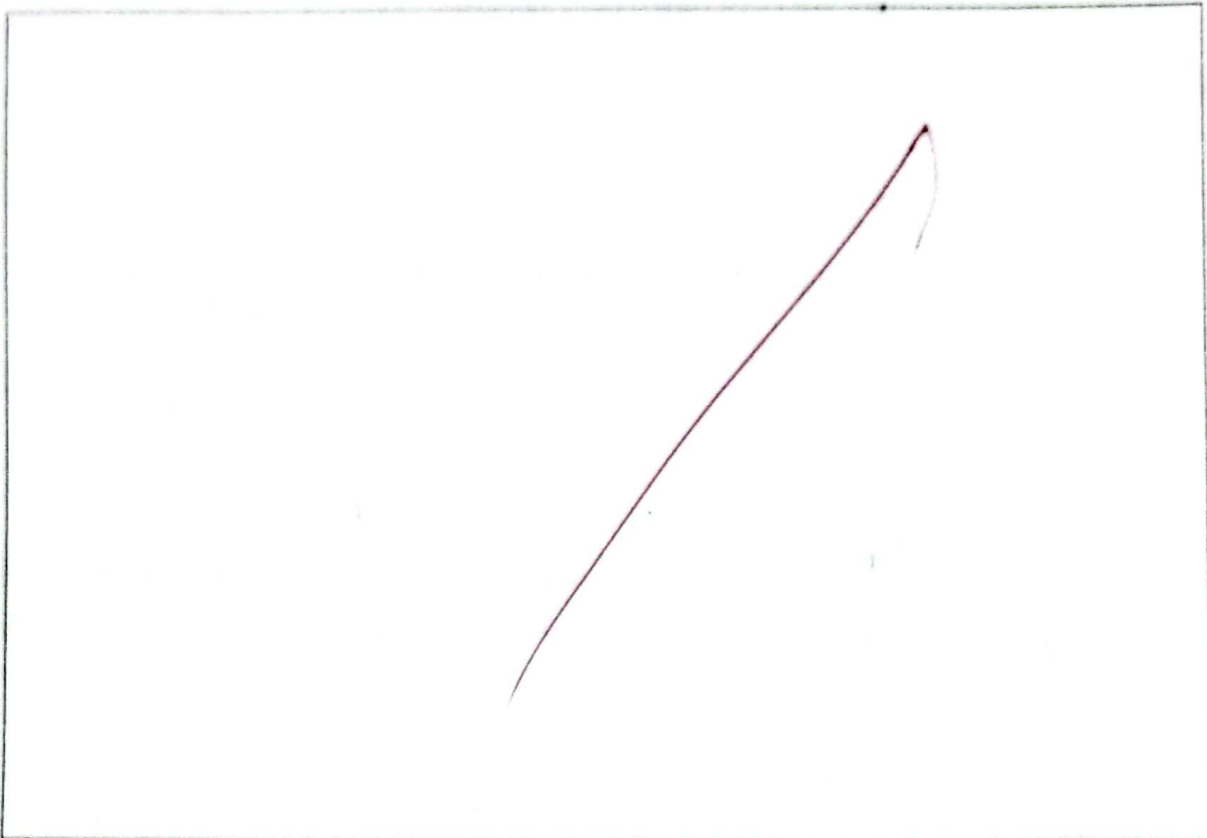


Q3: Analyze combinational and sequential logic circuits]

Q6: Using MUX, design a circuit for a smart warning system for seat belts in a car. Assume that we have four input parameters including Seat Occupied (O), Seat Belt Fasten (F), Car Ignition (I), Car in Motion (M). The warning (W) should appear if the seat is occupied, the car is turned on, and the seatbelt is not fastened. Or if the seat is occupied, the car is in motion, and the seatbelt is not fastened. Draw the truth table first. You must not use any MUX bigger than 4x1 and there shouldn't be more than 3 MUX in total. [12 marks]

O	F	I	M	W
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0





**Rough Work**