National University of Computer and Emerging Sciences

FAST School of Computing Spring-2023 Islamabad Campus

Serial No:

Final Exam
Total Time: 3 Hours
Total Marks: 145

_____
Signature of Invigilator

EE-1005: Digital Logic Design Solution

Monday, 27th May, 2023

Course Instructors

Dr. Mehwish Hassan, Dr. Niaz Ahmed, Shehzad Ahmad, Dr. Muhammad Awais, Nirmal Tariq

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Student Name	Roll No.	Course Section	Student Signature

DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

Instructions:

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **twenty-two (22)** different printed pages including this title page. There are total of **10** questions.
5. Calculator sharing is strictly prohibited.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. **Please note that any error carried forward shall not be taken into account during the grading**

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	Q-1	Q-2	Q-3	Q-4	Q-5	Q-6	Q-7	Q-8	Q-9	Q-10	Total
Marks Obtained											
Total Marks	**20**	**08**	**10**	**10**	**20**	**10**	**15**	**30**	**10**	**12**	**145**

Question 1 [20 Marks]

Question 1 (20 marks)

Answer the following multiple-choice questions on Page

1. The binary number 011011101 is equal to the decimal number

a) 121

b) 221

c) 441

2. The subtraction of 1111 and 0111 in binary equals

a) 1000

b) 1010

c) 1100

3. The decimal number +122 is expressed in 2's complement form as

a) 01111010

b) 11111010

c) 01000101

d) 01011101

4. The binary number 101100111 001 010 100 001 can be written in octal as

a) $(5471230)_8$

b) $(5471241)_8$

c) $(2634521)_8$

d) $(23162501)_8$

5. The binary number 1000 1101 0100 0110 1111 can be written in hexadecimal as

a) $(AD467)_{16}$

b) $(8C46F)_{16}$

c) $(8D46F)_{16}$

6. A BCD-to-7 segment decoder has 0011 on its inputs. The active outputs are

a) a, c, f, g, d

b) b, c, f, g, a

c) a, b, c, d, g

7. The Boolean function $D(1 + B) + A(C + \overline{C}) + B(A\overline{A} + 0)$ simplifies to

a) $D + AC$

b) $A + B + D$

c) $A + D$

8. The output of a NAND gate with inputs A, B and C is 0 (LOW) when

a) A =0, B = 0, C = 0

b) A =1, B =1, C = 0

c) A =1, B =1, C = 1

9. A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at = 3 ms. The output pulse can be described as

a) It goes LOW at t = 0 and back HIGH at t = 3 ms.

b) It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms.

c) It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms.

10. All Boolean expressions can be implemented with

a) AND Gate

b) OR Gate

c) NAND Gates

11. The AND operation can be produced with

a) Two NAND gates

b) Three NAND gates

c) Three NOR gates

12. 12. The result of the following expression in base-16 (hexadecimal) arithmetic? (A8 + B2) - 3E

a) 6A

b) D4

c) 7C

d) F2

13. What do we get if we simplify the following Boolean expression: (A' + B) . (A + C') . (B' + C)

a) A' + B' + C'

b) A' . B' . C'

c) A' + B + C

d) A . B . C

14. A decimal number 87 in octal is represented as

a) 127

b) 117

c) 126

d) 106

15. Evaluating the following arithmetic expression in binary: (1011 + 110) + (111 - 10) results in

a) 11100

b) 10110

c) 11101

d) 10101

16. What is the result of the following bitwise operation: ~(1010 & 1100)

a) 1010

b) 0101

c) 1111

d) 0000

17. Simplifying the following Boolean expression using Boolean algebra laws: (A + B) . (A' + B) will result in

a) AB

b) A+B

c) AB'

d) A'+B

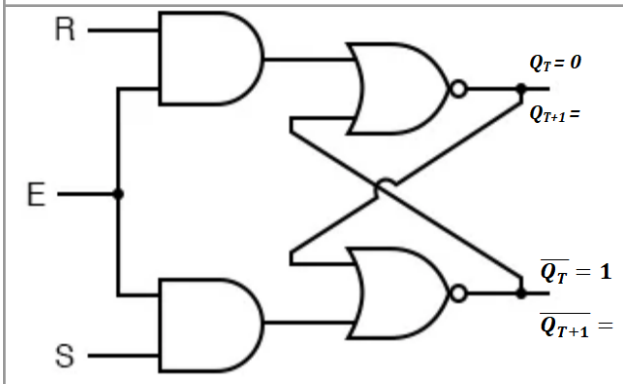
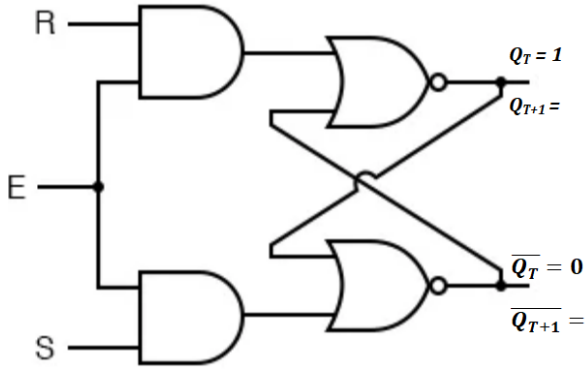
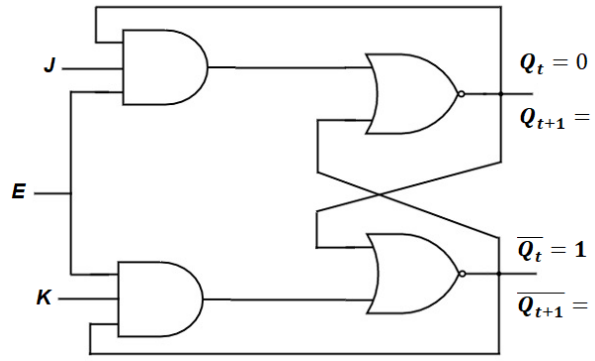
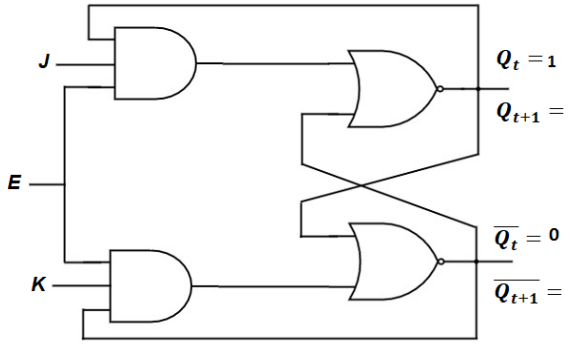
18. If the binary number 10100011 is ANDed with the mask 00001111, what is the result ____**00000011**____

19. The fractional binary number 0.11 has a decimal value of ____**0.75**_____

20. The fractional decimal number 0.45 has a binary representation as ____**0.01110**_____

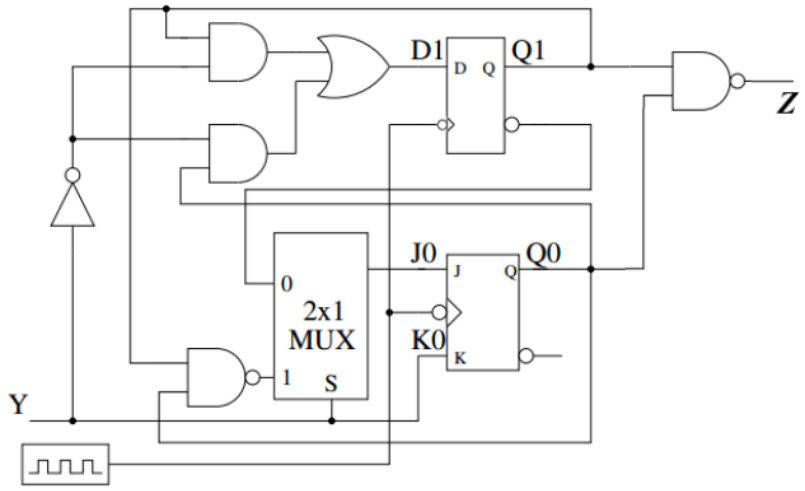
Question 2 (8 marks)
Process the **Gated SR and JK Latch** given below for all possible cases and fill the table accordingly?
NOTE: No marks will be given for direct answer.

CIRCUIT:

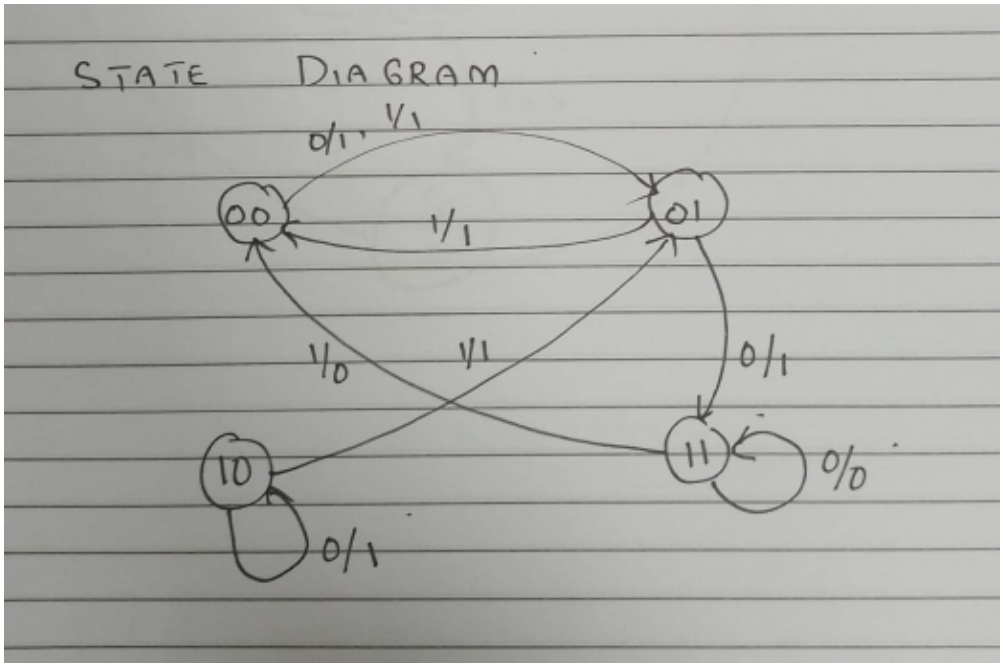
Case-I ($Q_t = 0$)	Case-II ($Q_t = 1$)
E=0, S= x , R= x , $Q_t = 0$, $Q_{t+1} = 0$	**E=0, S= x , R= x , $Q_t = 1$, $Q_{t+1} = 1$**
	
E=0, J= x , K= x , $Q_t = 0$, $Q_{t+1} = 0$	**E=0, J= x , K= x , $Q_t = 1$, $Q_{t+1} = 1$**
	

Question 3 (10 marks)

Derive the state table and state diagram of the following sequential circuit.

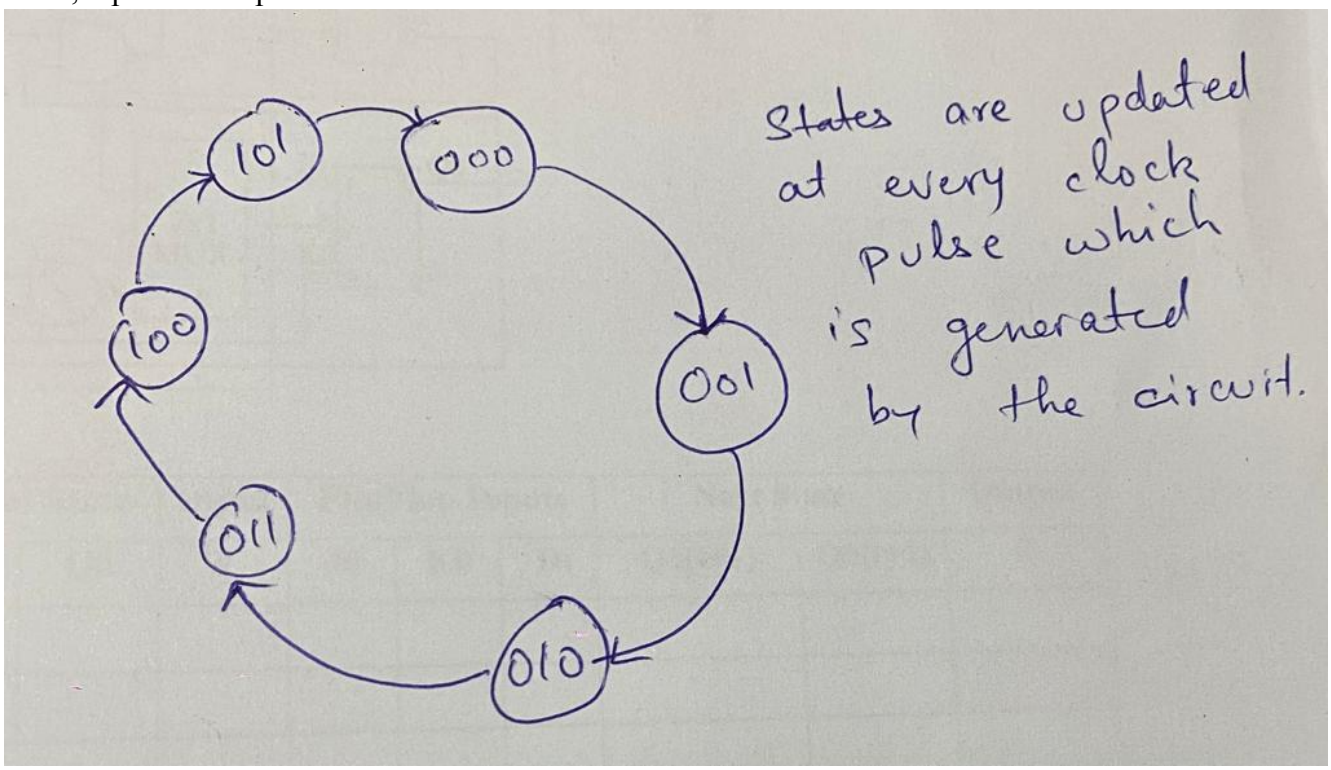


Present State		Input	FlipFlop Inputs			Next State		Output
Q1	Q0	Y	J0	K0	D1	Q1(t+1)	Q0(t+1)	Z
0	0	0	1	0	0	0	1	1
0	0	1	1	1	0	0	1	1
0	1	0	1	0	1	1	1	1
0	1	1	1	1	0	0	0	1
1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	1	1
1	1	0	0	0	1	1	1	0
1	1	1	0	1	0	0	0	0



Question 4 (10 marks)

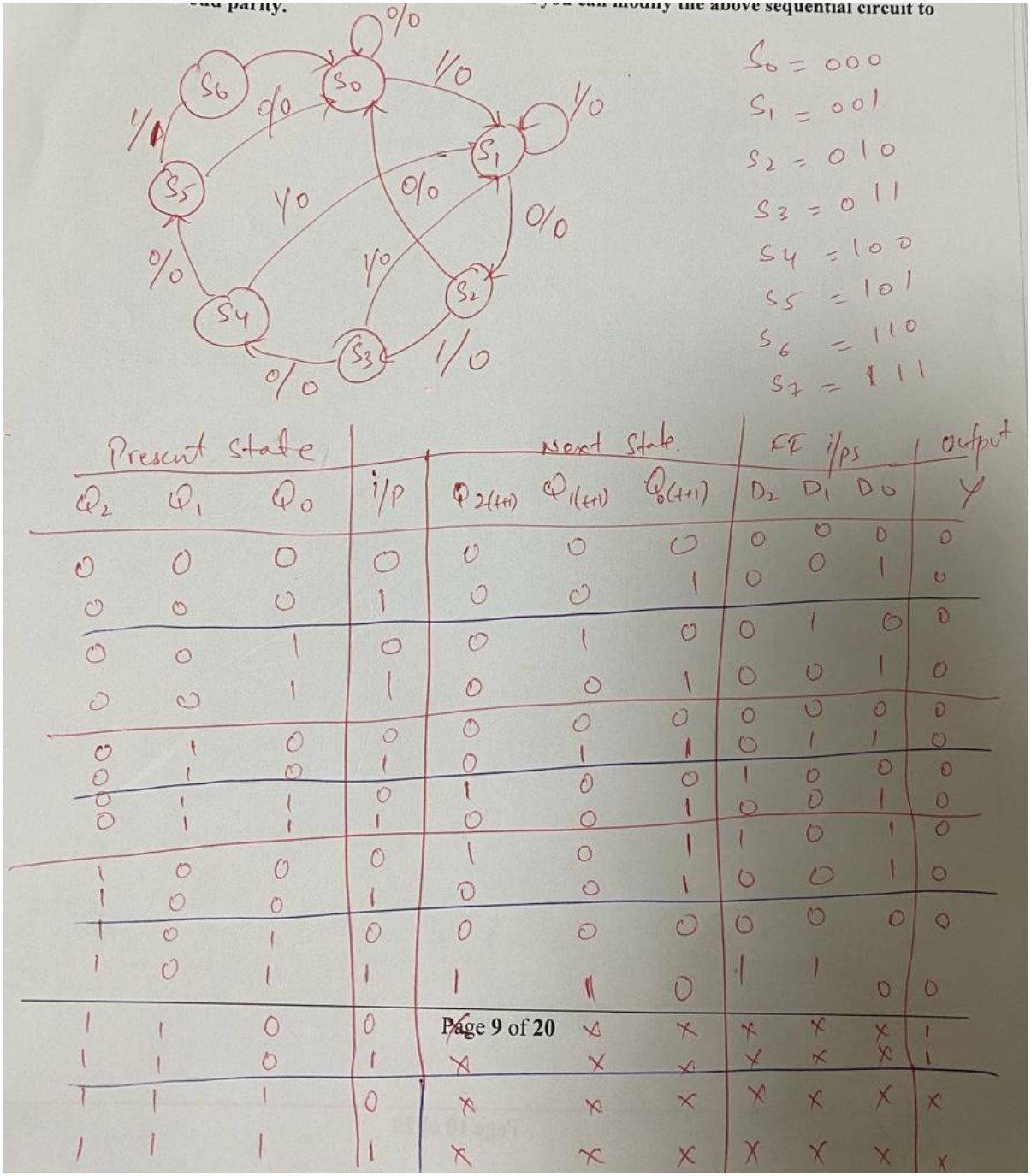
In the shipping department of a softball factory, the balls roll down a conveyor and through a slide into boxes for shipment. Each ball passing through the slide activates a switch circuit that produces a clock pulse. The capacity of each box is 5 balls. **Draw only the state diagram** of the given scenario to clearly indicate when a box is full so that an empty box can be moved into position. Clearly identify states, input and output

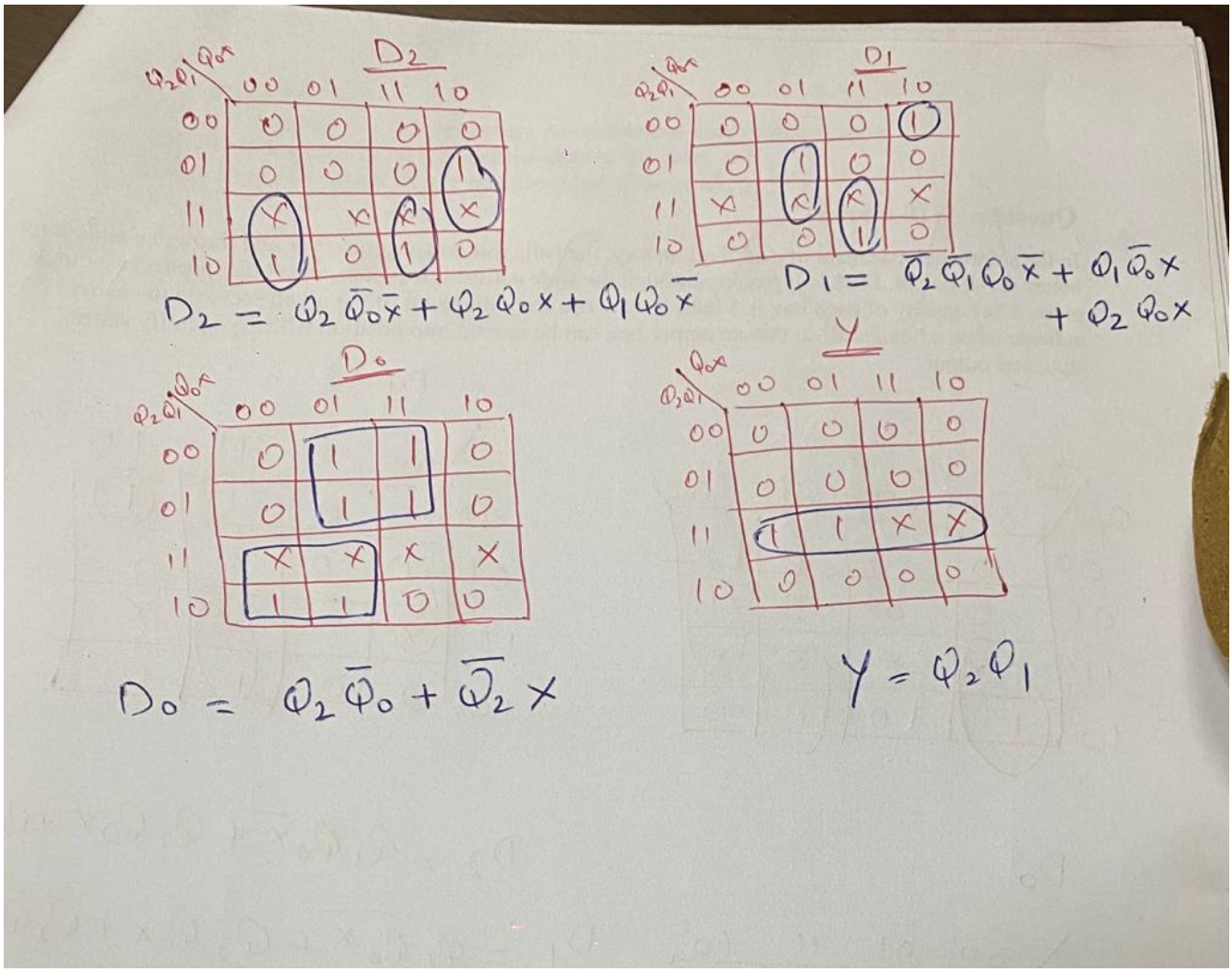


Question 5 (20 marks) Error carried forward will not be considered

Design a sequential circuit that can detect the given sequence 100101 (starting with LSB). Provide a detailed design description, including the state diagram (4 marks), state table (6 marks), equations (6 marks), and circuit diagram (4 marks) using **D Flipflop.**

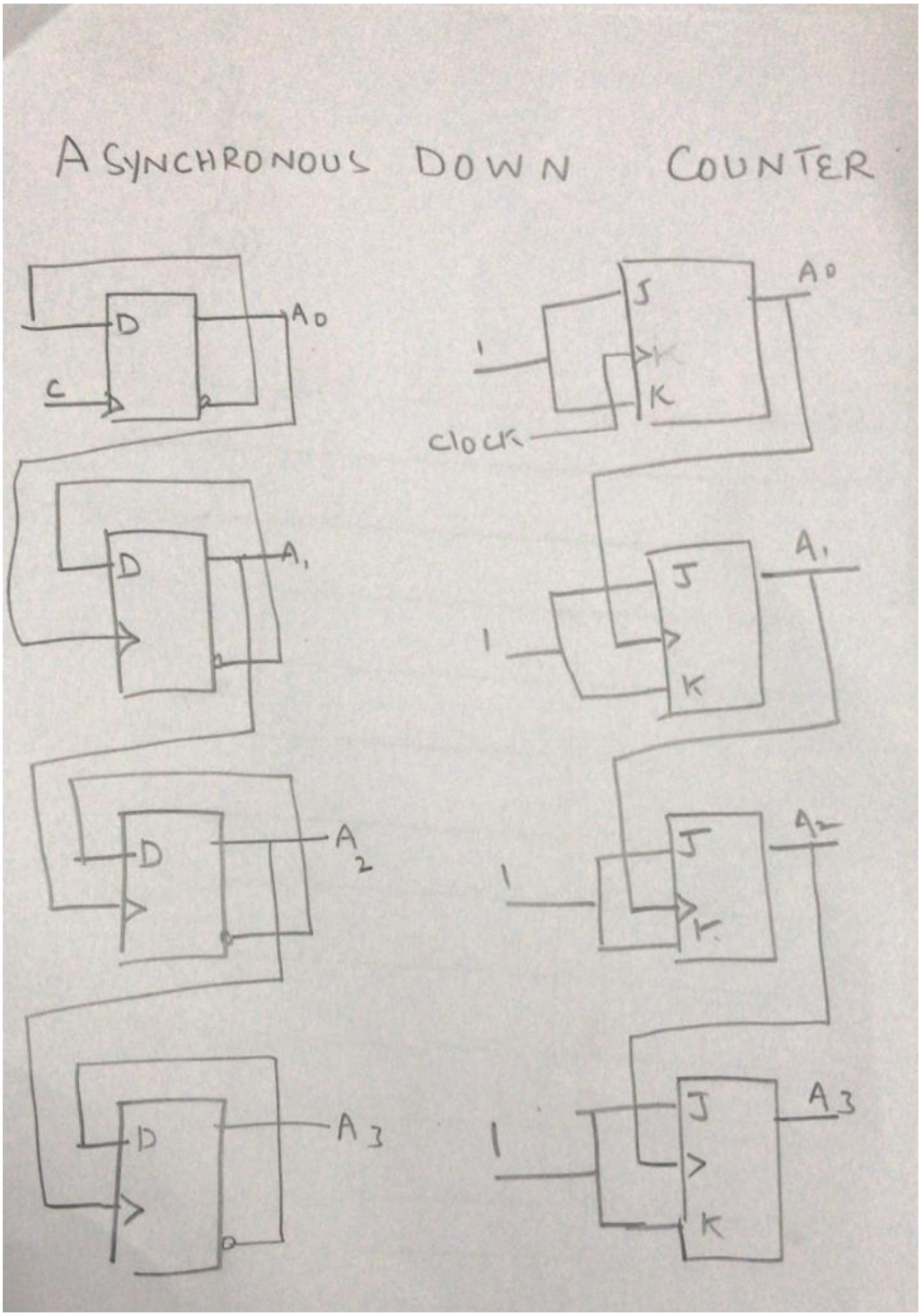
Bonus Marks: You will be given 5 bonus marks if you can modify the above sequential circuit to check for odd parity.




D2
D1
D0
Y
$D_2 = Q_2\bar{Q}_0\bar{x} + Q_2Q_0x + Q_1Q_0\bar{x}$
$D_1 = \bar{Q}_2\bar{Q}_1Q_0\bar{x} + Q_1\bar{Q}_0x + Q_2Q_0x$
$D_0 = Q_2\bar{Q}_0 + \bar{Q}_2x$
$Y = Q_2Q_1$

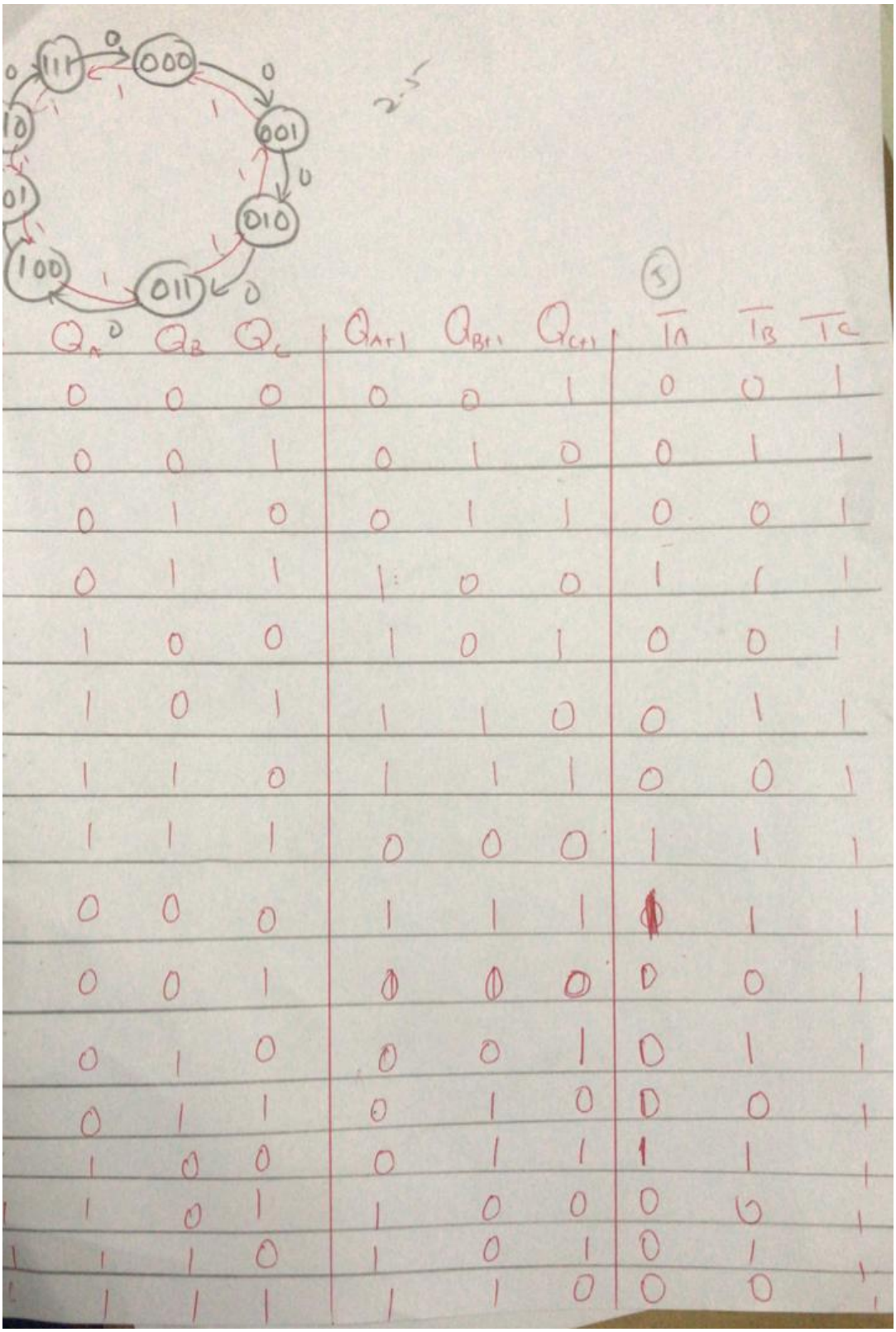
Question 6 (10 marks)

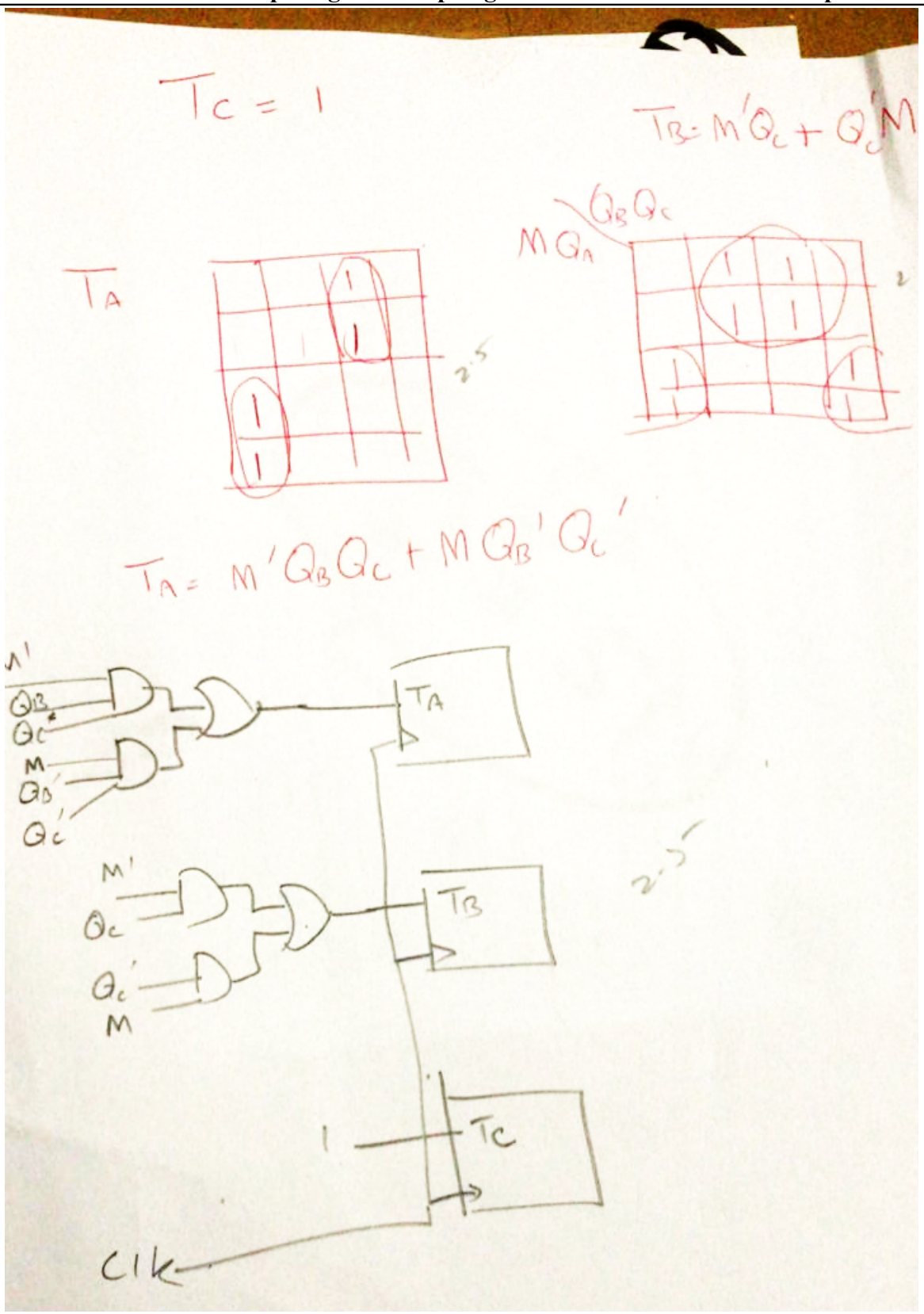
Draw the logic diagram of a four-bit binary Asynchronous down counter using
(a) D flip-flops that trigger on the positive-edge of the clock and
(b) JK flip-flops that trigger on the positive-edge of the clock.



Question 7 (16 marks)

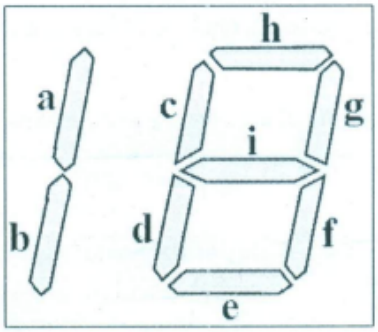
Design a synchronous **3-bit up/down counter** using '**T**' flip flops. The counter should **count up** when control input **'M'** is 0 and **count down** when the control input is 1. Clearly show each step of the design such as state diagram, state table, state equations and circuit diagram.



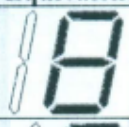
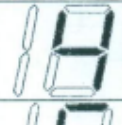

TC = 1
TB = M'QC + QC'M
QBQC
MQA
TA
TA = M'QBQC + MQB'QC'
M'
QB
QC
M
QB'
QC'
TA
M'
QC
QC'
M
TB
1
TC
Clk

Question 8 (30 marks)

You have worked with 7 segment displays in your class and labs. This question requires you to work with ***9-Segment Displays.*** The structure of the **9-Segment Display** is given below:



The **9-Segment Display** can be used to display decimal numbers from **0** to **15** as shown below:

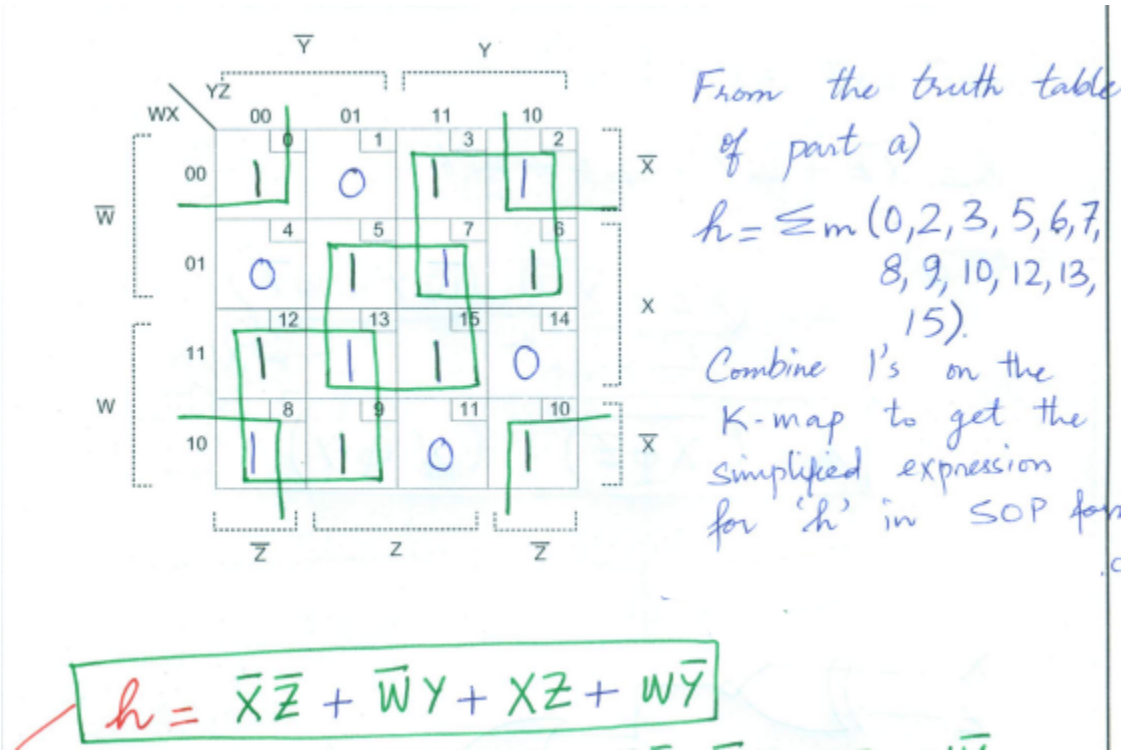
Digit	9 Segment Equivalent	Digit	9 Segment Equivalent
0		8	
1		9	
2		10	
3		11	
4		12	
5		13	
6		14	
7		15	

The following parts of the question require you to design a "***Binary to 9-Segment Display Decoder".*** This "***Binary to 9-Segment Display Decoder"*** takes four bits **(W, X, Y, Z)** at its input **(MSB: W and LSB: Z)** and generates nine outputs **(a,b,c,d,e,f,g,h,i)** to feed into the **9-segment display,** and turn ON/OFF the required LED segments**.** An LED Segment is turned ON if its corresponding bit (a or b or c, etc) is 1. Similarly, an LED Segment is turned OFF if its corresponding bit (a or b or c, etc) is 0.
Do as directed in the following parts:

a) Fill the **complete Truth Table** for the "***Binary to 9-Segment Display Decoder".*** **[16 Marks]**

Truth Table for Binary to 9-Segment Display Decoder												
Binary Inputs				Binary to 9-Segment Display Decoder Outputs								
W	X	Y	Z	a	b	c	d	e	f	g	h	i
0	0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	0	0	0	0	1	1	0	0
0	0	1	0	0	0	0	1	1	0	1	1	1
0	0	1	1	0	0	0	0	1	1	1	1	1
0	1	0	0	0	0	1	0	0	1	1	0	1
0	1	0	1	0	0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	0	1	1
0	1	1	1	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	0	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	0
1	0	1	1	1	1	0	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	0	1	1	1
1	1	0	1	1	1	0	0	1	1	1	1	1
1	1	1	0	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0	1	1	0	1	1

b) Derive a simplified expression for only output bit **"h"** of the ***Binary to 9-Segment Display Decoder*** using K-map (SOP form). **[5 Marks]**



c) Continuing with part-b), draw a **circuit diagram for the simplified expression of "h"** that you found. **You are required to use a mix of Complex (X-OR, etc) and Primitive (AND, OR, etc) Digital Logic Gates.**

[4 Marks]

From part b)

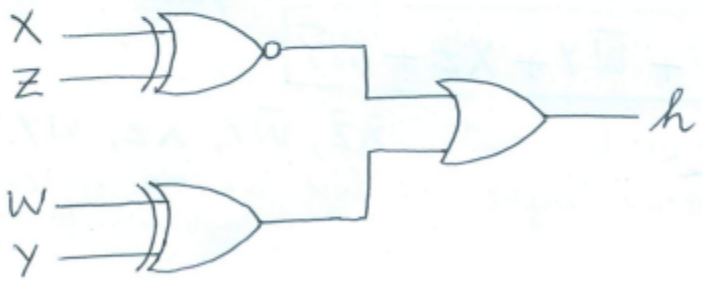
$$h = \bar{X}\bar{Z} + \bar{W}Y + XZ + W\bar{Y}$$

Re-arrange:

$$h = \underbrace{(XZ + \bar{X}\bar{Z})}_{\hookrightarrow \text{XNOR}} + \underbrace{(\bar{W}Y + W\bar{Y})}_{\hookrightarrow \text{XOR}}$$

$$\therefore \boxed{h = (\overline{X \oplus Z}) + (W \oplus Y)}$$

Circuit Diagram:



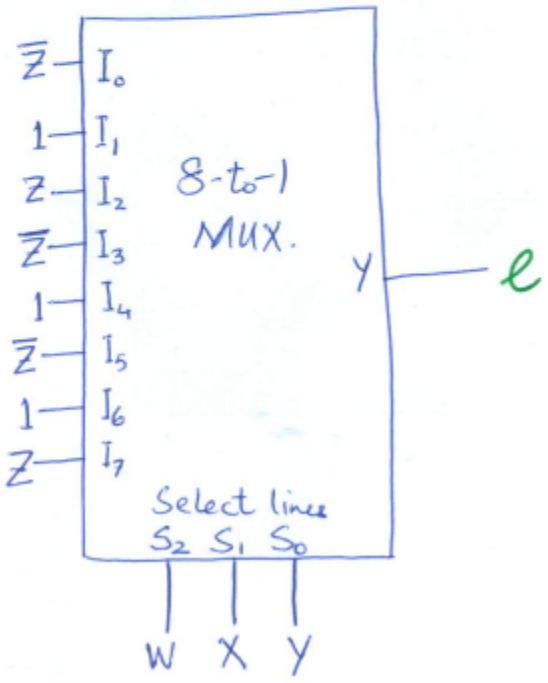
Complex Gates: XOR, XNOR

Primitive Gate: OR

d) You are now required to implement the **output bit "e" of the *Binary to 9-Segment Display Decoder*** by using an 8x1 MUX? **You are required to show your implementation here by drawing a diagram.** **[5 Marks]**

W	X	Y	Z	e	
0	0	0	0	1	$\bar{Z} = I_0$
0	0	0	1	0	
0	0	1	0	1	$1 = I_1$
0	0	1	1	1	
0	1	0	0	0	$Z = I_2$
0	1	0	1	1	
0	1	1	0	1	$\bar{Z} = I_3$
0	1	1	1	0	
1	0	0	0	1	$1 = I_4$
1	0	0	1	1	
1	0	1	0	1	$\bar{Z} = I_5$
1	0	1	1	0	
1	1	0	0	1	$1 = I_6$
1	1	0	1	1	
1	1	1	0	0	$Z = I_7$
1	1	1	1	1	

Number of inputs, $n = 4$
We will use a MUX
with $(n-1) = 3$ select lines
That is a 8-to-1 Line MU



Question 9 (10 marks)

Given diagram represents a Universal Shift Register. Table 1. represents the working of the given circuit.
NOTE: ZERO marks will be given for incomplete/incorrect implementation of the circuit.

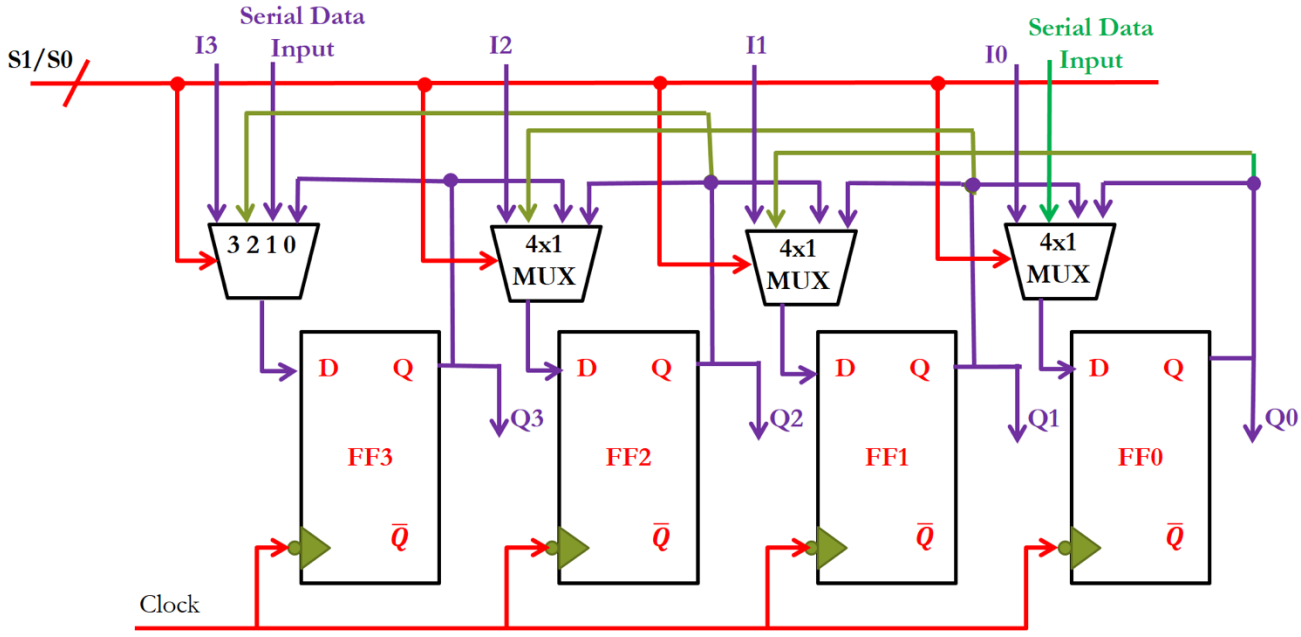


Figure Q9

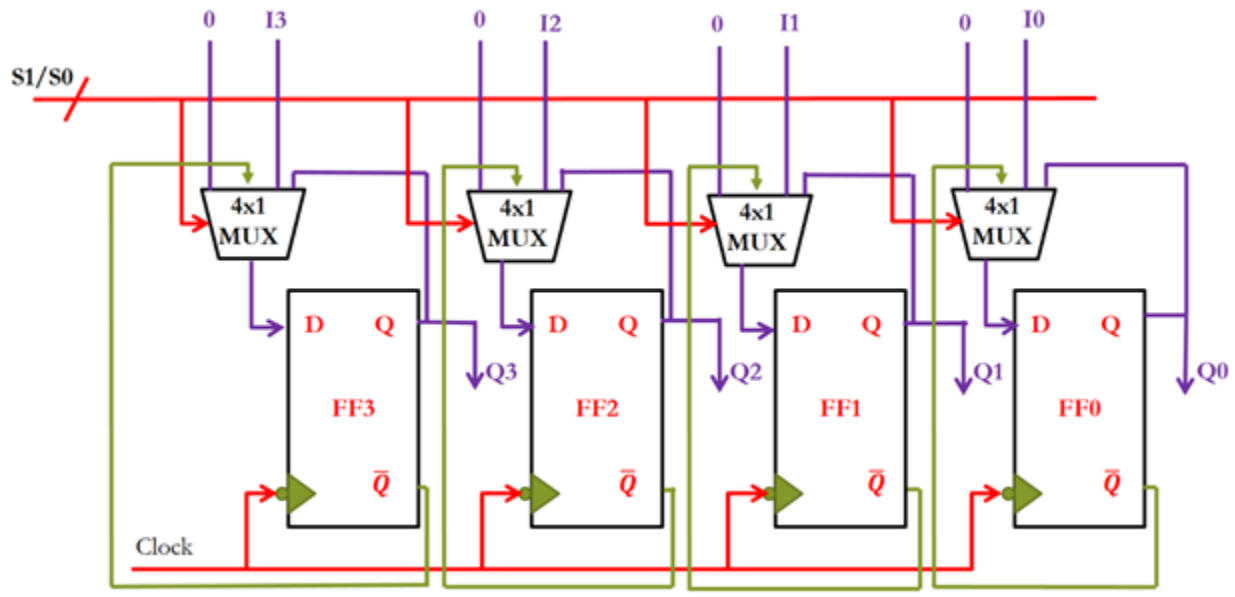
Table 1.

S1	S0	Operation
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Load Parallel Data

Modify the circuit to operate in a manner given in Table 2.

Table 2.

S1	S0	Operation
0	0	No Change
0	1	Load Parallel Data
1	0	Complement Output
1	1	Clear Register


0
I3
0
I2
0
I1
0
I0
S1/S0
4x1 MUX
4x1 MUX
4x1 MUX
4x1 MUX
D
Q
FF3
FF2
FF1
FF0
Q3
Q2
Q1
Q0
Clock

Question 10 (12 marks)

A bi-directional shift register is represented in the following Figure-Q10(a). Initially the Register stores the decimal number eight (8). Complete the timing table (at the end of the question) with respect to the state of control line represented in the Figure Q10(b).

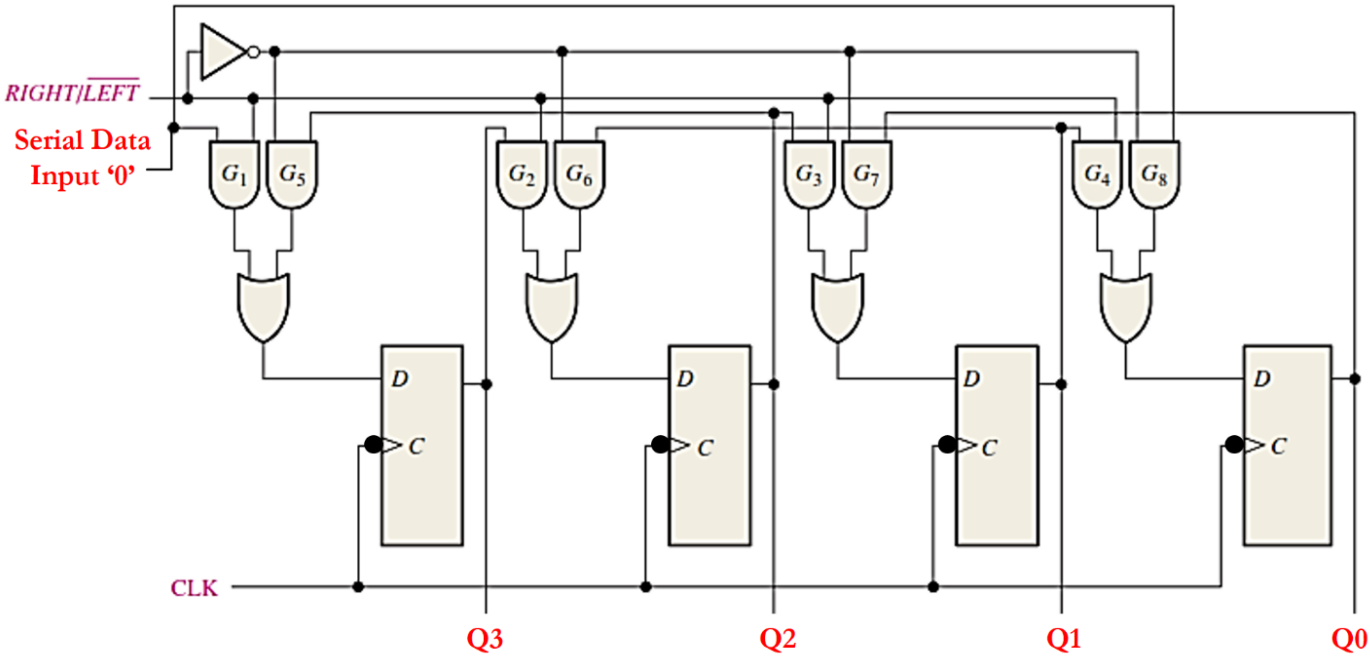


Figure-Q10 (a)

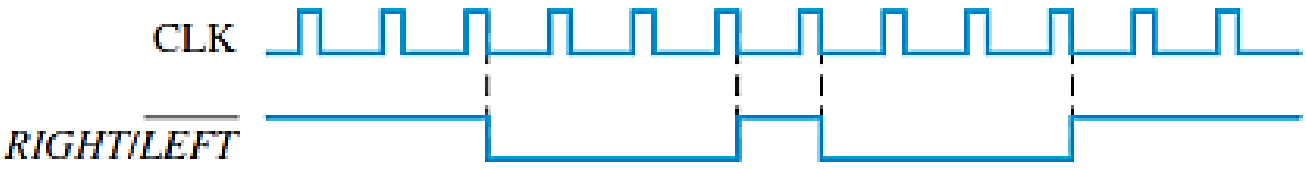


Figure-Q10 (b)

Timing Table:

Clock	Q3	Q2	Q1	Q0	Shift Direction
Initial Condition	1	0	0	0	
↓	0	1	0	0	Right
↓	0	0	1	0	Right
↓	0	0	0	1	Right
↓	0	0	1	0	Left
↓	0	1	0	0	Left
↓	1	0	0	0	Left
↓	0	1	0	0	Right

	1	0	0	0	Left
	0	0	0	0	Left
	0	0	0	0	Left
	0	0	0	0	Right
	0	0	0	0	Right

Rough Work