National University of Computer and Emerging Sciences

FAST School of Computing **Spring-2024** **Islamabad Campus**

EE-1005: Digital Logic Design

Final Exam

BS-CS & BS-SE

Date: 31st May, 2024

Total Time: 3 Hours

Total Marks: 130

Course Instructor(s)

Dr. Mehwish Hassan, Mr. Shams Farooq, Muhammad Aamir Gulzar

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Student Name	Roll No.	Course Section	Student Signature

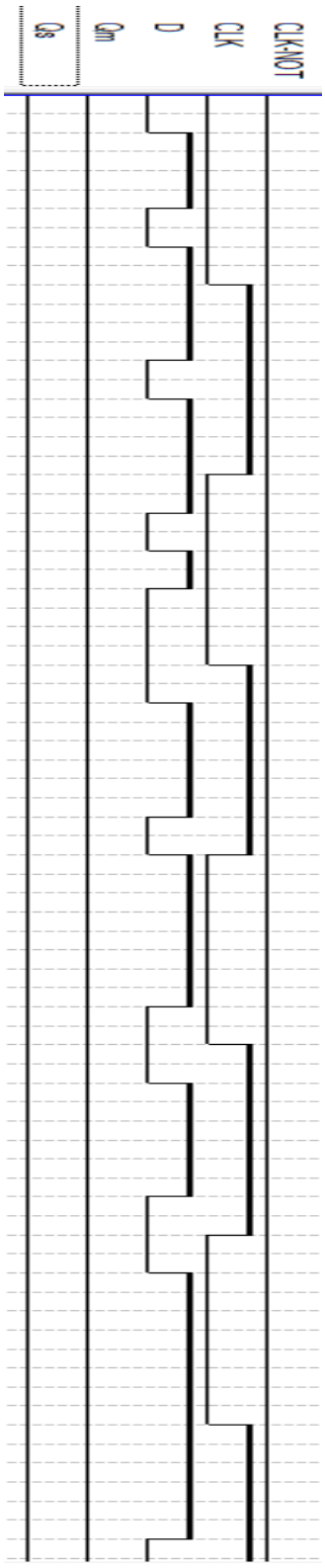
Instructions:

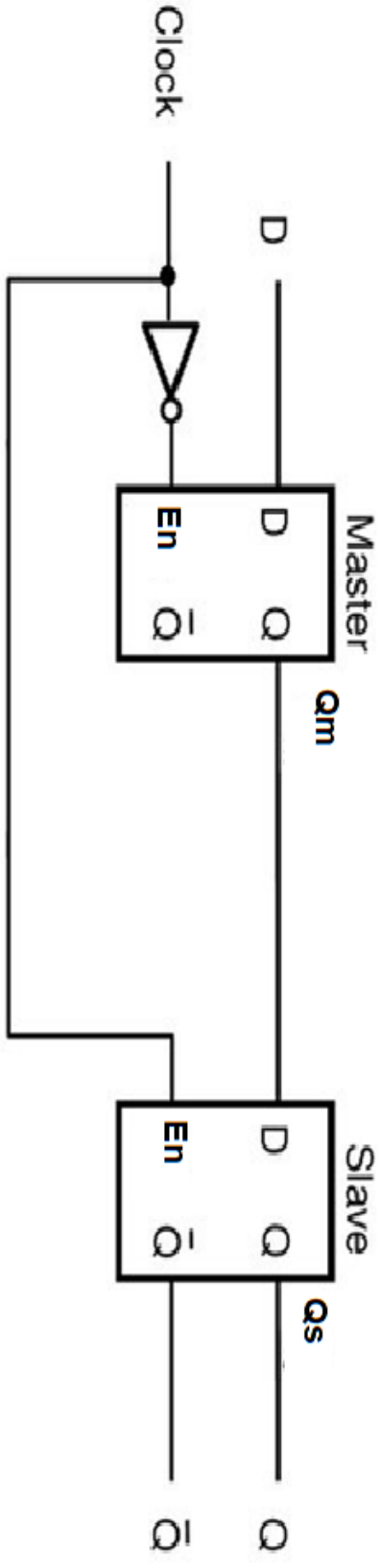
1. Read the question carefully, understand the question, and then attempt your answers either on the question paper or in the provided answer booklet as required.
2. Attempt all your questions and their parts in sequence on the answer sheet to receive **5 bonus** marks
3. Verify that you have **9** printed pages of the question paper including this page. There are **Nine (9)** questions.
4. Submit both your question paper and answer sheets. There is no need to staple the question paper with the answer sheets.
5. Sharing calculators or any other stationery is strictly prohibited.

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Bonus	Total
Marks Obtained											
Total Marks	**10**	**20**	**15**	**10**	**15**	**10**	**15**	**10**	**20**	**5**	**130**

Question. No. 1

Update the timing diagram for the outputs **CLK_NOT**, **Qm**, and **Qs** by considering the given **CLK** and **D** as inputs to the circuit shown below, where **En** is active high. Assume both latches store zero initially (Attempt it on question paper) **[10]**





Question. No. 2

Consider the circuit given below. Process circuit for given **INPUTS** and complete the below given table. (Attempt on question paper) **[20]**

1.
Process circuit for inputs,

where **C=0** and

Old States are.

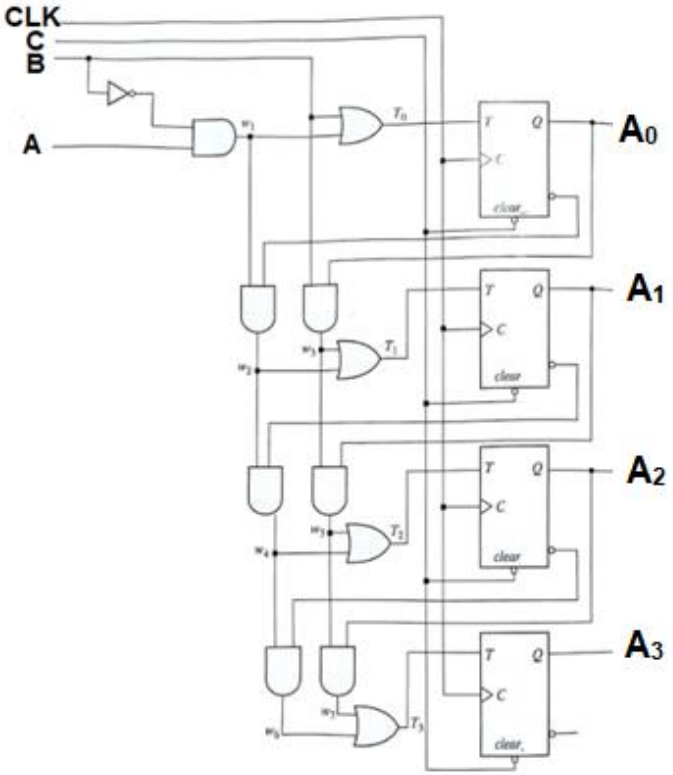
$A_0^t =$ **1,** $A_1^t =$ **0,** $A_2^t =$ **0,** $A_3^t = 1$

Calculate **Next States**

$A_0^{t+1} =$, $A_1^{t+1} =$,

$A_2^{t+1} =$, $A_3^{t+1} =$

[3]



2.
Process circuit for inputs.

where **C=1, B=1** and

Old States are

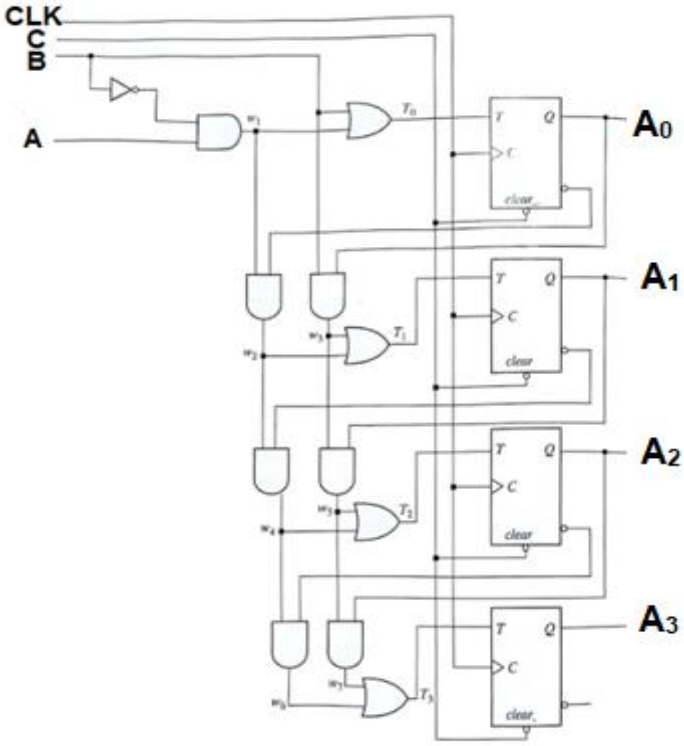
$A_0^t = 1, A_1^t = 0, A_2^t = 0, A_3^t = 1$

.
Calculate **Next States** after clock pulse.

$A_0^{t+1} =$, $A_1^{t+1} =$

$A_2^{t+1} =$, $A_3^{t+1} =$

[3]



3.

Process circuit for inputs,
where **C=1, B=0, A= 1** and

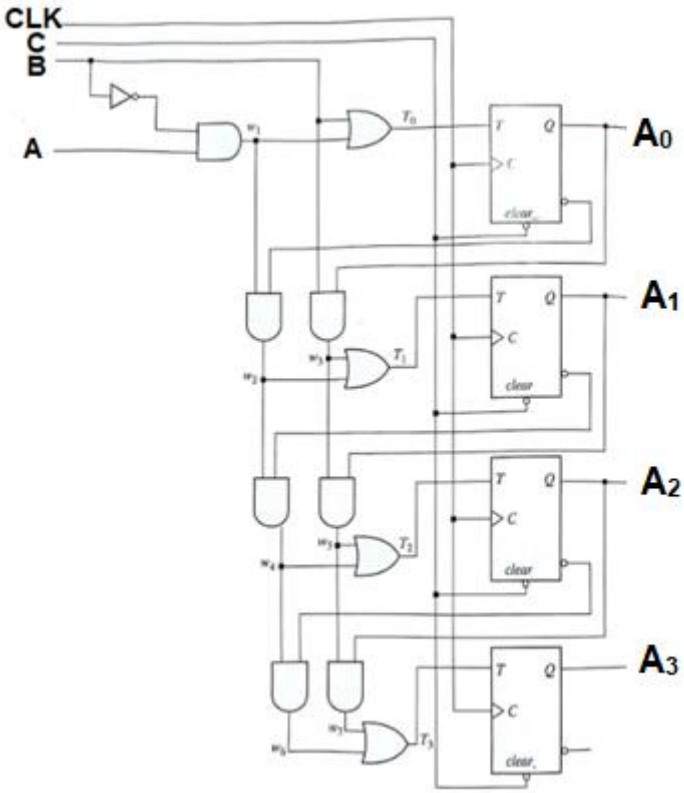
Old States are
$A_0^t = 0, A_1^t = 0, A_2^t = 1, A_3^t = 0$.

Calculate **Next States** after clock pulse.

$A_0^{t+1} =$, $A_1^{t+1} =$,

$A_2^{t+1} =$, $A_3^{t+1} =$

[3]



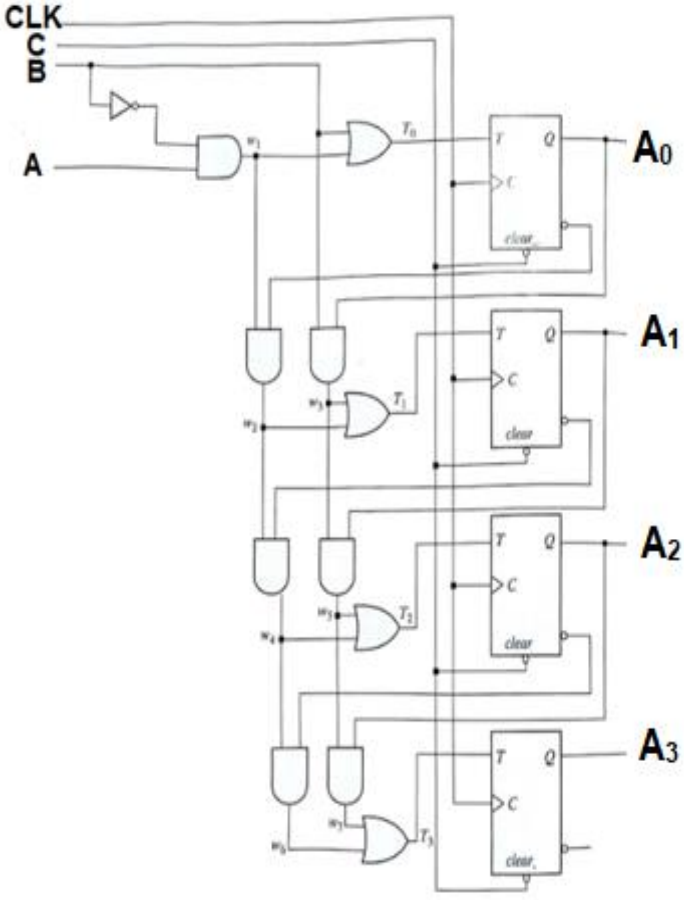
4.

Process circuit for inputs,
where **C=1, B=0, A= 0** and
Old States are $A_0^t = 0, A_1^t = 1, A_2^t = 1,$
$A_3^t = 0$ Calculate **Next States** after clock pulse

$A_0^{t+1} =$, $A_1^{t+1} =$,
$A_2^{t+1} =$, $A_3^{t+1} =$

[3]

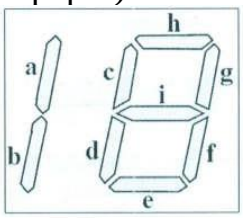
C	CLK	B	A	Function



Name above processed circuit _____ **[3]**

Question.No.3

You have worked with 7 segment displays in your class and labs. This question requires you to work with 9-Segment Displays. The structure of the 9-Segment Display is given below. (Attempt on question paper) [5+5+5=15]



The 9-Segment Display can be used to display decimal numbers from 0 to 15 as shown below:

Digit	9 Segment Equivalent	Segment **h**	Digit	9 Segment Equivalent	Segment **h**
0			8		
1			9		
2			10		
3			11		
4			12		
5			13		
6			14		
7			15		

The following parts of the question require you to design a “Binary to 9-Segment Display Decoder”. This “Binary to 9-Segment Display Decoder” takes four bits (W, X, Y, Z) at its input (MSB: W and LSB: Z) and generates nine outputs (a,b,c,d,e,f,g,h,i) to feed into the 9-segment display, and turn ON/OFF the required LED segments. An LED Segment is turned ON if its corresponding bit (a or b or c, etc) is 1. Similarly, an LED Segment is turned OFF if its corresponding bit (a or b or c, etc) is 0. Do as directed in the following parts:

a. Fill the Truth Table for output “h" only given above.

b. Derive a simplified expression for only output bit "h" of the Binary to 9-Segment Display Decoder using K-map (SOP form).

WX/YZ				

Expression:

c. Continuing with part-b, draw a circuit diagram for the simplified expression of "h" that you found. You are required to use a mix of Complex (X-OR, etc) and Primitive (AND, OR, etc) Digital Logic Gates.

Question.No.4

A bi-directional shift register is represented in the following Figure-(a). Initially the Register stores the decimal number eight (8). Complete the timing table (at the end of the question) with respect to the state of control line represented in the Figure (b). (Attempt it on question paper) [10]

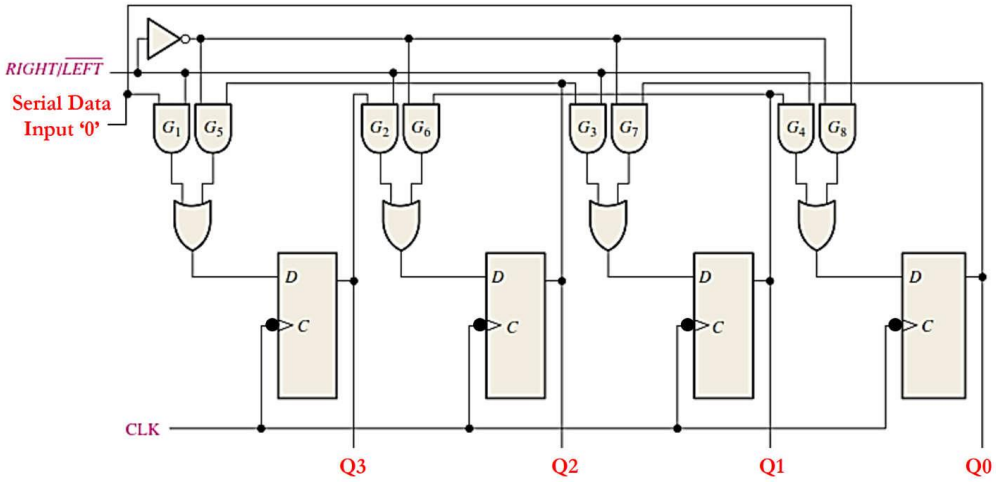


Figure (a)

Figure (b)

Clock	Q3	Q2	Q1	Q0	Shift Direction
Initial Condition					
↓					
↓					
↓					
↓					
↓					
↓					
↓					
↓					
↓					
↓					
↓					
↓					

Question.No.5

Design a priority encoder following this priority. Only expressions required and No Circuit. Diagram required (Attempt it on question paper) [15]

$$D_0 > D_3 > D_1 > D_2$$

D0	D1	D2	D3	X	Y	V(En)
1						
	1					
		1				
			1			

D0	D1	D2	D3	X	Y	V

K-Maps:

X =

$D_0D_1 \backslash D_2D_3$				

Y =

$D_0D_1 \backslash D_2D_3$				

V =

$D_0D_1 \backslash D_2D_3$				

Question.No.6

a. What is the difference between a latch and a flip-flop (one line answer)?
b. Implement a JK flip-flop with a T flip-flop and a minimal AND-OR-NOT network. Draw the logic diagram to show your design. [2+8=10]

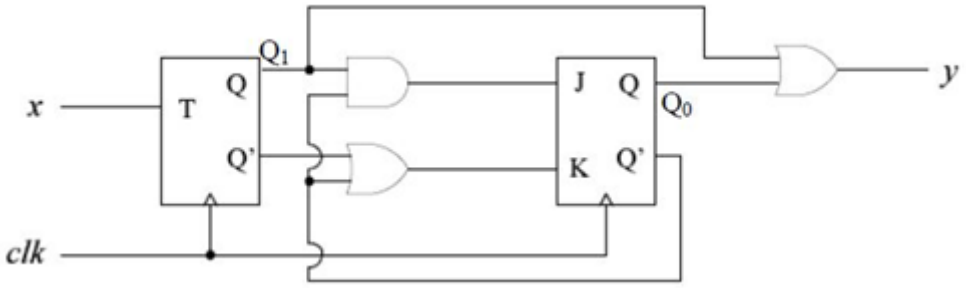
Question.No.7

Given a three-inputs boolean function f(a,b,c) = Σm(0, 1, 2, 3, 7). [5+5+5=15]

a. Implement the function using a minimal network of 2:4 decoders and OR gates.
b. Implement the function using a minimal network of 4:1 multiplexer.
c. Implement the function using a minimal network of 2:1 multiplexer.

Question.No.8

Write the state table of the below given sequential circuit. [10]



Question.No.9

Design a random counter given below? Find self-correcting state for unused state 2? And force correct state 4? You are supposed to use three different flip-flops where **D flipflop** is the least, **JK flipflop** to store middle bit, and **T-Flip Flop** to store most significant bit. Complete the excitation table for all the flip-flops.) **[20]**

Excitation Table					
Present State	**Next State**	**D**	**J**	**K**	**T**
0	0				
0	1				
1	0				
1	1