National University of Computer and Emerging Sciences

FAST School of Computing **Spring 2020** **Islamabad Campus**

EL-227: Digital Logic & Design Lab

Friday, 26th June, 2020

Remote Final Exam

Attempt Time: 3 Hours
Submission Time: (on Google Classroom and through email) **15 minutes**

Total Marks: 50

Lab Instructor(s)

Mr. Shams Farooq, Mr. Saad Salman,
Mr. Shoaib Mehboob, Ms. Humera Sabir,
Ms. Kainat Iqbal, Ms. Saba Kanwal,
Ms. Fatima Farooq, Ms. Parisa Salma

Instructions:

1. The final exam will be attempted offline in the student's own handwriting (in readable way).
2. The students will use A4 size blank white sheets to attempt the exam (portrait format unless a diagram or table requires landscape). Each sheet of the A4 size paper **MUST** have the Roll Number, Name, the course code, name of the course and Signature of the student at the top of **EACH** sheet.
3. Students will use cam-scanner, MS lens, or an equivalent application to scan and convert their hand-written answer sheets into a **SINGLE** pdf file (keeping the correct order of pages and question numbers), which they will submit on LMS and **MUST also** email to the email address (of the concerned course/lab instructor) which will be provided. They will be given 15 minutes (after the 3 hours attempt time) for this purpose. All students must use the standard file name format (Full course code - Roll number – Section e.g. EL227-i190123-B2). Submissions after 30 minutes may not be accepted. **Try to submit soon after 3 hours of attempt time and do not wait for 15 minutes to be elapsed.**
4. For proven **cheating/ plagiarism**, student will get an **F grade even if the student had opted for S/U grade**, and the case will be referred to DDC (Department's Disciplinary Committee). Instructors will conduct vivas of randomly selected students or in case of doubt (significantly different attempt as compared to past performance in the course or matching attempt with other students). Plagiarism includes sharing an attempt to other students (copy providing). Students who are not able to satisfactorily answer instructor's questions (based on the exam as well as slightly lateral but related concepts) during viva will also be considered as plagiarism cases.
5. Students should carry a clean scanning that is free from any marks/stains etc.

	Q-1	Q-2	Q-3	Total
Marks	**10**	**10**	**30**	**50**

IMPORTANT NOTE

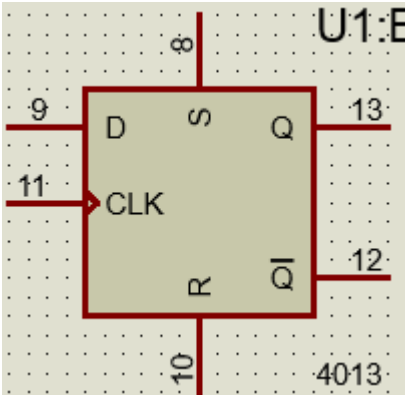
- ✓ No marks will be given for the late submission
- ✓ No marks will be given for the direct answers
- ✓ Corrupt files will not be considered for evaluations
- ✓ Save the projects before adding it to the zip file
- ✓ You are supposed to Label your proteus file intensively
- ✓ You have to submit folder(.RAR) with the followings
  - **Proteus Project files** for all questions and sub Questions in total (7-project files)
  - **Paper work** done for all the questions as .pdf
  - **Snap shots** of all proteus files. (7 snap shot)
- ✓ Naming convention for every file
  - Every file submitted should follow convention
    - CourseCode-RollNo-Section (e.g **EL227-i190123-B2**).
- ✓ Kindly consider 4-digit number assign to you in an attached excel sheet.

  FOR EXAMPLE: number assigned to you is (9821)

  - Where **D1** is **Last** digit of assigned number e.g. **(1)**
  - Where **D2** is **Third** digit of assigned number e.g. **(2)**
  - Where **D3** is **Second** digit of assigned number e.g. **(8)**
  - Where **D4** is **First** digit of assigned number e.g. **(9)**

Question 1 [5+5=10Marks]

I. Design a 4-bit Ripple up counter (Asynchronous counter) using Flip-Flop given below? Implement designed circuit in proteus?



II. Convert the above designed 4-bit Ripple counter to MOD(D4) Counter? Where D4 digit is assigned to you in excel sheet? For example: if ID assigned to you is 9821 than D4=9

Question 2 [4+6=10Marks]

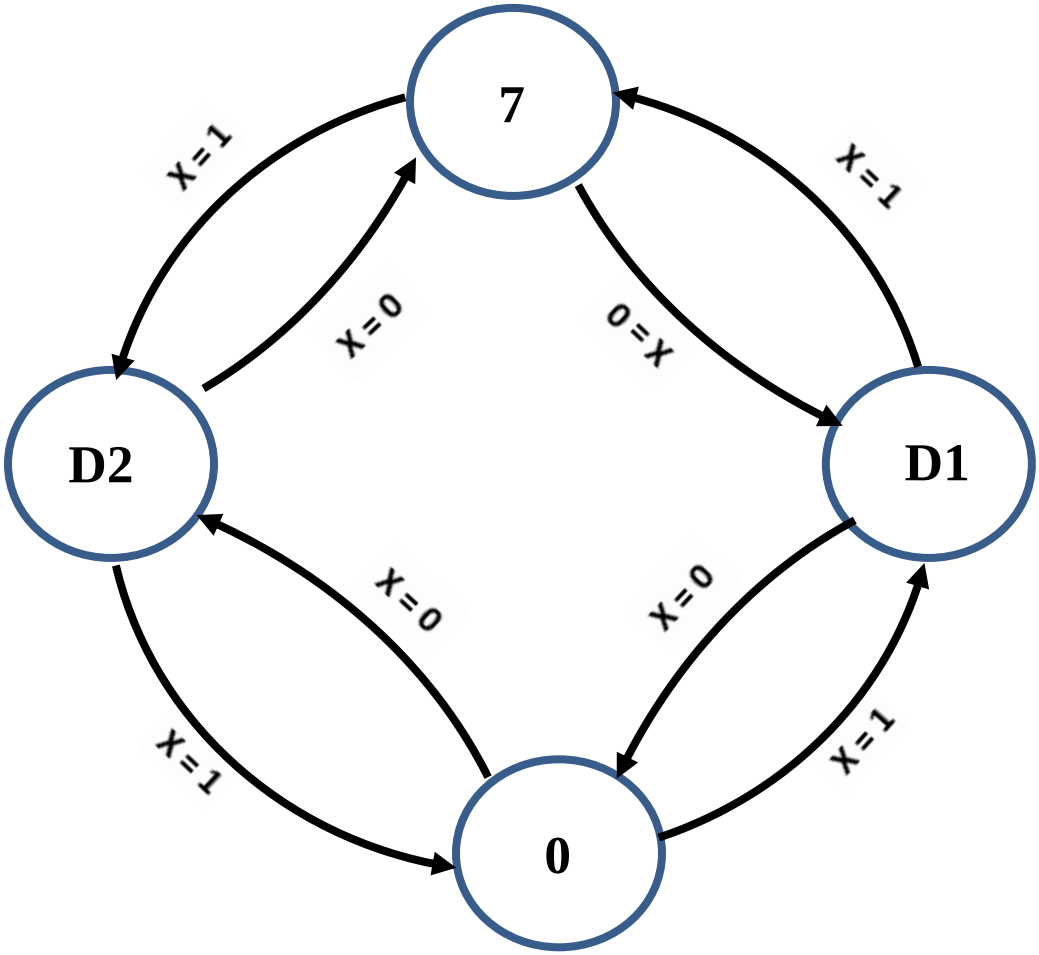
I. Implement following function using 16 x 1 multiplexer?

$$F(A,B,C,D) = \prod_{A,B,C,D}(D1, D2, D3, D4,10,11,13,15)$$

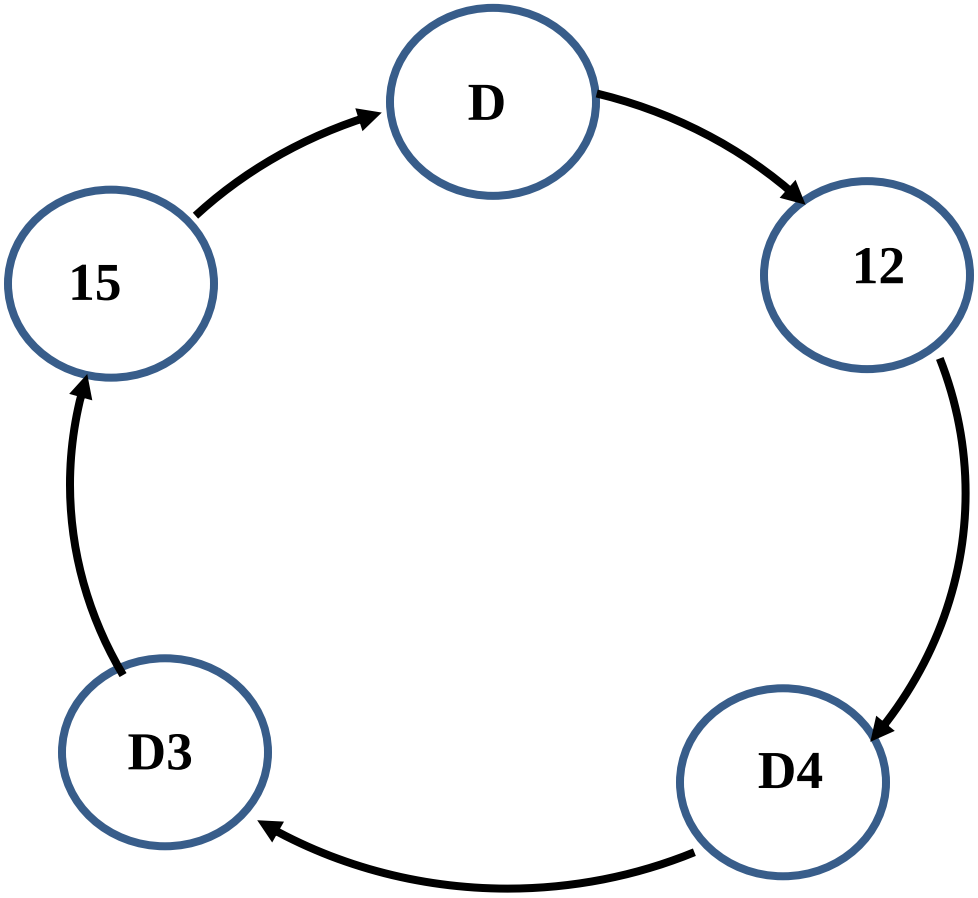
II. Implement function F given above using 8 x 1 multiplexer?

Question 3 [10+10+10= 30Marks]

I. Design circuit for following state diagram using JK flip Flop? Display each state in BINARY & DECIMAL



II. Design circuit for given state diagram using D Flip-Flop? Display each state in BINARY & DECIMAL



III. ADD binary numbers generated by both state machine and display the result in DECIMAL using 7-segment display