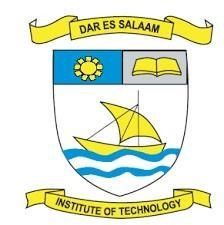
**DAR ES SALAAM INSTITUTE OF TECHNOLOGY**

****

**DEPARTMENT OF COMPUTER STUDIES**

**BACHELOR OF COMPUTER ENGINEERING**

**BENG-20 COE**

**GROUP 9 MEMBERS:**

|  |  |  |
| --- | --- | --- |
| **S/N** | **NAME** | **REGISTRATION NUMBER** |
| 1 | WINFRIDA WALTER MUZZE | 200240213013 |
| 2 | ELIAS MKONGO SEIF | 190230220783 |
| 3 | THOBIAS KASITA RICHARD | 200240224283 |
| 4 | INNOCENT SYLIVESTER | 200240224416 |
| 5 | ARFAJA ARFAJA MOHEMED | 190230221888 |

ASSIGMENT 04: ETU 07422 DIGITAL ELECTRONICS

# Question 1

1. Compare the performance of binary serial and parallel adders.

|  |  |  |
| --- | --- | --- |
| **Function** | **Serial Adder** | **Parallel Adder** |
| **Process of addition** | Only one bit at a time, as one after another | All bits are added simultaneously |
| **Speed of operation** | slow | Fast |
| **Number of full adders required** | Only one | One for each bit addition |
| **cost** | cheap | expensive |

1. Design of three-bit parity generator.[ Hint Include the odd parity generator and even parity generator ]

The parity generating technique is one of the most widely used error detection techniques for the data transmission.

A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter.

even parity bit scheme, the parity bit is ‘0’ if there are even number of 1s in the data stream and the parity bit is ‘1’ if there are odd number of 1s in the data stream.

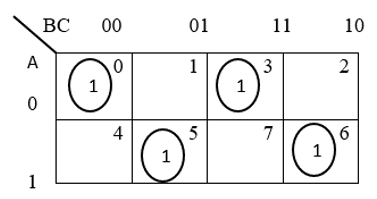
In odd parity bit scheme, the parity bit is ‘1’ if there are even number of 1s in the data stream and the parity bit is ‘0’ if there are odd number of 1s in the data stream. Let us discuss both even and odd parity generators.

**Even Parity Generator**

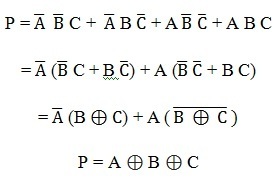
For the 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

|  |  |  |  |
| --- | --- | --- | --- |
| **3-bits message** | | | **Even parity bit generator** |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

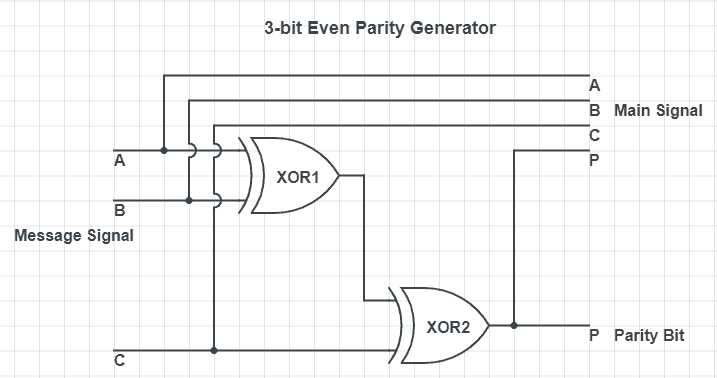
The K-map simplification for 3-bit message even parity generator is



From the above truth table, the simplified expression of the parity bit can be written as



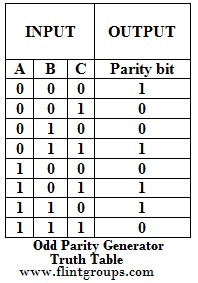
The above expression can be implemented by using two Ex-OR gates. The logic diagram of even parity generator with two Ex – OR gates is shown below. The three bit message along with the parity generated by this circuit which is transmitted to the receiving end where parity checker circuit checks whether any error is present or not.



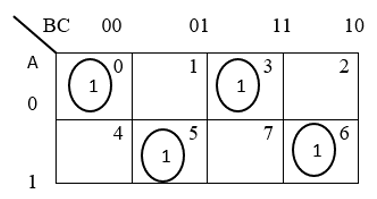
**Odd Parity Generator**

Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.



The truth table of the odd parity generator can be simplified by using K-map as

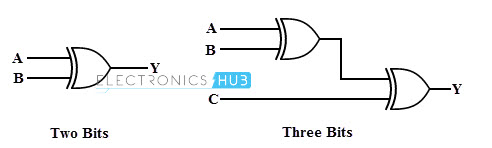


The output parity bit expression for this generator circuit is obtained as

P = A ⊕ (B ⊕ C)

The above Boolean expression can be implemented by using one Ex-OR gate and one Ex-NOR gate in order to design a 3-bit odd parity generator.

The logic circuit of this generator is shown in below figure, in which two inputs are applied at one Ex-OR gate, and this Ex-OR output and third input is applied to the Ex-NOR gate, to produce the odd parity bit. It is also possible to design this circuit by using two Ex-OR gates and one NOT gate.



1. State the effect of minimizing a fundamental sum of products expression

Minimization is important since it reduces the cost and complexity of the associated circuit.

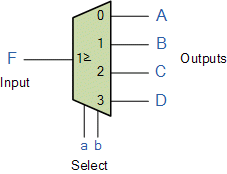
The process of simplifying the algebraic expression of a boolean function is called minimization. Minimized version of the expression takes a smaller number of logic gates and also reduces the complexity of the circuit substantiall. So, sum of product when minimized it an cause the occurrence of little number of gates and that will tends to reduce the circuit normal functionally as its deduces from the on bits.

# Question 2

1. Describe the main function of a demultiplexer in digital circuits .

The demultiplexer is a combinational logic circuit designed to switch one common input line to one of several seperate output line

he function of the Demultiplexer is to switch one common data input line to any one of the 4 output data lines A to D



1. Briefly explain, why a multiplexer can be used as a 'universal logic block'? S

Multiplexers in Digital Logic. It is a combinational circuit which have many data inputs and single output depending on control or select inputs. For N input lines, log n (base2) selection lines, or we can say that for 2 n input lines, n selection lines are required.

# Question 3

1. Describe the term half adder as used in digital electronics

The half adder is a combinational circuit used to perform the addition of two binary inputs and produces the two binary outputs as sum (S) and the carry(C) bits.

1. Design a single bit comparator [Hint: Use circuit diagram to present your design]

A 1-bit comparator compares two single bits.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | A>B | A<B | A=B |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 |

Let’s apply a shortcut to find the equations for each of the cases. Normally, we can

use a K-map. But this shortcut is efficient and handy when you understand it.

For A>B, there is only one case when the output is high when A=1 *and* B=0. Let’s call this X. We can write the equation as follows

X(which stands for A>B) = AB’

Similarly, denote A<B with Y and A=B with Z.

Since Y is high when A=0 and B=1, we get the following equation

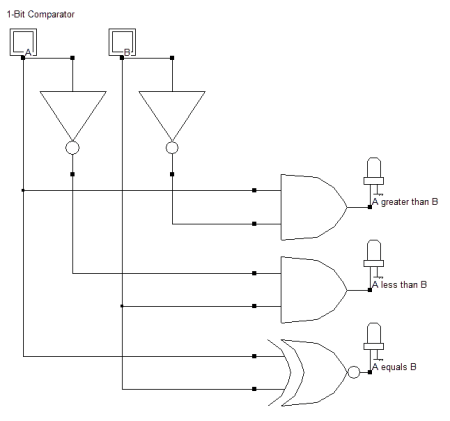
Y = A’B

Since Z is high in two cases, there will be an [OR gate](https://technobyte.org/2018/09/logic-gates-simplified-deriving-all-gates-using-nand-and-nor-gates#What_is_an_OR_gate). This is because the logic behind an OR gate is that a high output can be achieved in one or more cases. Z is high when A=0 and B=0, it is also high when A=1 and B=1. Therefore,

Z = A’B’ + AB

This is similar to the equation of an [EXNOR gate](https://technobyte.org/2018/09/logic-gates-simplified-deriving-all-gates-using-nand-and-nor-gates#What_is_an_EXNOR_gate_XNOR). Hence,

Z = A\oplusB

[](https://i2.wp.com/technobyte.org/wp-content/uploads/2018/09/1-bit-comparator.png?ssl=1)

The logic circuit of a 1-bit comparator

# Question 4

1. State the main difference between non-critical and critical races

**A critical race** condition occurs when the order in which internal variables are changed determines the eventual state that the state machine will end up in.

WHILE

**A non-critical race** condition occurs when the order in which internal variables are changed does not determine the eventual state that the state machine will end up in.

1. What is meant by 'breaking the feedback path' in the analysis of an asynchronous sequential circuit?

feedback is defined as the process of returning part of the signal output from a circuit or device back to the input of that circuit or device. Feedback systems are widely used in amplifier circuits, oscillators, process control systems, and in many other areas.