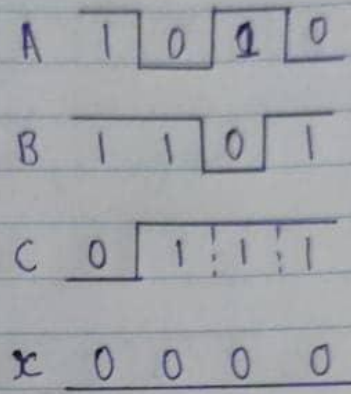


3  
NOR

Inputs  
10, 13, 7  
↓ ↓ ↓  
1010, 1101, 0111  
↓ ↓ ↓  
A B C

x = output  
Timing Diagram:

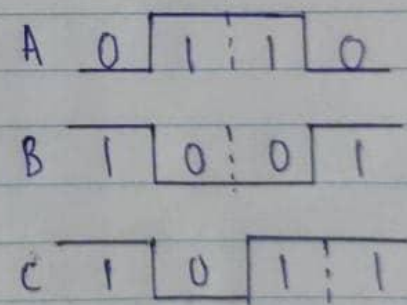


A	B	C	x
1	1	0	0
0	1	1	0
1	0	1	0
0	1	1	0

4  
NAND

Inputs  
6, 9, 11  
↓ ↓ ↓  
0110, 1001, 1011  
↓ ↓ ↓  
A B C

x = output  
Timing Diagram:



A	B	C	x
0	1	1	1
1	0	0	1
1	0	1	1
0	1	1	1

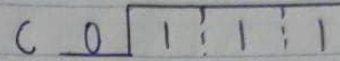
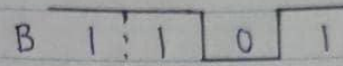
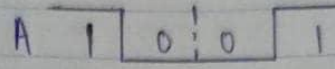
5

a)

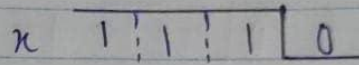
A	B	C	x
1	1	0	1
0	1	1	1
0	0	1	1
1	1	1	0

x = output

Timing diagram



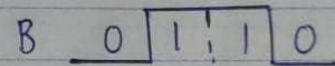
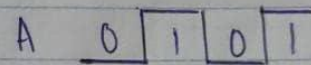
Output = NAND operation



b)

A	B	x
0	0	0
1	1	0
0	1	1
1	0	1

Timing diagram



Output = XNOR operation x 0 0 1 1