

Digitaltechnik Labor 1

Die digitale Zweifaltigkeit

Versuchsbericht

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Inhaltsverzeichnis

1 Einleitung	2
2 Hardwareentwurf	2
3 Aufbau	3
4 Analyse des Hardwareaufbaus	3
5 Schlussfolgerungen	4
6 Verbesserungsvorschläge	4
A Anhang: Bilder der Schaltungen	5
B Anhang: Datenblatt des BCD-Codewandlers	8

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1 Einleitung

In diesem Bericht wird der Umgang mit Hardwarekomponenten der Elektrotechnik erlernt, außerdem werden erste Schaltungen entwickelt. Zuerst wird eine Leuchtdiode mit Taster betrieben, anschließend werden verschiedene integrierte Schaltkreise (IC) hinzugefügt. Schließlich wird eine 7-Segment-Anzeige über eine BCD-Codierung angesteuert. Verwendete Abbildungen und Tabellen in dieser Ausarbeitung sind – soweit nicht anders angegeben – von dem Autor erstellt worden.

2 Hardwareentwurf

Die Hardwareschaltungen wurde bereits durch die Aufgabenstellung festgelegt. An dieser Stelle ist also keine Entwurfsplanung nötig. Das Breadboardlayout ist dem Abschnitt 3 zu entnehmen. An manchen Stellen wurde leicht vom Layout aus der Laboranleitung abgewichen.

Alle drei Schaltungen werden mit einer Versorgungsspannung V_{cc} von 3,3 V betrieben.

LED-Schaltung In der ersten Schaltung wird ein Taster als Schließer verwendet. In Reihe dazu befindet sich eine rote LED wird mit einem Vorwiderstand von $220\ \Omega$. Die LED wurde in Durchlassrichtung geschalten.

NAND-Schaltung Bei der NAND-Schaltung wurde der SN74HC00N verwendet. An zwei Eingängen wird je ein Taster mit einem hochohmigen Widerstand von $10\ k\Omega$ als Pull-down geschalten. Die Verwendung der LED ist analog zur vorherigen Schaltung.

NOR-Schaltung Der Schaltungsaufbau ist hier identisch zur NAND-Schaltung, lediglich der IC wird durch den SN74HC02N ausgetauscht.

BCD-Codewandler Erläuterungen zu den Eingängen LT, BI und LE sind dem Dokument „Vorbereitung zum Versuch: Die digitale Zweifaltigkeit. Versuch 1“ von Jan Hoegen zu entnehmen.

Die Kathoden der Anzeige werden an einen einzelnen $1\ k\Omega$ Widerstand angeschlossen. Dies hat zur Folge, dass die Leuchtstärke der Anzeige bei verschiedenen Eingangszuständen nicht konstant ist. Am DIP-Schalter als Eingang werden erneut Pull-Down-Widerstände von $10\ k\Omega$ verwendet.

Statt des M74C4511 wurde der CD74HC4511E verwendet. Die Funktion sowie die Belegung der Pins ist unverändert, das zugehörige Datenblatt befindet sich im Anhang B.¹

¹Herausgeber: Texas Instruments. Abgerufen am 08.04.2022 von https://www.ti.com/lit/ds/symlink/cd74hc4511.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&ts=1649347240369&ref_url=https%253A%252Fwww.mouser.com%252F

3 Aufbau

Zur Besseren Übersicht befinden sich die Fotoaufnahmen des Breadboardlayout im Anhang A dieses Dokuments.

Abbildung 1 zeigt den Aufbau der LED-Schaltung. Die NAND-Schaltung ist der Abbildung 2 zu entnehmen. Als nächstes wird der Aufbau der NOR-Schaltung in Abbildung 3 gezeigt. Zuletzt wird der BCD-Codewandler betrachtet. Der zugehörige Schaltungsaufbau wird in 4 gezeigt.

4 Analyse des Hardwareaufbaus

LED-Schaltung Wenn der Taster geschlossen ist, leuchtet die LED auf. Dies entspricht den Erwartungen eines Schließers, da erst dann der Stromkreis geschlossen ist.

NAND-Schaltung Tabelle 1 zeigt den beobachteten Zusammenhang zwischen Taster und der LED der Schaltung. Erst dann, wenn beide Taster gleichzeitig betätigt werden, geht die LED aus. Dies entspricht den Erwartungen an ein NAND-Gatter.

Tabelle 1: Wahrheitstabelle der NAND-Schaltung

T1	T2	LED
0	0	1
0	1	1
1	0	1
1	1	0

NOR-Schaltung Tabelle 2 zeigt den beobachteten Zusammenhang zwischen Taster und der LED der Schaltung. Die LED geht aus, sobald mindestens einer der beiden Taster betätigt werden. Dies entspricht den Erwartungen an ein NOR-Gatter.

Tabelle 2: Wahrheitstabelle der NOR-Schaltung

T1	T2	LED
0	0	1
1	0	0
0	1	0
1	1	0

BCD-Decoder In der Tabelle 3 wird zu jeder Schalterstellung des DIP die angezeigte Ziffer notiert. Es fallen zwei Dinge auf: Zum einen entspricht die angezeigte Ziffer der Codierung im

Tabelle 3: Wahrheitstabelle des BCD-Codewandlers

1	2	3	4	Ziffer
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Datenblatt. Zum anderen sind alle Segmente aus, wenn ein Wert höher als 1001 eingestellt wird. Beides entspricht den Vorgaben im Datenblatt.

5 Schlussfolgerungen

Es lässt sich folgern, dass Taster und IC so arbeiten, wie die Laboranleitung verlangt, und ein korrektes Schaltungsdesign verwendet wurde.

Der Taster arbeitet als Schließer und lässt einen Stromfluss zu, solange er gedrückt ist. Auch das NAND und das NOR arbeiten wie erwartet. Der BCD-Codewandler übersetzt einen Zustand am DIP-Schalter und die 7-Segment-Anzeige zeigt die dazugehörige Ziffer an. Für Eingangszustände größer als 1001 ist der Output als *Blank* definiert. Daher bleibt in diesen Fällen das Display schwarz.

Mir persönlich fiel es leicht, die Schaltungen aufzubauen und in Betrieb zu nehmen. Etwaige Fehler konnte ich schnell beheben. Auch die Tatsache, dass ich die Versuche nachgearbeitet habe, hat mich nur wenig beeinträchtigt.

6 Verbesserungsvorschläge

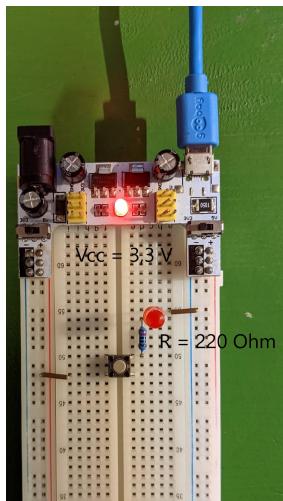
In diesem Versuchsbericht habe ich keine Schaltbilder oder andere Diagramme aus der Laboranleitung übernommen und hier erneut gezeigt. Ich bin mir nicht sicher, ob diese Vermeidung von Redundanz zu einem Nachteil für mich wird. Hätte der Bericht so formuliert werden sollen,

dass auch ein außenstehender Leser die Ergebnisse nicht nur nachvollziehen, sondern auch nachbilden kann?

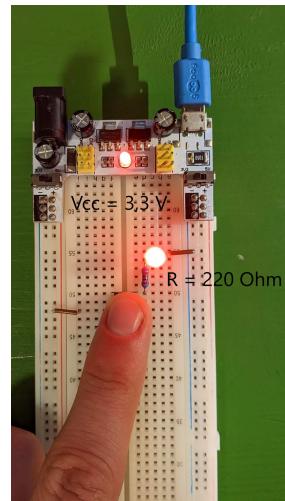
Mir ist nicht klar, wie groß der Umfang des Kapitel „Schlussfolgerungen“ sein soll. Jede Schaltung hat ihre Funktion erfüllt und es waren keine Abweichungen zu erkennen. Bis auf die Wahrheitstabellen mussten keine Messparameter beschrieben oder interpretiert werden.

A Anhang: Bilder der Schaltungen

Abbildung 1 zeigt den Aufbau der LED-Schaltung. Die NAND-Schaltung ist der Abbildung 2 zu entnehmen. Als nächstes wird der Aufbau der NOR-Schaltung in Abbildung 3 gezeigt. Zuletzt wird der BCD-Codewandler betrachtet. Der zugehörige Schaltungsaufbau wird in 4 gezeigt.



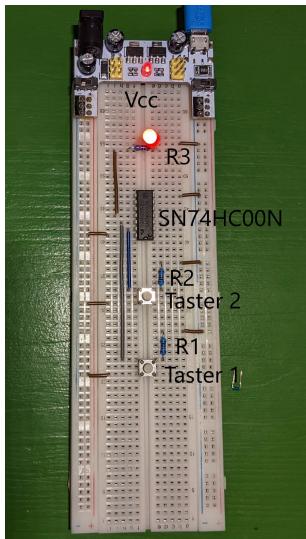
(a) Taster ist Offen



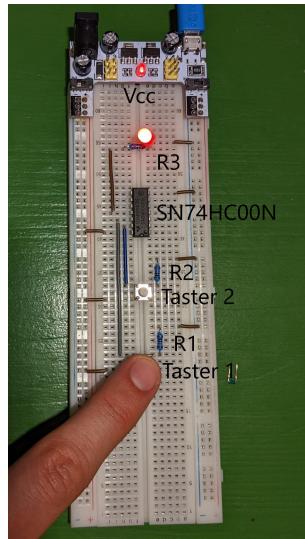
(b) Taster ist geschlossen

Abbildung 1: Realisierung der LED-Schaltung

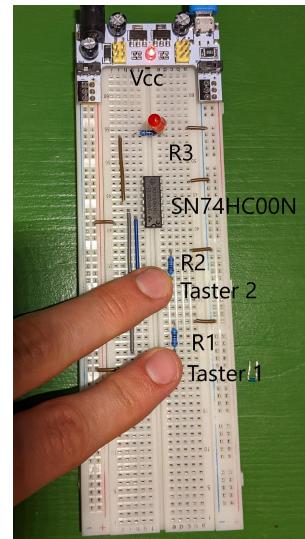
Legende: $R = 220 \Omega$, $V_{cc} = 3,3 \text{ V}$



(a) Taster 1 und 2 sind offen



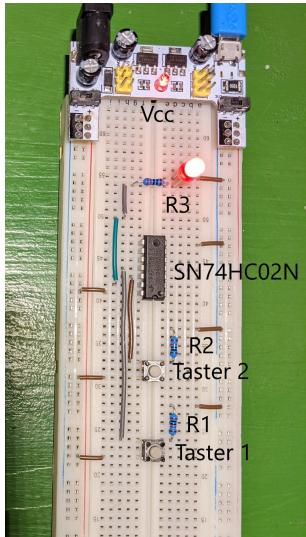
(b) Taster 1 ist geschlossen, Taster 2 ist offen



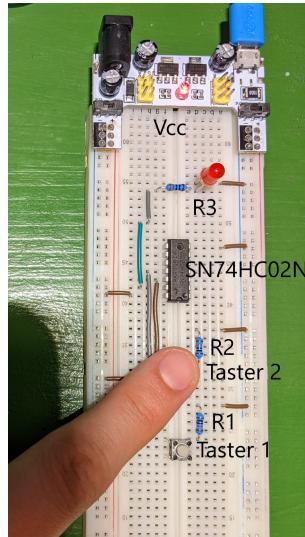
(c) Taster 1 und 2 sind geschlossen

Abbildung 2: Realisierung der NAND-Schaltung

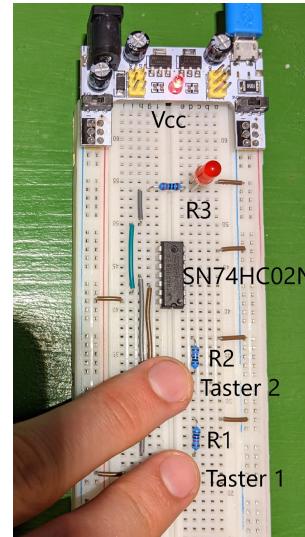
Legende: $R_1 = R_2 = 10 \text{ k}\Omega$, $R_3 = 220 \Omega$, $V_{cc} = 3,3 \text{ V}$



(a) Taster 1 und 2 sind offen



(b) Taster 1 ist offen, Taster 2 ist geschlossen



(c) Taster 1 und 2 sind geschlossen

Abbildung 3: Realisierung der NOR-Schaltung

Legende: $R_1 = R_2 = 10 \text{ k}\Omega$, $R_3 = 220 \Omega$, $V_{cc} = 3,3 \text{ V}$

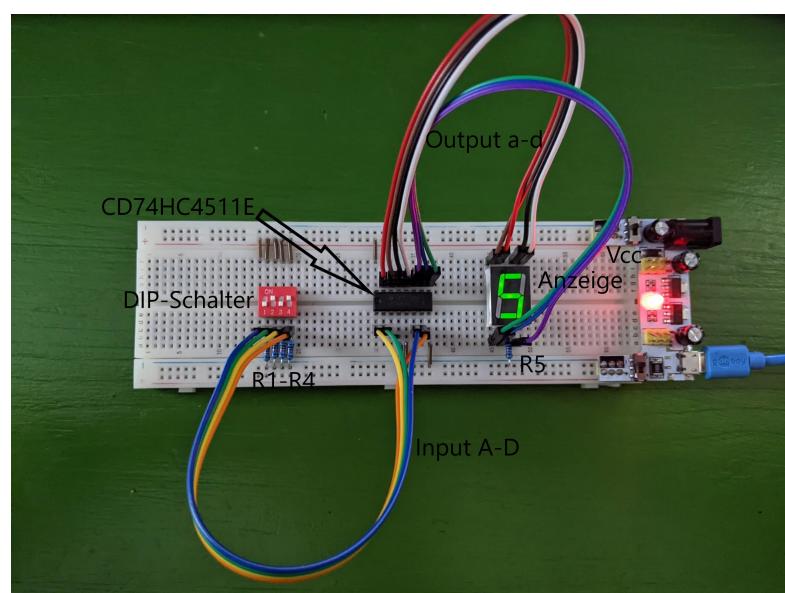


Abbildung 4: Realisierung des BCD-Decoder
Legende: $R_1 = R_2 = R_3 = R_4 = 10 \text{ k}\Omega$, $R_5 = 1 \text{ k}\Omega$, $V_{cc} = 3,3 \text{ V}$

CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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- 2-V to 6-V V_{CC} Operation ('HC4511)
- 4.5-V to 5.5-V V_{CC} Operation (CD74HCT4511)
- High-Output Sourcing Capability
 - 7.5 mA at 4.5 V (CD74HCT4511)
 - 10 mA at 6 V ('HC4511)
- Input Latches for BCD Code Storage
- Lamp Test and Blanking Capability
- Balanced Propagation Delays and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 'HC4511
 - High Noise Immunity, N_{IL} or N_{IH} = 30% of V_{CC} at $V_{CC} = 5$ V
- CD74HCT4511
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8$ V Maximum, $V_{IH} = 2$ V Minimum
 - CMOS Input Compatibility, $I_I \leq 1 \mu\text{A}$ at V_{OL}, V_{OH}

description/ordering information

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0 - D_3), an active-low blanking (BL) input, lamp-test (LT) input, and a latch-enable (LE) input that, when high, enables the latches to store the BCD inputs. When LE is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube of 25	CD74HC4511E	CD74HC4511E
			CD74HCT4511E	CD74HCT4511E
	SOIC – M	Tube of 40	CD74HC4511M	HC4511M
		Reel of 2500	CD74HC4511M96	
		Reel of 250	CD74HC4511MT	
	TSSOP – PW	Reel of 2000	CD74HC4511PWR	HJ4511
		Reel of 250	CD74HC4511PWT	
	CDIP – F	Tube of 25	CD54HC4511F3A	CD54HC4511F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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FUNCTION TABLE

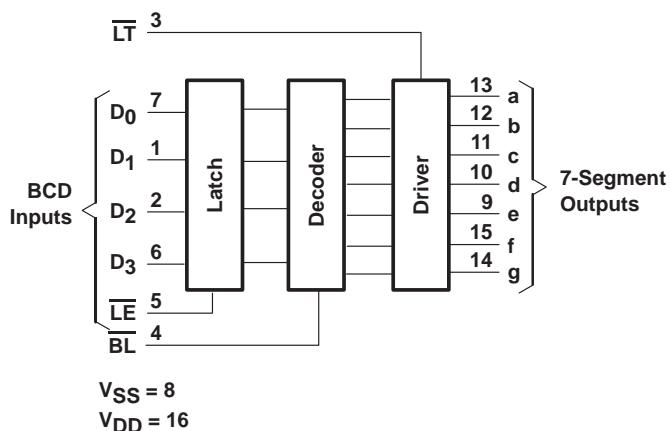
INPUTS			OUTPUTS							DISPLAY				
\overline{LE}	\overline{BL}	\overline{LT}	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	†	†	†	†	†	†	†	†

X = Don't care

† Depends on BCD code previously applied when $\overline{LE} = L$

NOTE: Display is blank for all illegal input codes (BCD > HLLH).

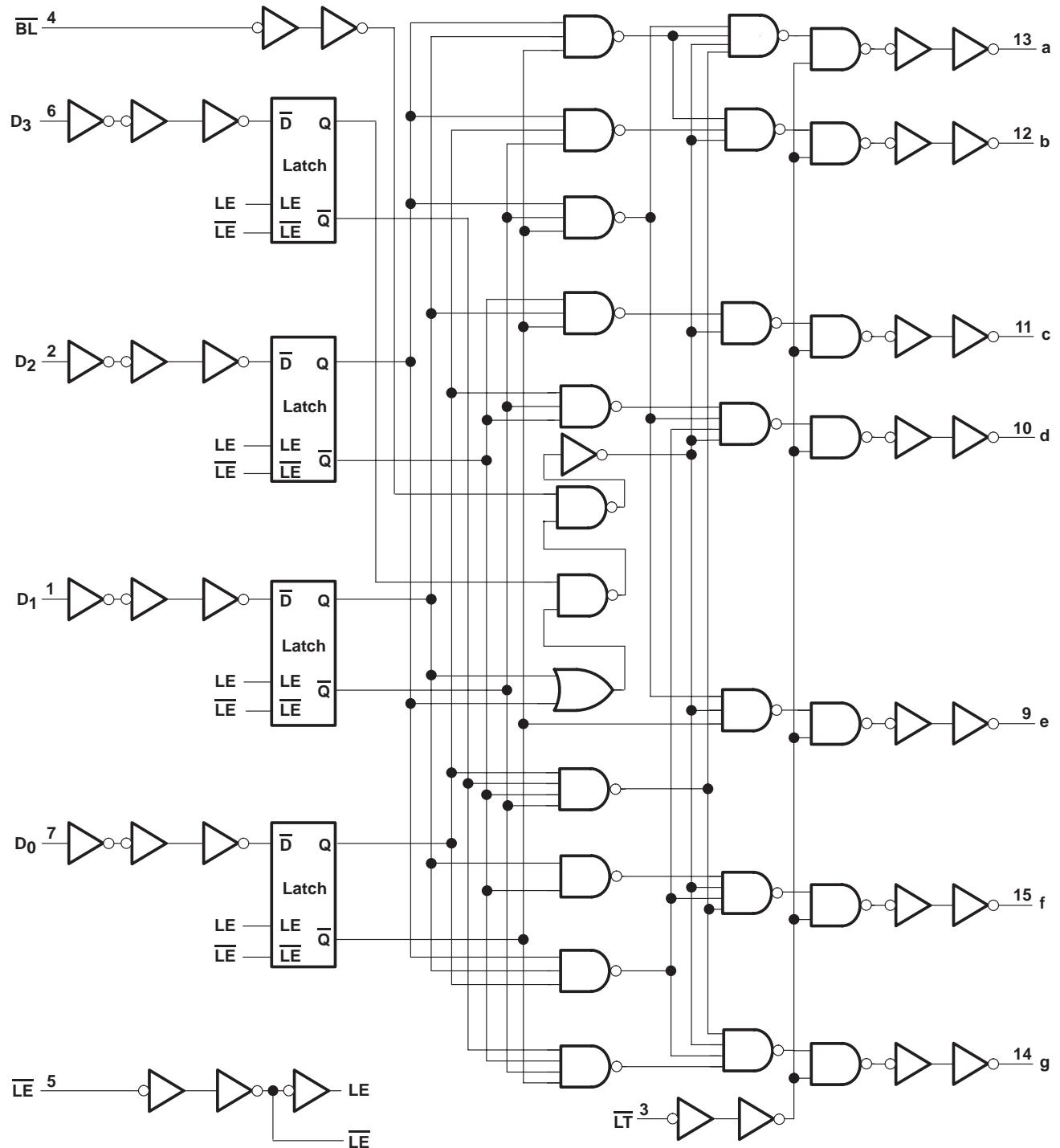
function diagram



CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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logic diagram



CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input diode current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1)	± 20 mA
Output diode current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1)	± 20 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
	M package	73°C/W
	PW package	108°C/W

Lead temperature (during soldering):

Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ in (1.59 ± 0.79 mm) from case for 10 s maximum	265°C
Unit inserted into a PC board (minimum thickness $1/16$ in, 1.59 mm), with solder contacting lead tips only	300°C
Storage temperature, T_{stg}	-65 to 150°C

sses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and continual operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not recommended. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for 'HC4511 (see Note 3)

		TA = 25°C		TA = -55°C TO 125°C		TA = -40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	6	2	6	2	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5	1.5	1.5	1.5	V
		V _{CC} = 4.5 V	3.15	3.15	3.15	3.15	3.15	
		V _{CC} = 6 V	4.2	4.2	4.2	4.2	4.2	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5	0.5	0.5	0.5	V
		V _{CC} = 4.5 V	1.35	1.35	1.35	1.35	1.35	
		V _{CC} = 6 V	1.8	1.8	1.8	1.8	1.8	
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	1000	1000	1000	1000	1000	ns
		V _{CC} = 4.5 V	500	500	500	500	500	
		V _{CC} = 6 V	400	400	400	400	400	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

recommended operating conditions for CD74HCT4511 (see Note 4)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V
t_t	Input transition (rise and fall) time		500		500		500	ns

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

'HC4511

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C	
			MIN	MAX	MIN	MAX	MIN	MAX
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.9		1.9	V
			4.5 V	4.4	4.4		4.4	
			6 V	5.9	5.9		5.9	
		$I_{OH} = -7.5 \text{ mA}$	4.5 V	3.98	3.7		3.84	V
		$I_{OH} = -10 \text{ mA}$	6 V	5.48	5.2		5.34	
			2 V	0.1	0.1		0.1	
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	4.5 V	0.1	0.1		0.1	V
			6 V	0.1	0.1		0.1	
			4.5 V	0.26	0.4		0.33	
		$I_{OL} = 4 \text{ mA}$	6 V	0.26	0.4		0.33	V
		$I_{OL} = 5.2 \text{ mA}$						
I_I	$V_I = V_{CC}$ or 0	6 V	± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V	8		160		80	μA
C_i				10		10	10	pF

CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

CD74HCT4511

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT	
						MIN	TYP	MAX	MIN		
			I _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 µA	4.4		4.4	4.4		
V _{OH}	V _I = V _{IH} or V _{IL}	4.5 V	I _{OH}	I _{OH} = -4 mA	3.98		3.7	3.84	V		
V _{OL}			I _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	0.1		0.1		0.1	
			I _{OL}		I _{OL} = 4 mA	0.26		0.4	0.33		
I _I	V _I = V _{CC} to GND	5.5 V				±0.1		±1	±1	µA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V				8		160	80	µA	
ΔI _{CC} [†]	One input at V _{CC} – 2.1 V, Other inputs at 0 or V _{CC}	4.5 V to 5.5 V				100	360		490	450	µA
C _i							10		10	10	pF

[†] Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS [‡]
LT, LE	1.5
BL, Dn	0.3

[‡] Unit load is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 µA maximum at 25°C.

'HC4511 timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
			2 V	80	120		100		ns
t _w	Pulse duration, LE low	4.5 V	16		24		20		
			6 V	14	20		17		
			2 V	60	90		75		ns
t _{su}	Setup time, BCD inputs before LE↑	4.5 V	12		18		15		
			6 V	10	15		13		
			2 V	3	3		3		ns
t _h	Hold time, BCD inputs before LE↑	4.5 V	3		3		3		
			6 V	3	3		3		



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CD54HC4511, CD74HC4511, CD74HCT4511
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

'HC4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	D _n	Output	C _L = 50 pF	2 V		300		450		375		ns
				4.5 V		60		90		75		
				6 V		51		77		64		
			C _L = 15 pF	5 V		25						
	LE	Output	C _L = 50 pF	2 V		270		405		340		
				4.5 V		54		81		68		
				6 V		46		69		58		
			C _L = 15 pF	5 V		23						
	BL	Output	C _L = 50 pF	2 V		220		330		275		
				4.5 V		44		66		55		
				6 V		37		56		47		
			C _L = 15 pF	5 V		18						
	LT	Output	C _L = 50 pF	2 V		160		240		200		ns
				4.5 V		32		48		40		
				6 V		27		41		34		
			C _L = 15 pF	5 V		13						
t _t		Any	C _L = 50 pF	2 V		75		110		95		ns
				4.5 V		15		22		19		
				6 V		13		19		16		



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

CD74HCT4511

timing requirements over recommended operating free-air temperature range $V_{CC} = 4.5$ V (unless otherwise noted) (see Figure 2)

				$T_A = 25^\circ C$		$T_A = -55^\circ C$ TO $125^\circ C$		$T_A = -40^\circ C$ TO $85^\circ C$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, \overline{LE} low			16		24		20		ns
t_{su}	Setup time, BCD inputs before $\overline{LE} \uparrow$			16		24		20		ns
t_h	Hold time, BCD inputs before $\overline{LE} \uparrow$			5		5		5		ns

CD74HCT4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25^\circ C$			$T_A = -55^\circ C$ TO $125^\circ C$		$T_A = -40^\circ C$ TO $85^\circ C$		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D_n	Output	$C_L = 50$ pF	4.5 V		60		90		75		ns
			$C_L = 15$ pF	5 V		25						
	\overline{LE}	Output	$C_L = 50$ pF	4.5 V			54		81		68	
			$C_L = 15$ pF	5 V		23						
	\overline{BL}	Output	$C_L = 50$ pF	4.5 V			44		66		55	
			$C_L = 15$ pF	5 V		18						
	\overline{LT}	Output	$C_L = 50$ pF	4.5 V		33		50		41		
			$C_L = 15$ pF	5 V		13						
t_t		Any	$C_L = 50$ pF	4.5 V			15		22		19	ns

operating characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ C$

PARAMETER			TYP	UNIT
C_{pd}^{\dagger}	Power dissipation capacitance	'HC4511	114	
		CD74HCT4511	110	pF

[†] C_{pd} is used to determine the dynamic power consumption, per package.

$$P_D = C_{pd} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$$

where: f_i = input frequency

f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

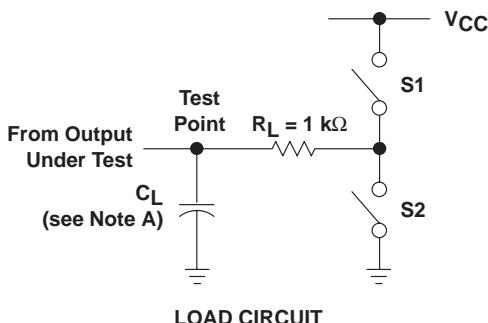


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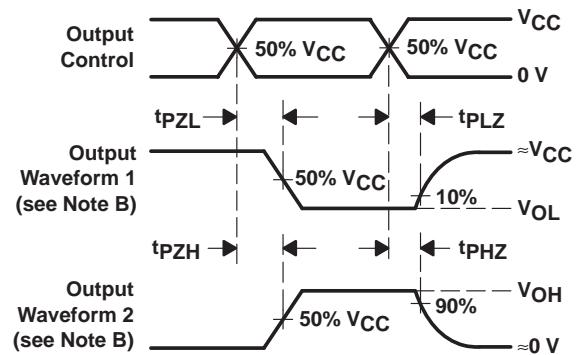
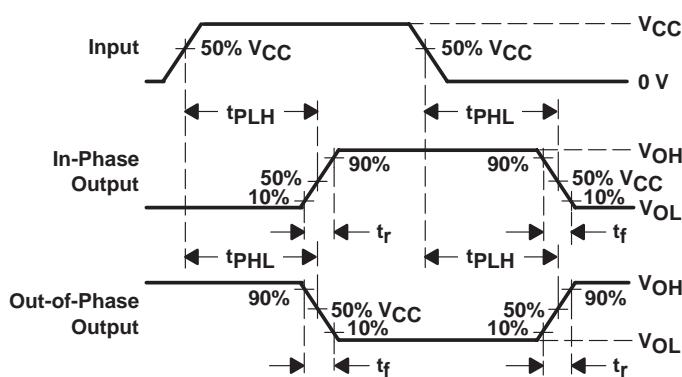
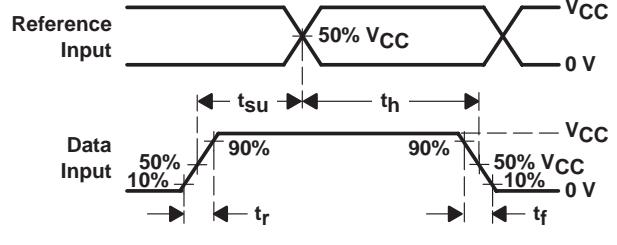
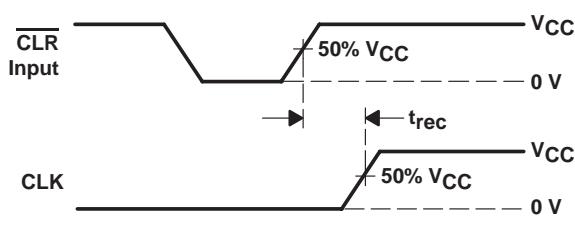
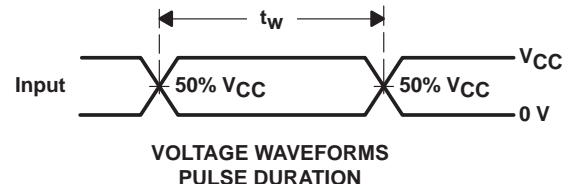
CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

PARAMETER MEASUREMENT INFORMATION – 'HC4511



PARAMETER	S1	S2
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd} or t_t	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

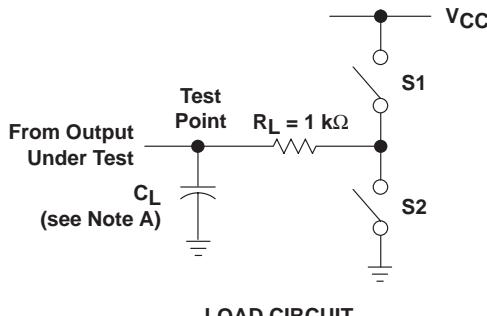


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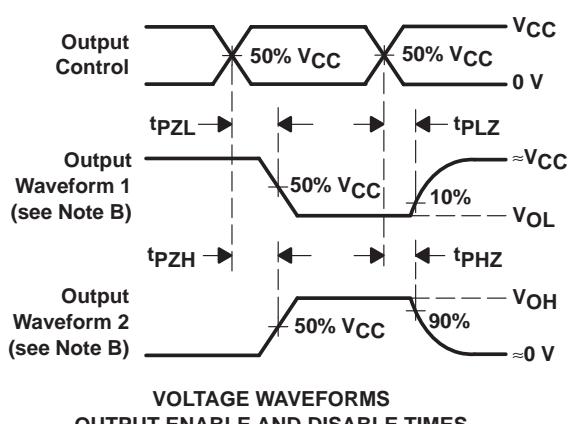
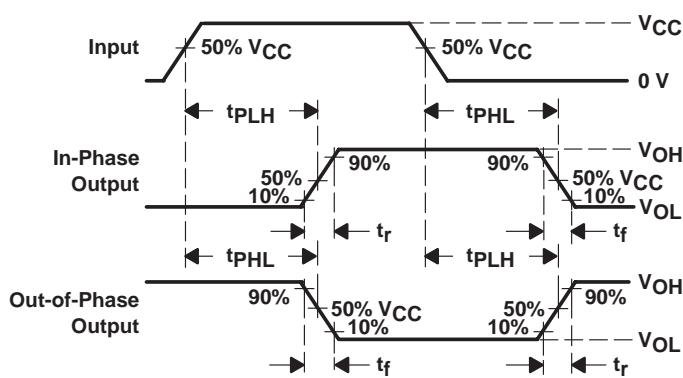
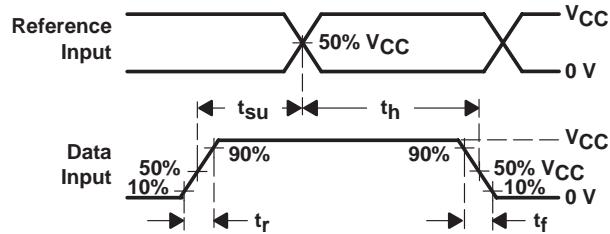
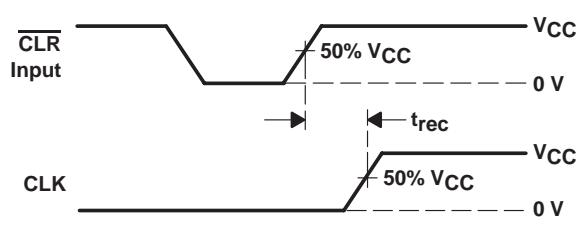
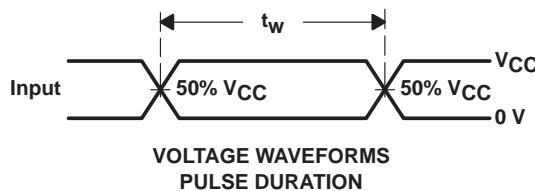
CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

SCHS279D – DECEMBER 1998 – REVISED OCTOBER 2003

PARAMETER MEASUREMENT INFORMATION – CD74HCT4511



PARAMETER	S1	S2
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd} or t_t	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

**TEXAS
INSTRUMENTS**

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8773301EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A	Samples
CD54HC4511F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A	Samples
CD74HC4511E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4511E	Samples
CD74HC4511EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4511E	Samples
CD74HC4511M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	Samples
CD74HC4511M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	Samples
CD74HC4511M96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	Samples
CD74HC4511MG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	Samples
CD74HC4511MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	Samples
CD74HC4511PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	Samples
CD74HC4511PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	Samples
CD74HC4511PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	Samples
CD74HC4511PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	Samples
CD74HC4511PWTE4	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	Samples
CD74HCT4511E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4511E	Samples
CD74HCT4511EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4511E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBSOLETE:** TI has discontinued the production of the device.

(²) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(³) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(⁴) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(⁵) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(⁶) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC4511, CD74HC4511 :

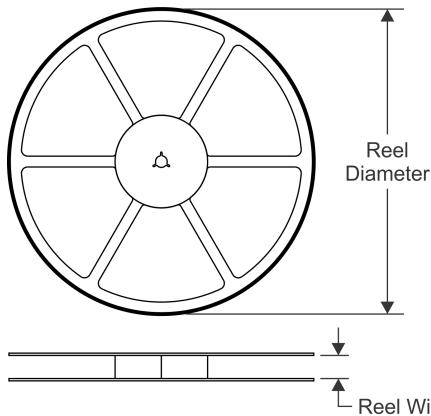
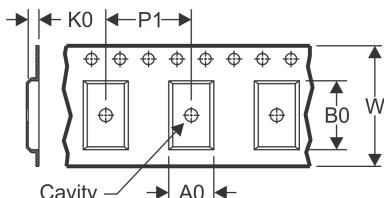
• Catalog : [CD74HC4511](#)

• Military : [CD54HC4511](#)

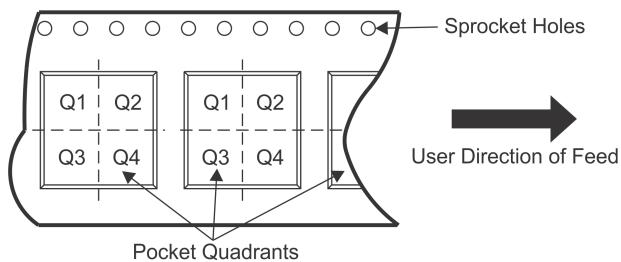
NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

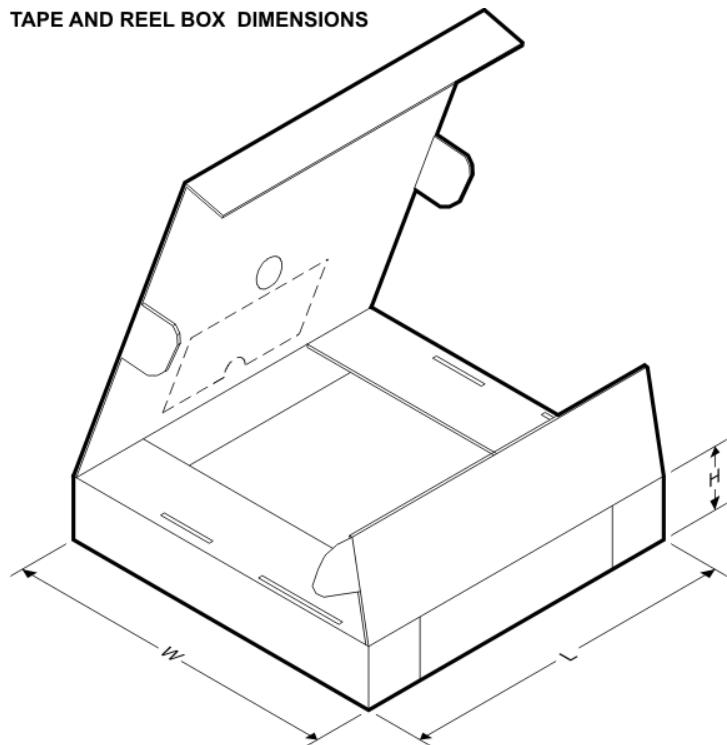
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


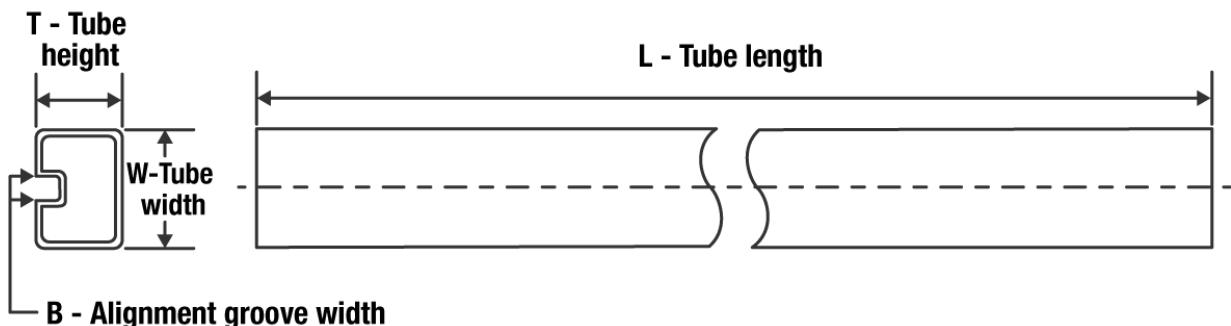
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4511M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4511PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4511PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4511M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4511PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
CD74HC4511PWT	TSSOP	PW	16	250	853.0	449.0	35.0

TUBE


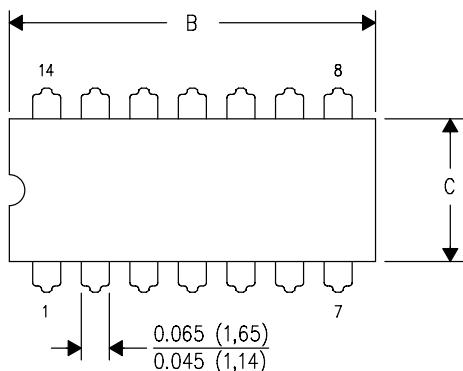
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4511M	D	SOIC	16	40	507	8	3940	4.32
CD74HC4511MG4	D	SOIC	16	40	507	8	3940	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4511EE4	N	PDIP	16	25	506	13.97	11230	4.32

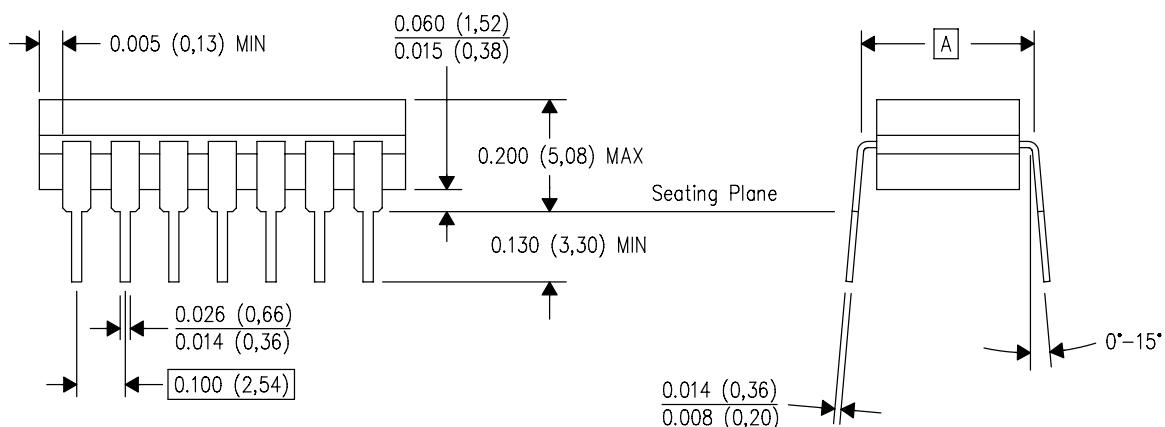
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:

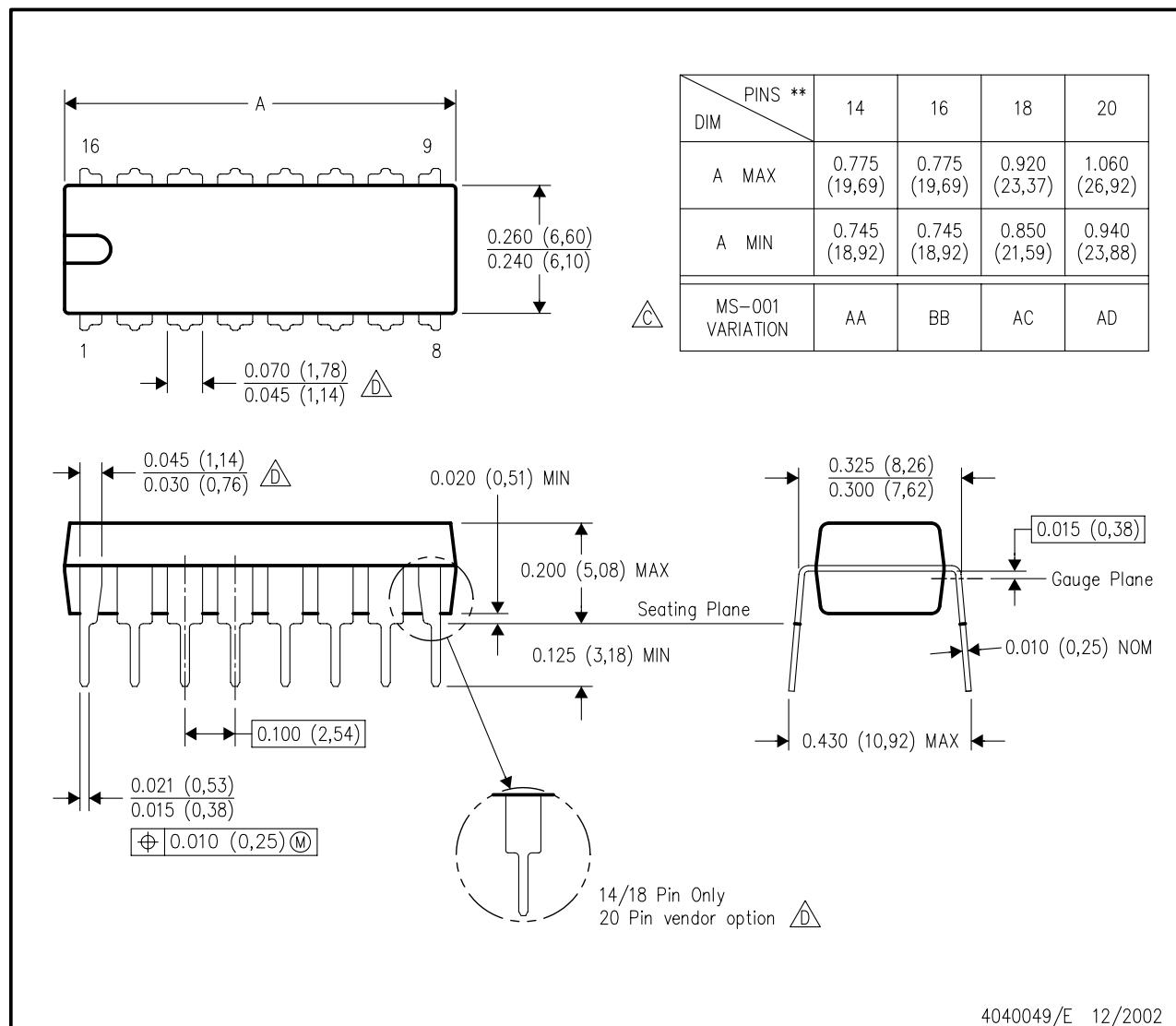
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

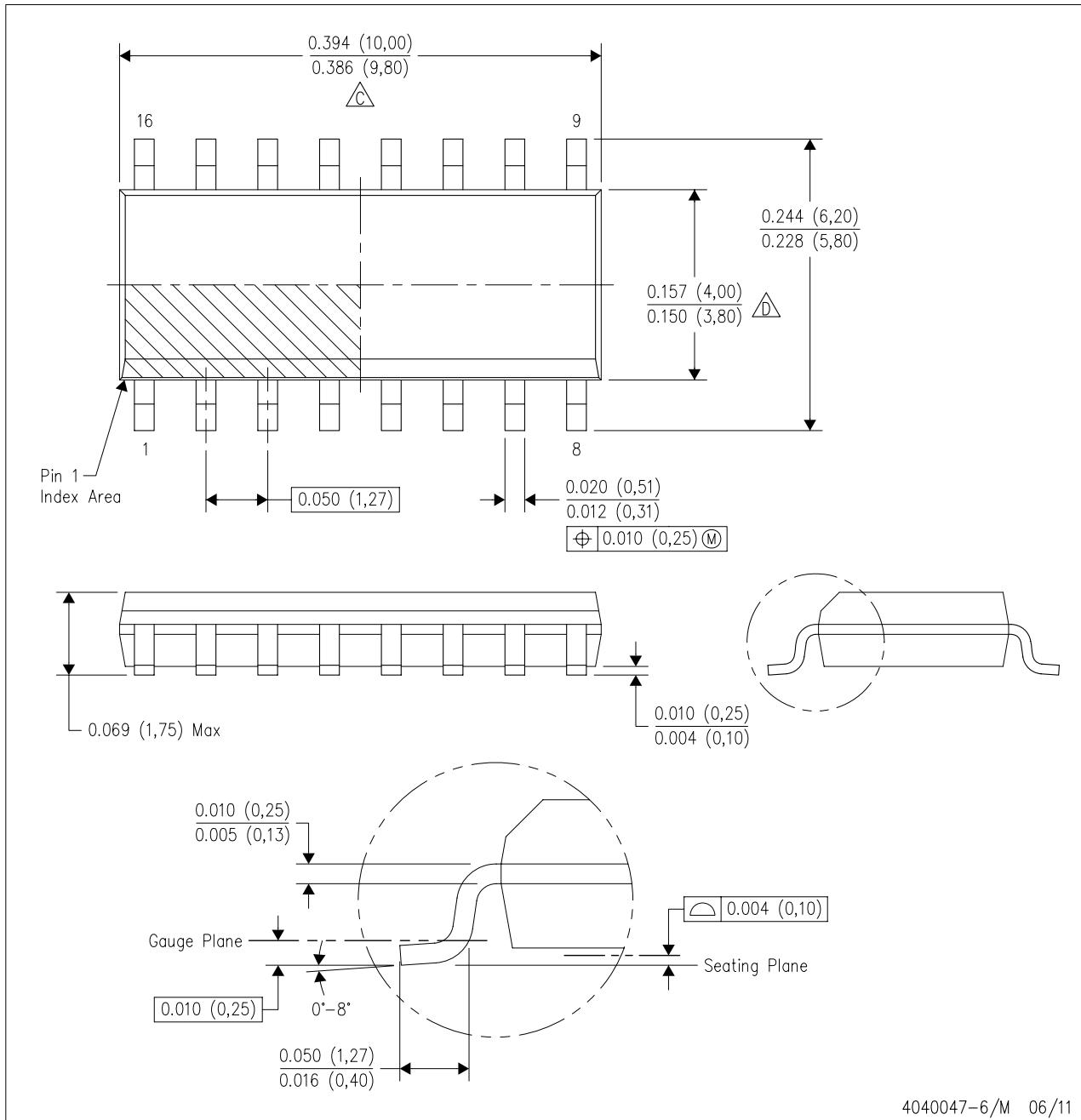


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Symbol C:** Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - Symbol D:** The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

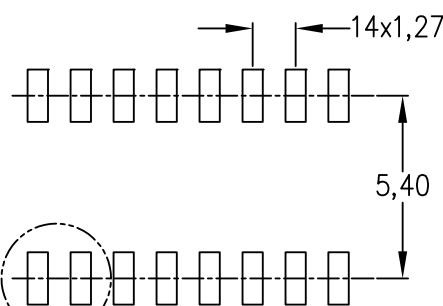
E. Reference JEDEC MS-012 variation AC.

LAND PATTERN DATA

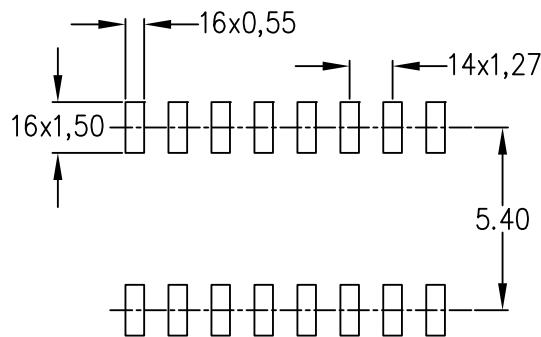
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

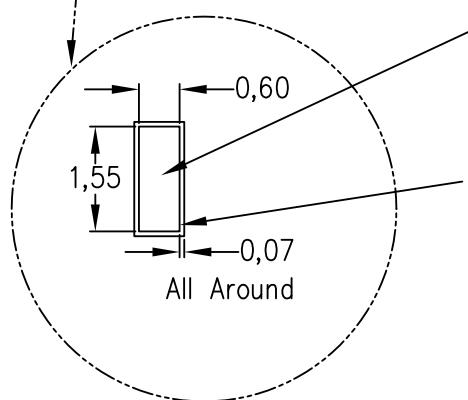
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

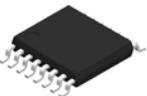
Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

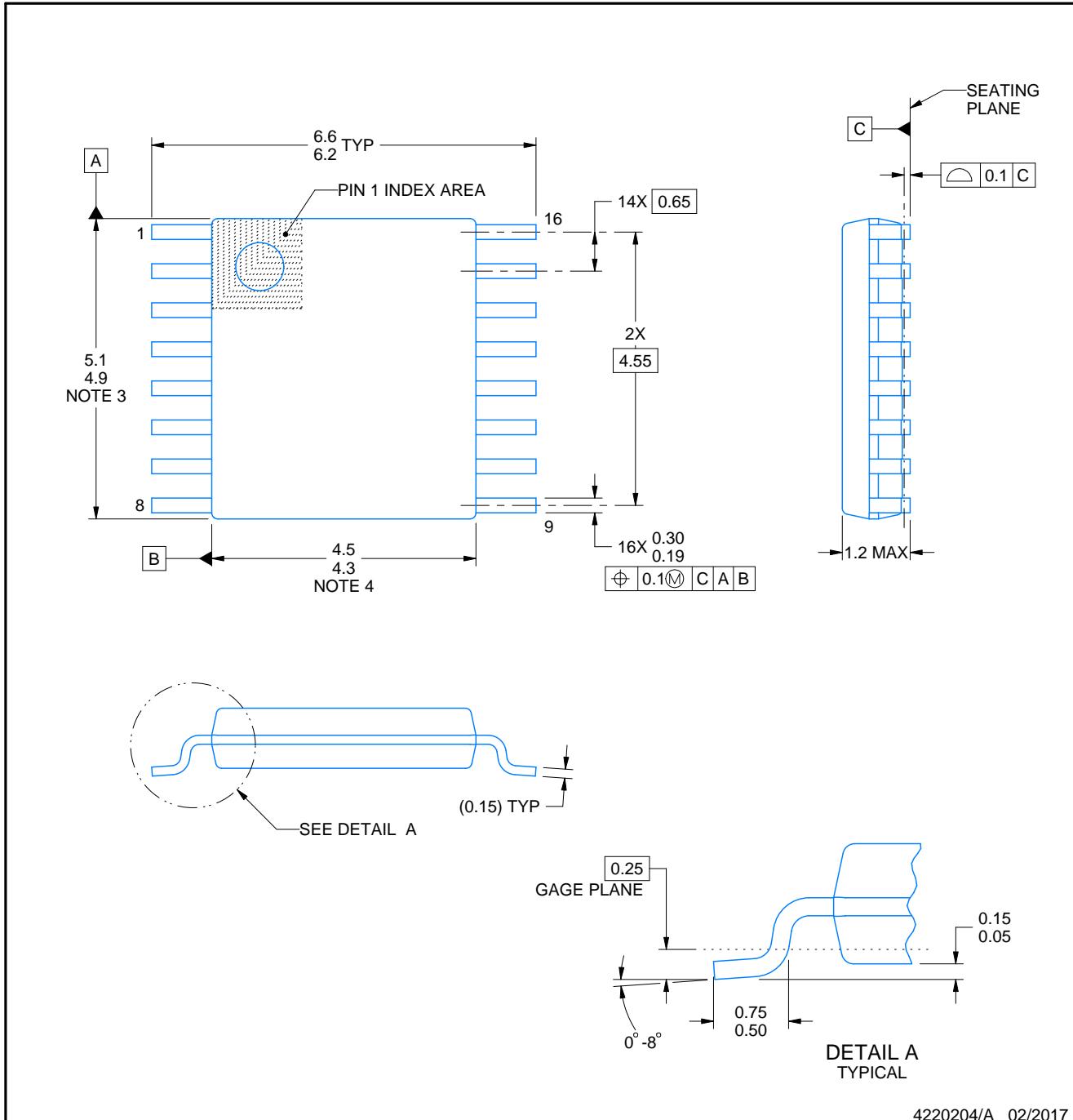
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

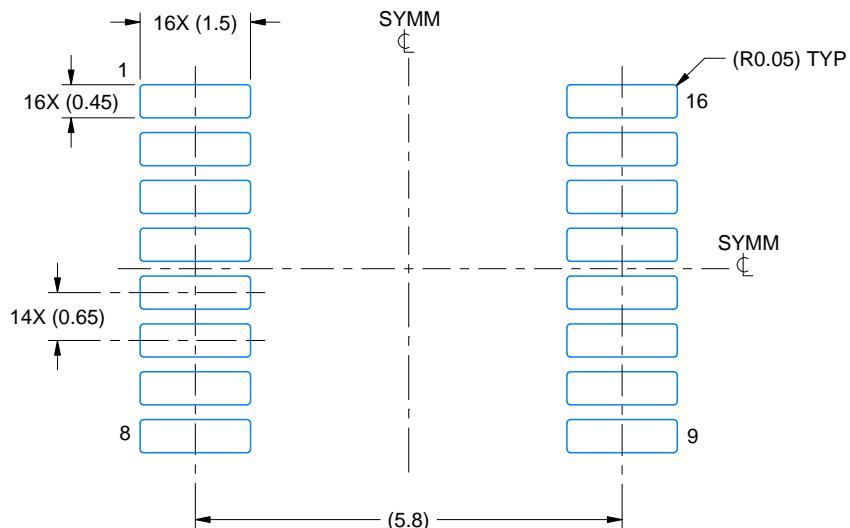
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
 5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

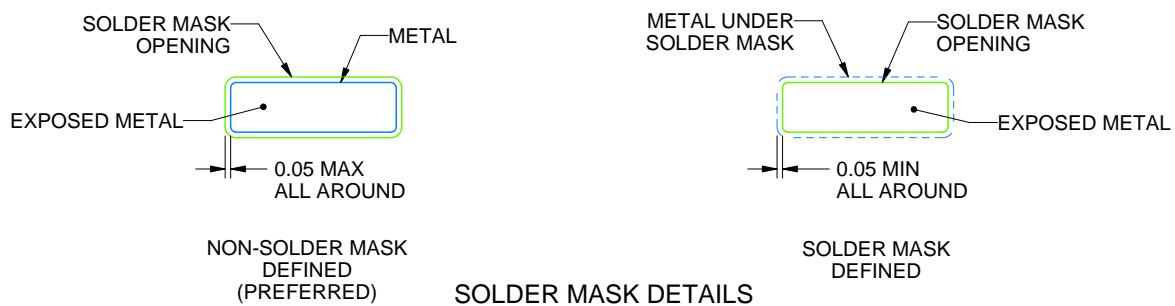
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

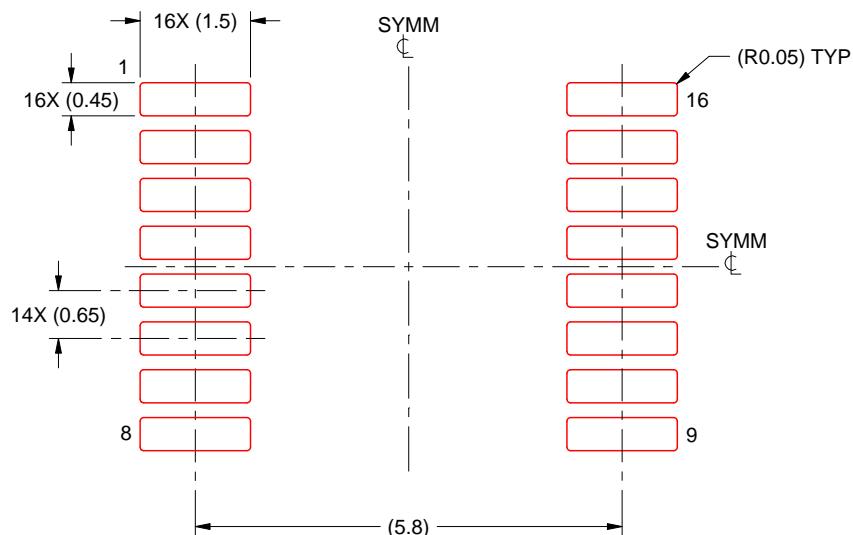
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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