Digital password based lock system

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***Abstract*— Door locks are used for security and protection. No one wants to live in a house that does not have a door and locks. It is important to have door locks so that we feel secure in our homes. Thus, we decided to design a password-based door locking system for our project. We wrote a Verilog code for this following system and implemented it on FPGA using Quartus 2.**

***Keywords*— FPGA, Moore finite state machine, Verilog HDL**

I. INTRODUCTION

(Password based door locking system)

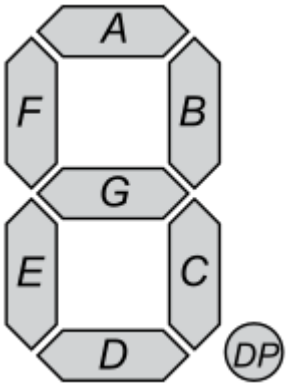
The system includes an electronic control assembly that controls the output load via a numerical password. Once the correct code or password has been entered, the door opens and the person is allowed to enter. If the password is incorrect, the door will be locked, denying access to the person.

A. *Moore finite machine*

a Moore machine is a finite-state machine whose current output values are determined only by its current state. This is in contrast to a Mealy machine, whose output values are determined both by its current state and by the values of its inputs. Like other finite state machines, in Moore machines, the input typically influences the next state. Thus the input may indirectly influence subsequent outputs, but not the current or immediate output.

B. *Seven segment machine*

A seven-segment display is form of electronics display device for displaying decimal device. Seven-segment displays are widely used in digital clocks, electronic meters, basic calculators, and other electronic devices that display numerical information.



In a simple LED package, typically all of the cathodes (negative terminals) or all of the anodes (positive terminals) of the segment LEDs are connected and brought out to a common pin; this is referred to as a "common cathode" or "common anode" device.

In common cathode LED to blink the led we have to give +5 volt (logic 1) to the individual anode, and in common anode for blink a particular led we have to give ground (logic 0) to individual cathode.

C . *Working :*

There are total of 10+1 switches assigned to the FPGA (to enter 0 to 9 + 1 reset switch). Through this switches the user can enter the password.

A clock is assigned to a button of FPGA which is used to trigger the input.

A red LED is assigned for the alarm (for 5 consecutive wrong password) and a green LED is assigned to show access.

A seven segment LED is used to display the number of turns left for the user to enter the password which when reaches zero alarm goes off and the count is reset back to 5 when the correct password is entered. It is also used to display the freeze state of the system.

For the 6^{th} consecutive wrong password the system freezes and can only be reset by the owner.

D. Counter and alarm system :

Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock.

We used a counter which increements once each time a wrong password is entered upto a maximum value of five. When the count reaches 5 an alarm rings. If a 6th time, a wrong password is entered the system gets locked and can only be unlocked by the user. And if at any point during the count the correct password is entered the count is reset to zero.

E. Quartus 2 :

Intel Quartus is programmable logic device design software produced by Intel. Quartus enables analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Quartus includes an implementation of VHDL and Verilog for hardware description, visual editing of logic circuits, and vector waveform simulation.

F. FPGA :

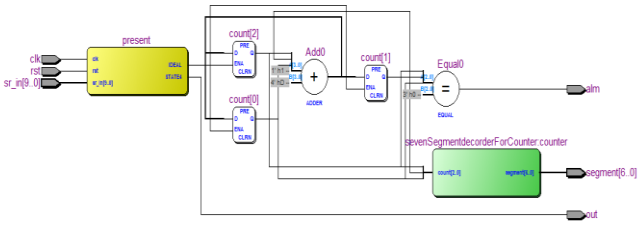
A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence the term field-programmable. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). Circuit diagrams were previously used to specify the configuration, but this is increasingly rare due to the advent of electronic design automation tools.

II. RTL DESIGN OF THE SYSTEM

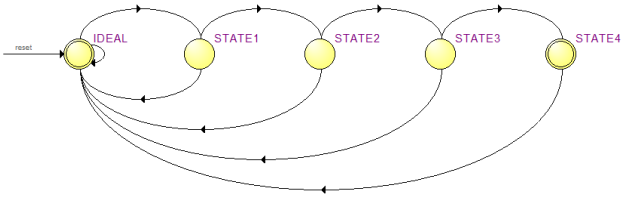
In digital circuit design, register-transfer level (RTL) is a design which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals.

Register-transfer-level abstraction is used in hardware description languages (HDLs) like Verilog and VHDL to create high-level representations of a ircuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level is typical practice in modern digital design.

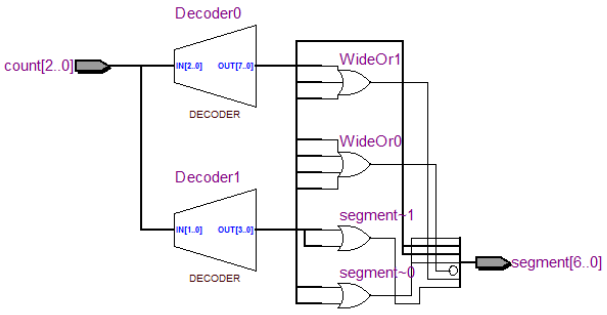
Unlike in software compiler design, where the register-transfer level is an intermediate representation and at the lowest level, the RTL level is the usual input that circuit designers operate on. In fact, in circuit synthesis, an intermediate language between the input register transfer level representation and the target netlist is sometimes used. Unlike in netlist, constructs such as cells, functions, and multi-bit registers are available. Examples include FIRRTL and RTLIL.



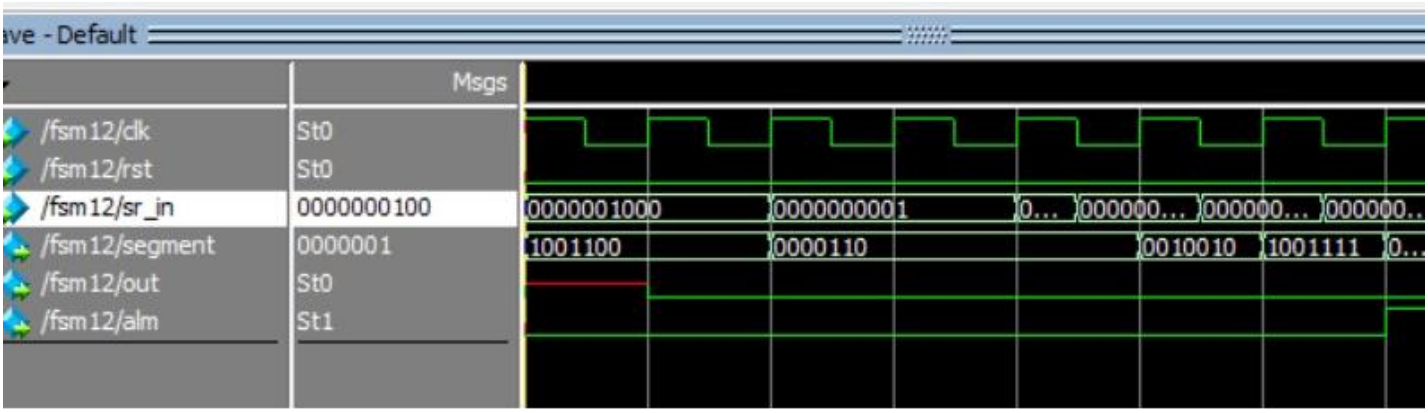
A. FSM module :



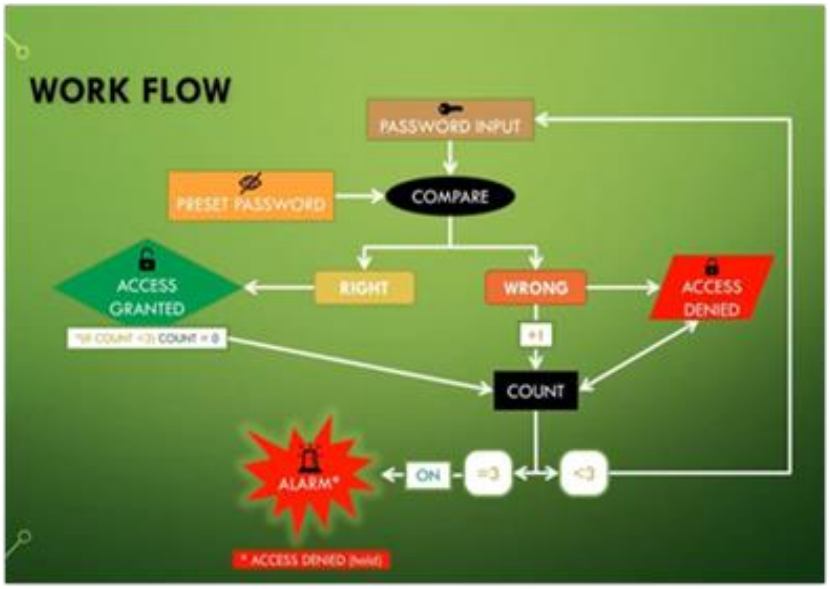
B. Seven segment decoder module *:*



III. SIMULATION



A. Dataflow :



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REFERENCES

https://www.wikipedia.org/

Thank you