JOAQUIN ARMATAGE

DIGITAL DESIGN ENGINEER

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SUMMARY

Electrical Engineer with interest in FPGAs, RTL design and EDA tools. Knowledgeable on the VLSI design process through graduate level coursework, HDL intensive projects and pragmatic industry experience. Looking for an entry level position to start my career.

PROJECTS

Handwritten RISC-V CPU
- Runs 32-bit ISA
- Fitted to a FPGA
- Boots a small Linux distro

2D Convolution on FPGA
- Processes float64 values
- Multiply-accumulate (MAC) modules
- SDRAM controller

Speech Recognition Model
- Trained using audio from Kaggle competition
- CNN machine learning
- Fitted to an FPGA

PROGRAMMING LANGUAGES

- Verilog
- VHDL
- Perl
- Python
- TCL
- C++
- C#
- C
- MATLAB
- BASH

SOFTWARE SKILLS

- Virtuoso
- Spectre X
- Innovus
- Xcelium
- JasperGold
- vManager
- PrimeTime
- PrimeSim
- Synplify
- Linux
- Quartus
- Vivado
- GNU
- VBox

EXPERIENCE

May 2021 – August 2021
Graduate Intern • Digital Design Engineer • Texas Instruments

- Designed RTL for a PCIe Retimer device in development.
- Validated the RTL with a local test bench.
- Instantiated the RTL into the overall design.
- Created new channel registers to operate the added RTL.
- Worked with an intern to validate from the device top level.

May 2020 – August 2020
Undergraduate Intern • Digital Design Engineer • Texas Instruments

- Created an EDA flow for Cadence Jasper Gold Connectivity.
- Wrote TCL and python scripts to drive the software
- Created a Unix directory with a Makefile to run the flow.
- Project will be used to help create a company-wide EDA flow.

May 2019 – August 2019
Undergraduate Intern • Test Engineer • Texas Instruments

- Wrote a test program to upgrade a chip to a new ATE.
- Daily work on the test floor with ATEs.
- Proposed efficient test methods that met yield expectations.

EDUCATION

Arizona State University, May 2021
Bachelor of Science in Engineering • Electrical Engineering
Minor in Mathematics

- Graduated Summa Cum Laude with a 3.98 cumulative GPA
- National Hispanic Merit Scholar
- Beus Scholar
- Relevant Coursework:
  - VLSI Design
  - Constructionist Approach to Microprocessor Design
  - Machine Learning Basics with Application to FPGAs
  - Digital Systems and Circuits