108011235
陳昭維
電機 23

EE3235 Analog Integrated Circuit Analysis and Design I

Homework 3
Cascade Amplifier

Due date: 2021.11.10 (Wed.) 13:20 (upload to eeclass system)

Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

Part I – Cascode Amplifier

(a) Design Process

The common source cascode amplifier is strongly dominated by the output resistance of the PMOS and NMOS, since the gain can be approximated by $A_v = -g_{m,n}(r_{o1} \,||\, r_{o2})$. The output resistance is calculated by $r_o = \frac{1}{\lambda I_D}$. From the 2 above formula, there are 2 approaches to acquire high gain, the first is to boost up the transconductance of the NMOS, but raising up the transconductance makes the drain current larger which inversely drops the output resistance lower. This leads to the second approach, use larger channel length, which diminishes the channel length modulation effect on the transistor. This will increase the output resistance when the transistors are in saturation region. A tradeoff between device size and gain can be observed from here.

From above I start from using 1μm as channel length. Courses from microelectronics reminds me that the mobility of electron is about twice larger than hole, I then set the W/L of PMOS to 2 and W/L of NMOS, and sweeps for the V_{in} and V_{b1} relation for given V_{b1} when V_{out} is at 0.5V. I then also reversed the ratio of NMOS and PMOS to observe if higher gain can be achieved, with surprising result, it actually does. With some few trials of increasing channel length and the fixed ratio relation ($\frac{W}{L}_{NMOS} : \frac{W}{L}_{PMOS} = 2:1$), I achieved the SPEC goals by setting $\frac{W}{L}_{NMOS} = \frac{3.82\mu m}{1.91\mu m} \frac{W}{L}_{PMOS} = \frac{1.91\mu m}{1.91\mu m}$ *and* $V_{in} = 0.4V, V_{b1} = 1.1\,V$. During design, I found out that with small changes on device such as gate voltage or channel width and length can drastically affect the performance.

(b)

.tf

```
****      small-signal transfer characteristics

      v(vout)/vin                                  =  -107.7740
      input resistance at                 vin      =   1.000e+20
      output resistance at v(vout)                 =     3.8525x
```

.op

```
**********************************************************************
******  option summary
******
runlvl   = 5          bypass   = 2.0000
**info** dc convergence successful at Newton-Raphson method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
******
.protect

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb1     =   1.1000  0:vdd     =   1.8000  0:vin     = 400.0000m
+0:vout    = 498.4701m 0:vss     =   0.


maximum nodal capacitance=   6.613E-14         on node     0:vss

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb1     =  23.3468f 0:vdd     =  37.7989f 0:vin     =  43.7248f
+0:vout    =   7.4827f 0:vss     =  66.1338f


**** voltage sources

subckt
element  0:vin      0:vb1      0:vdd      0:vss
 volts    400.0000m    1.1000     1.8000     0.
 current    0.         0.        -1.5238u   49.4473a
 power      0.         0.         2.7428u    0.

    total voltage source power dissipation=    2.7428u       watts
```

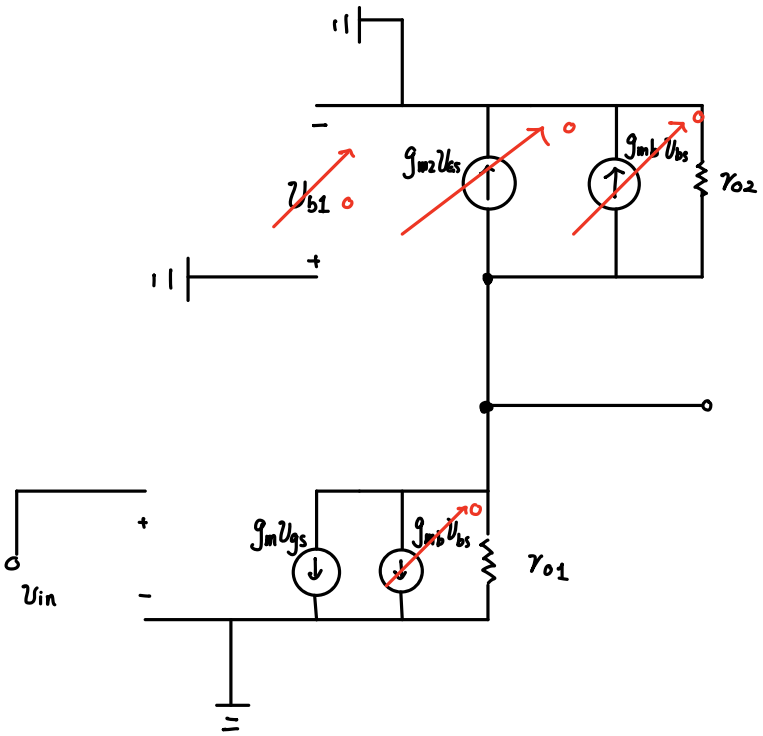
```
**** mosfets


subckt
element   0:mp1        0:mn1
model     0:p_18.1     0:n_18.1
region    Saturation   Saturation
 id         -1.5238u      1.5238u
 ibs       2.115e-22   -2.839e-22
 ibd        165.9053a   -170.5694a
 vgs       -700.0000m    400.0000m
 vds        -1.3015      498.4701m
 vbs          0.           0.
 vth       -486.4380m    354.6310m
 vdsat     -206.6975m     80.2505m
 vod       -213.5620m     45.3690m
 beta        67.2814u    606.2986u
 gam eff    557.0846m    507.4459m
 gm          12.3797u     27.9754u
 gds         25.0682n    234.5027n
 gmb          3.8440u      5.7626u
 cdtot        2.1140f      5.3687f
 cgtot       23.3468f     43.7248f
 cstot       26.9468f     45.4175f
 cbtot       10.8522f     20.7163f
 cgs         20.8850f     37.1248f
 cgd        686.3449a      1.3439f
```

From part (a) with known formula $A_v = -g_{m,NMOS}\,(r_{o,N} \,||\, r_{o,P})$, from above operating point information, transconductance of the NMOS is $g_{m,NMOS} = 27.9754\ \mu S$, $r_{o,N} = \frac{1}{g_{ds,NMOS}} = \frac{1}{234.5027\times10^{-9}}\ \Omega$,

$r_{o,P} = \frac{1}{g_{ds,PMOS}} = \frac{1}{25.0682\times10^{-9}}\Omega$

This leads to $A_v = -27.9754 \times 10^{-6} \times \left(\frac{1}{234.5027\times10^{-9}+25.0682\times10^{-9}}\right) = -107.7756\ V/V$

The relative error rate is $\left|\frac{-107.7756+107.774}{107.774}\right| = 1.48 \times 10^{-3}\%$, which is almost identical between simulation value and hand calculate value.



$g_{m1} = 27.9754\ \mu S$

$g_{ds,n} = 234.5027\ nS$

$g_{ds,p} = 25.0682\ nS$

$$A_V = -27.9754 \times 10^{-6} \times \left(\frac{1}{234.5027 \times 10^{-9}} \,//\, \frac{1}{25.0682 \times 10^{-9}} \right)$$

$$= -107.7756\ V/V$$

(c) (d)

I choose W/L = $\frac{1.5\ \mu m}{0.35\ \mu m}$ and V_{b2} to 1.16 V to achieved the spec

.tf

```
****      small-signal transfer characteristics

      v(vout)/vin                                =    10.2693
      input resistance at                 vin    =     9.7378k
      output resistance at v(vout)               =    65.8648k
```

.op

```
**********************************************************************
******  option summary
******
runlvl   = 5          bypass   = 2.0000
**info** dc convergence successful at Newton-Raphson method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
******
.protect

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb2     =   1.1600  0:vdd     =   1.8000  0:vin     = 500.0000m
+0:vout    = 796.1436m 0:vss     =   0.


maximum nodal capacitance=   4.887E-15          on node     0:vin

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb2     =   4.0128f 0:vdd     =   0.      0:vin     =   4.8867f
+0:vout    =   2.0725f 0:vss     =   0.


**** voltage sources

subckt
element  0:vin      0:vb2      0:vdd      0:vss
 volts    500.0000m    1.1600     1.8000     0.
 current   10.0386u    0.        -10.0386u   -1.2964p
 power     -5.0193u    0.         18.0694u   0.

    total voltage source power dissipation=   13.0501u       watts
```

```
**** resistors

subckt
element  0:rd
 r value  100.0000k
 v drop     1.0039
 current   10.0386u
 power     10.0773u


**** mosfets

subckt
element  0:mn2
model    0:n_18.1
region   Saturation
 id        10.0386u
 ibs      -89.2925a
 ibd     -142.1728a
 vgs       660.0000m
 vds       296.1436m
 vbs      -500.0000m
 vth       566.5795m
 vdsat     131.5512m
 vod        93.4205m
 beta        1.4275m
 gam eff   519.9009m
 gm        134.0418u
 gds         5.1838u
 gmb        16.7241u
 cdtot       2.0725f
 cgtot       4.0128f
 cstot       4.8867f
 cbtot       3.6991f
 cgs         3.1457f
 cgd       543.6366a
```

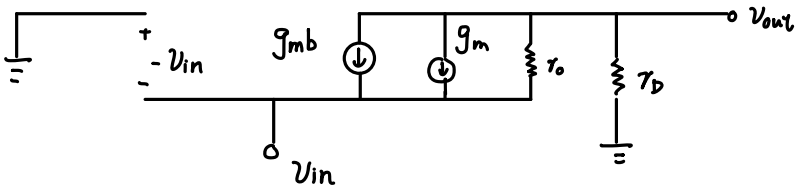
From small signal model of common gate amplifier considering body conductance is

$A_V = \left(g_m + g_{mb} + \frac{1}{r_o}\right)(r_D \,||\, r_o)$, from above operating point information, $g_m = 134.0318 \times 10^{-6}\ S$

$g_{mb} = 16.7241 \times 10^{-6}\ S$, $\frac{1}{r_o} = g_{ds} = 5.1838 \times 10^{-6}\ S$, $r_o = \frac{1}{5.1838 \times 10^{-6}}\ \Omega$

$$A_V = \left(g_m + g_{mb} + \frac{1}{r_o}\right)(r_D \,||\, r_o) = (155.9497 \times 10^{-6}) \times 65859.6662 = 10.2708\ V/V$$

The relative error rate is $\left|\frac{10.2708 - 10.2693}{10.2693}\right| = 0.015\%$, which is almost identical between simulation value and hand calculate value.



$$A_V = \left[g_m + g_{mb} + \frac{1}{r_o} \right] (r_D \,//\, r_o)$$

$$= \left[134.0418 \times 10^{-6} + 16.7241 \times 10^{-6} + 5.1838 \times 10^{-6} \right]$$

$$\times \left[100 \times 10^{3} \,//\, \frac{1}{5.1838 \times 10^{-6}} \right]$$

$$= (155.9497 \times 10^{-6}) \times 65859.6662$$

$$= 10.2708 \ \text{V/V}$$

(e)

```
******************************************************************
******  option summary
******
runlvl  = 5         bypass  = 2.0000
**info** dc convergence successful at Newton-Raphson method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
******
.protect

****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb1     =   1.1000  0:vb2     =   1.1600  0:vdd     =   1.8000
+0:vin     = 400.0000m 0:vout    = 799.9505m 0:vss     =   0.
+0:vx      = 500.3702m


maximum nodal capacitance=   6.613E-14         on node     0:vss

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb1     =  23.3469f 0:vb2     =   4.0115f 0:vdd     =  37.7994f
+0:vin     =  43.7262f 0:vout    =   2.0707f 0:vss     =  66.1339f
+0:vx      =  12.3664f
```

```
**** current sources

subckt
element  0:i1
 volts    500.3702m
 current   10.0000u
 power     -5.0037u


    total current source power dissipation=  -5.0037u       watts

**** resistors

subckt
element  0:rd
 r value  100.0000k
 v drop     1.0000
 current   10.0005u
 power     10.0010u
```

```
**** mosfets


subckt
element  0:mp1       0:mn1       0:mn2
model    0:p_18.1    0:n_18.1    0:n_18.1
region   Saturation  Saturation  Saturation
 id        -1.5237u     1.5242u   10.0005u
 ibs      2.115e-22  -2.840e-22   -89.3586a
 ibd       165.6631a  -171.2196a  -142.8527a
 vgs      -700.0000m   400.0000m   659.6298m
 vds        -1.2996    500.3702m   299.5803m
 vbs         0.           0.      -500.3702m
 vth      -486.4380m   354.6215m   566.5581m
 vdsat    -206.6975m    80.2555m   131.3200m
 vod      -213.5620m    45.3785m    93.0716m
 beta       67.2814u   606.2981u     1.4275m
 gam eff   557.0846m   507.4459m   519.9092m
 gm         12.3793u    27.9820u   133.8095u
 gds        25.0914n   234.4641n     5.1114u
 gmb         3.8439u     5.7637u    16.6901u
 cdtot       2.1145f     5.3665f     2.0707f
 cgtot      23.3469f    43.7262f     4.0115f
 cstot      26.9468f    45.4197f     4.8854f
 cbtot      10.8526f    20.7142f     3.6976f
 cgs        20.8850f    37.1263f     3.1444f
 cgd       686.3508a     1.3438f   543.4210a
```

```
**** voltage sources

subckt
element  0:vin       0:vb1       0:vb2       0:vdd       0:vss
 volts    400.0000m    1.1000      1.1600      1.8000      0.
 current     0.           0.          0.       -11.5242u   -1.3008p
 power       0.           0.          0.        20.7436u    0.

    total voltage source power dissipation=   20.7436u       watts
```

Comment:

(i)

V_x has slight changes comparing to common source stage (which is 498.4701 mV) and the common gate stage (which is fixed at 0.5V), V_x is biased at 500.3702 mV, which is biased at a neglectable small increase voltage comparing to the 2 previous case.

(ii)

```
****     small-signal transfer characteristics

     v(vout)/vin                              =    -2.7911
     input resistance at              vin     =  1.000e+20
     output resistance at v(vout)             =   99.9149k
```

Comment:

The gain from the transfer function is -2.7911 V/V, whereas the value acquired from multiplying the gain from individual gain stage is $A_1 \times A_2 = -107.7740 \times 10.2693 = -1106.7635\ V/V$

The reason for this significant drop is because simply multiplying both values hasn't taken the effect of the input impedance from the common gate amplifier to the common source amplifier into account.

The gain of common source amplifier should be adjusted from $-g_{m,MN1} \times (r_{o,MN1} \parallel r_{o,MP1})$ into $-g_{m,MN1} \times (r_{o,MN1} \parallel r_{o,MP1} \parallel (\frac{1}{g_{m,MN2}}) \parallel R_{current\ source})$, consider that the current source is ideal, so it's resistance is close to infinite. The gain can be calculated as $A_1 = -27.9820 \times 10^{-6} \times \frac{1}{25.0914 \times 10^{-9} + 234.4641 \times 10^{-9} + 133.8095 \times 10^{-6}} = -0.2087\ V/V$

Then the overall gain should be $A_{V,overall} = -0.2087 \times 10.2693 = 2.1432$ V/V

The value still varies a bit from the acquired gain, so I decided to probe the gain at Vx.

```
****     small-signal transfer characteristics

     v(vx)/vin                                = -271.0849m
     input resistance at             vin      =  1.000e+20
     output resistance at v(vx)               =    9.6880k
```

The value above shows that the gain I calculated was undervalued. With the result from above, $A_{V,overall} = -271.0849 \times 10^{-3} \times 10.2693 = -2.7839\ V/V$, which is very close to $-2.7911\ V/V$.

Then I decided to use the input impedance from part (c) (d)

```
input resistance at             vin      =    9.7378k
```

to calculate the gain

$$A_V = -27.9820 \times 10^{-6} \times \frac{1}{25.0914 \times 10^{-9} + 234.4641 \times 10^{-9} + \frac{1}{9.7378 \times 10^{3}}} \times 10.2693$$

$$= -27.9820 \times 10^{-6} \times 9713.2498 \times 10.2693$$

$$= -2.7912\ V/V \Rightarrow \text{which is identical to the simulation}$$

This once again reminds me that when there is voltage difference between source and bulk, I must always taken body conductance into account.

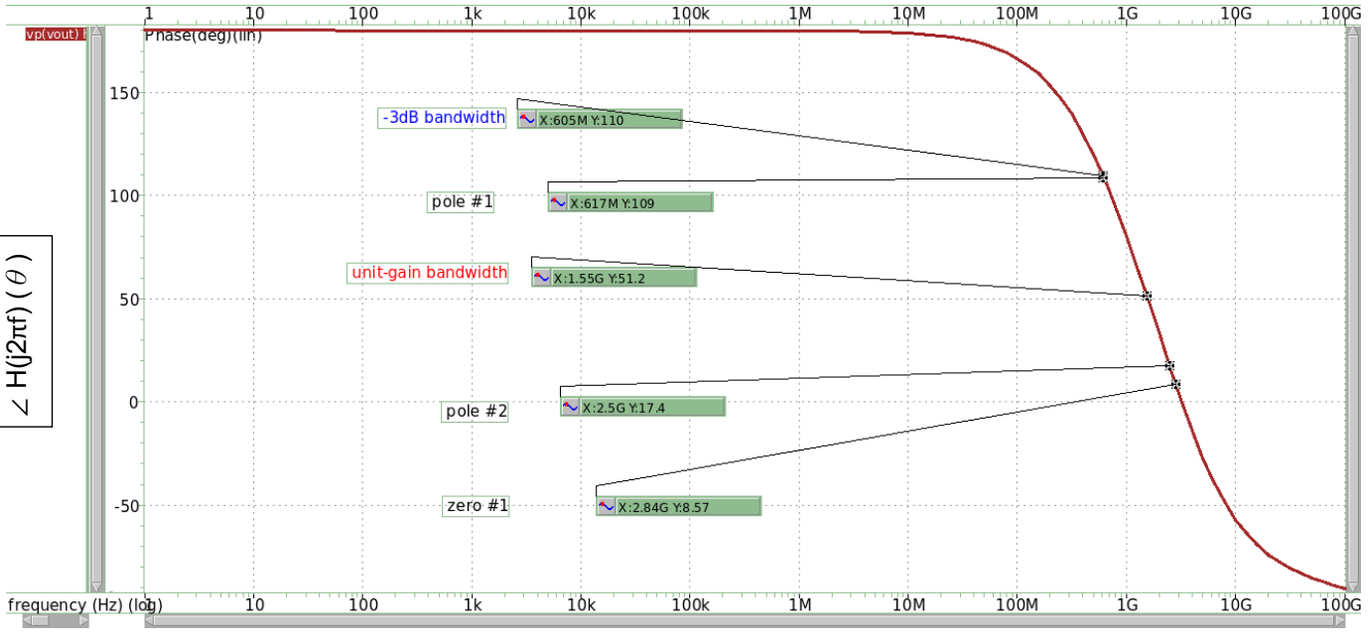
(f)

```
**************************************************
  ******   pole/zero analysis

   input =  0:vin          output = v(vout)

      poles (rad/sec)                 poles ( hertz)
real            imag            real            imag
-3.87643g       0.              -616.953x       0.
-15.7140g       0.              -2.50096g       0.

      zeros (rad/sec)                 zeros ( hertz)
real            imag            real            imag
17.8238g        0.              2.83675g        0.

 ***** constant factor = 9.53881g
******
.protect

****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=   8.9155     at=   6.3096
             from=   1.0000     to= 100.0000g
bw= 607.6032x
ugb=   1.5519g
```

| H(j2πf) | (dB)

Frequency (Hz)

Phase - Frequency



∠ H(j2πf) (θ)

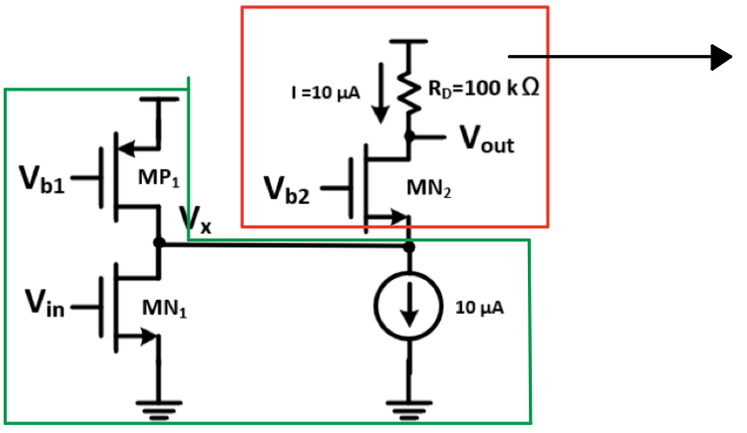
Frequency (Hz)

(g)

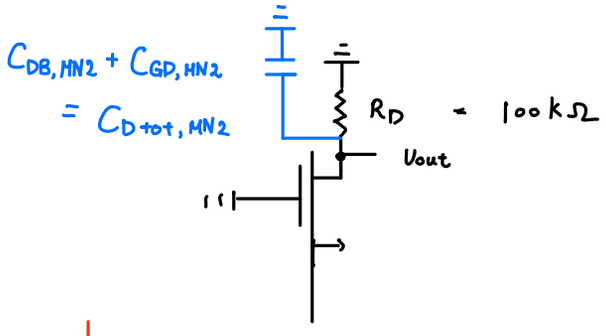
```
**************************************************
******    pole/zero analysis

   input =  0:vin          output = v(vout)

      poles (rad/sec)                poles ( hertz)
real             imag           real             imag
-3.87643g        0.             -616.953x        0.
-15.7140g        0.             -2.50096g        0.

      zeros (rad/sec)                zeros ( hertz)
real             imag           real             imag
17.8238g         0.             2.83675g         0.
```

element	0:mp1	0:mn1	0:mn2
model	0:p_18.1	0:n_18.1	0:n_18.1
gm	12.3793u	27.9820u	133.8095u
gds	25.0914n	234.4641n	5.1114u
gmb	3.8439u	5.7637u	16.6901u
cdtot	2.1145f	5.3665f	2.0707f
cgtot	23.3469f	43.7262f	4.0115f
cstot	26.9468f	45.4197f	4.8854f
cbtot	10.8526f	20.7142f	3.6976f
cgs	20.8850f	37.1263f	3.1444f
cgd	686.3508a	1.3438f	543.4210a

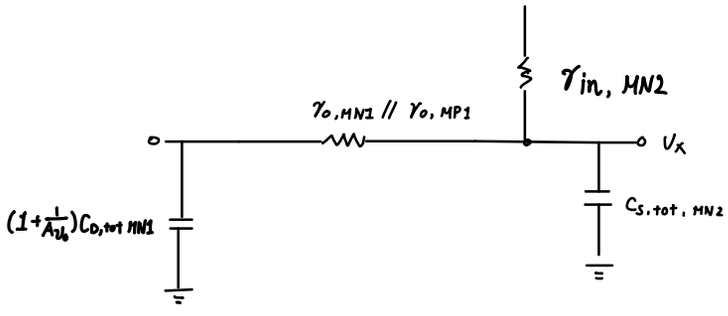
```
maximum nodal capacitance=   6.613E-14       on node     0:vss

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb1     =  23.3469f 0:vb2     =   4.0115f 0:vdd     =  37.7994f
+0:vin     =  43.7262f 0:vout    =   2.0707f 0:vss     =  66.1339f
+0:vx      =  12.3664f
```



(c)



the resistance is significant larger, so this is clear to be the dominant pole.



$$|\omega_{p,out}| = \frac{1}{R_D \times C_{Dtot,MN2}}$$

$$= \frac{1}{100\,k \times 2.0707\,f}$$

$$= 4829.28 \times 10^6 \ (rad/s)$$

$$= 768.6\ MHz$$

$$(r_{o,MN1} \,//\, r_{o,MP1} \,//\, r_{in,MN2})$$

$$= \frac{1}{25 \times 10^{-9} + 234.46 \times 10^{-9} + 9737.8}$$

$$= 9713.258\ \Omega$$

For the pole at V_x, since the drain capacitance of MN1 floats from V_{in} to V_x, to avoid the error from miller approximation, I will use `+0:vx = 12.3664f`

$$\Rightarrow \left| \omega_{p,x} \right| = \frac{1}{9713.258 \times 12.3664 \times 10^{-15}} = 8.325 \times 10^{9} \text{ rad/s}$$

$$= 1.325 \text{ GHz}$$

Comment:

The dominant pole calculated has a certain amount of difference. Comparing to classmates with the same approach of calculating it, they all have a close hand calculation value compare to the simulation value. I notice that the differences between our design is the size of MN2, my channel length of MN2 is 0.35µm, the neglection of drain-source capacitance will cause larger error because the drain and source are closer in my design, so my speculation would be that the realistic node capacitance would be higher. Without the consideration of drain source capacitance, the equivalence capacitance at node V_{out} is smaller, which causes the pole to be larger, which corresponds to the larger value I acquired from hand calculation.

The second pole isn't close either, the courses from past weeks have taught us that to get the actual transfer function, the direct analysis using KCL and KVL must be done. But if we are simply looking both poles in terms of order, then it is still a good approximation.

There are more to be observed, I found out that with a smaller size of my channel length of MN2, this causes my dominate pole to be 10 times larger compared to my classmates. Meanwhile, the gain is 1.5 ~ 2 times smaller compared to my classmates. There is a trade-off between gain and bandwidth in this cascade design. I personally think that having larger bandwidth is a better design, because courses of communication system, the need of implementing communication is highspeed circuit.

(h)

Table I Perforamance Table

Work Item	Unit	Specification	Simulation	Calculation
Vdd	V	1.8		
	Common Source Amplifier			
Vin	V	-	0.4 V	
Vb1	V	-	1.1 V	
Vx	V	0.5	498.4701 mV	
Gain($\lvert A_1 \rvert$)	V/V	> 90	107.774 V/V	107.7756 V/V
	Common Gate Amplifier			
Vin	V	0.5	0.5 V	
Vo	V	-	796.1436 mV	
I	μA	10	10.0386 μA	
Gain($\lvert A_2 \rvert$)	V/V	> 10	10.2693 V/V	10.2708 V/V
	Cascade Amplifier			
Vin	V	-	0.4 V	
Vx	V	0.5	500.3702 mV	
Vo	V	-	799.9505 mV	
Gain ($\lvert A_1 \times A_2 \rvert$)	V/V	> 1	2.7911 V/V	
Dominate Pole	MHz	> 55	616.953 MHz	768.6 MHz
Unit Gain Bandwidth	MHz	> 70	1.5519 GHz	