110 Fall EE3235 Analog Integrated Circuit Analysis and Design I

Homework 6 Differential amplifier

Due date:2021.12.22(Wed.) 13:20 pm (upload to eeclass System)

This homework is for you to design a source-coupled pair stage. The problem sets include HSPICE simulations and hand calculations. The SPICE model is cic018.l. Please use the parameters from HSPICE simulation results for hand calculations.

In this differential pair circuit, please use V_{DD}=1.8V, temperature=25°C.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report in **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include the output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

1. Circuit Design

Please design the device size of MX, MS, diode-connection transistor MR, and the bias voltage VBS and VBS1, to make the small differential signal voltage gain (Vout/Vi) larger than 9 (V/V). Please print out the small-signal parameters of active devices from the list file. Please write down your design flow in detail.

Design Flow(這 part 使用中文)

因為這次的 PMOS 是 diode connect，所以從 Vout 向上看的 Impedance 是$\frac{1}{g_{m,R}} \parallel r_{o,R}$ 而向下看是$r_{o,X}$，因此這個 differential gain 就會是 $g_{m,X}\left(\frac{1}{g_{m,R}} \parallel r_{o,R} \parallel r_{o,X}\right) \approx \frac{g_{m,X}}{g_{m,R}}$ ， 這說明著在同樣的 saturation drain current 之下兩者能夠導通的電流的能力要相差 9 倍. 以 device dimensions 來看的話 $A_V \approx -\sqrt{\frac{\mu_N \frac{W}{L}_X}{\mu_P \frac{W}{L}_P}}$ ，因此可以預期 NMOS 的 W/L 會遠大於 PMOS 的 W/L。

從 $\frac{g_{m,X}}{g_{m,R}}$ 角度來看，如果撇除掉 channel length modulation 的影響，可以列出

$g_{m,R} = \frac{2I_D}{V_{DD}-V_{out}-|V_{TH,R}|}$ $g_{m,X} = \frac{2I_D}{V_{BS}-V_X-V_{TH,X}}$ ，兩者相除可得 $\frac{g_{m,X}}{g_{m,R}} = \frac{\mu_p \frac{W}{L}_R (V_{DD}-V_{out}-|V_{TH,R}|)}{\mu_n \frac{W}{L}_X (V_{BS}-V_X-V_{TH,X})}$ 因此可以預期 V_{out} 的那點電壓要降到非常低而 $V_{GS,X}$ 可能要非常貼近 threshold voltage.

再來根據三顆 MOS 的 saturation drain current 公式(不考慮 channel length modulation)我可以列出以下

$$I_{D,R} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}_R(1.8 - V_{out} - |V_{TH,R}|)^2 \qquad I_{D,X} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_X(V_{BS} - V_X - V_{TH,X})^2$$

$$I_{D,S} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_X(V_{BS1} - V_{TH,S})^2$$

W	L	VDD	Vout	VTH,MR	ID	Vov				
		1.8			#DIV/0!	1.8				
								Vout	VBS - VTH,Mx	Saturation detect
								0	0	0
W	L	VBS	VX	VTH,Mx	ID	VOV				
					#DIV/0!	0		Vx	VBS1-VTH,Ms	Saturation detect
								0	0	0
W	L	VBS1		VTH,Ms	ID					
					#DIV/0!					

因此利用了 EXCEL 做出了一個 ID 試算表 藍色格子是 active floating 的電壓點、橘色格子是會變動的 Threshold voltage、綠格子則是對 tail current MOS 以及中間 NMOS 的 bias gate voltage. 右側的格子則是確定$V_{DS} > V_{GS} - V_{TH}$。而在做這個之前要先了解$\mu_n C_{ox}$ 和 $\mu_p C_{ox}$。 隨著 size 的變動 $\mu_p C_{ox}$大約落在$55 \sim 65\ \mu A/V^2$ 而 $\mu_n C_{ox}$ 大約落在 $300 \sim 350\ \mu A/V^2$，因此在估計時就使用 60 和 325 $\mu A/V^2$ 作為估計值。

我一開始設計的時候是從上往下思考，因為 PMOS 的結構讓他導通後會一直在 saturation region. 所以就設定預期的 Vout 的位置以及 PMOS 選用的 Size 後的 threshold voltage 來算出 drain current，之後就讓下面兩顆的 MOS 的各項參數去匹配這個電流大小。像是$I_{D,R} = I_{D,X}$ 和 $2I_{D,R} = I_{D,S}$。但實際做起來就發現 Vout 的可預期性太低了，因為我的假設是把這個 floating voltage 壓在某個點，來控制其他會移動的點，但還有許多小訊號參數和別的效應沒考慮到，例如 PMOS 的 VSD 不斷增加使 channel length modulation 的效應增強，以至於跑模擬時的那個點不如預期。

因此轉換思考的方向，即使下面的 current source 不是 cascode structure 讓他沒那麼貼近 ideal current source, 但那個節點的相對浮動程度會相對穩定，而且也只要單純考慮$(V_{BS1} - V_{TH,S})$ 計算出 drain current 後，再回去上面的 PMOS 和 NMOS 設計匹配的電流大小並且往自己預期的方向調整。

在設計的過程會發現那個 tail MOS 的節點電壓會越來越低，因此 gate bias 要更加靠近 threshold voltage。因為這個趨勢但同時要導通大的電流因此需要懸殊的 W/L 比例。

在設計過程中讓有讓 $\frac{g_{m,X}}{g_{m,R}}$ 的值符合了 gain 應該要到達的大小，但因為當時的 NMOS size 的 W/L 太大導致於 NMOS 的r_o太小，於是我的 gain 不能單純地用 transconductance 相除值來估計。此時 Vout 的電壓也被拉到非常低的電壓。因此能做的改善就是把想辦法把那個 floating 的電壓稍微往上推，並且讓 NMOS 的 W/L 以及總體電流下降，因此也同時需要調整 tail current 的 biasing level 和 PMOS 的 size。在最後的調整的當中發現其實 PMOS 和 NMOS 在做電流匹配的時候可以讓 PMOS 的電流設定小一點，因為我預期那個 Vout 會在很低電壓的位置，從 VDD 到 Vout 會橫跨很大的 VSD 因此 channel length modulation 的效應會更顯著。

和同學比較設計過後其實發現自己當初的想法和憂慮是錯誤的，我原本想說要不要用 m > 1 來達成 transconductance 的差距，但當時我很擔心 capacitance 的值會遽增讓 pole 很小，但事實上這些 MOS 的電容在折數很低的時候都遠比 load capacitor 還小。再加上這個 amplifier 的 gain 不大，因此原本因為被 miller effect 增大的 floating capacitance 即使折數上升變更大但還是遠不及 load capacitor 的 2pF，且以結果來看即使只用 load capacitance 來當 approximation nodal capacitance 和 pole approximation 其實也可以。因此只要能確保 NMOS 的 r_o 不要變得太小(gain 上不去)或太大(pole 太

小)，事實上 m>1 會有更大的設計彈性，尤其是可以避免為了大 W/L 因此選用小 channel length 導致在 short channel 時會有太大的 threshold voltage。

Device Parameters

```
**** mosfets

subckt
element  0:mr1      0:mr2      0:mx1      0:mx2      0:ms
model    0:p_18.1   0:p_18.1   0:n_18.1   0:n_18.1   0:n_18.1
region   Saturation Saturation Saturation Saturation Saturation
  id     -115.3295u -115.3295u  115.3295u  115.3295u  230.6590u
  ibs      1.576e-20  1.576e-20 -346.1281a -346.1281a -3.421e-20
  ibd    193.3928a  193.3928a   -2.2225f   -2.2225f -338.8685a
  vgs     -1.4718    -1.4718   473.8924m  473.8924m  521.0000m
  vds     -1.4718    -1.4718   277.0752m  277.0752m   51.1076m
  vbs      0.         0.       -51.1076m  -51.1076m    0.
  vth    -527.5830m -527.5830m  454.2207m  454.2207m  519.4805m
  vdsat  -813.6996m -813.6996m   79.8353m   79.8353m   88.0557m
  vod    -944.2342m -944.2342m   19.6717m   19.6717m    1.5195m
  beta    295.7659u  295.7659u   61.6244m   61.6244m  185.3948m
  gam eff 557.0838m  557.0838m  508.8586m  508.8586m  507.4461m
  gm      195.9626u  195.9626u    2.2582m    2.2582m    3.5854m
  gds       7.7016u    7.7016u   46.7159u   46.7159u    2.8474m
  gmb      67.2754u   67.2754u  428.0280u  428.0280u  542.2045u
  cdtot     2.1661f    2.1661f  135.4417f  135.4417f  148.7687f
  cgtot     5.7066f    5.7066f  280.4622f  280.4622f  139.6602f
  cstot     7.4446f    7.4446f  330.0065f  330.0065f  196.2772f
  cbtot     4.9033f    4.9033f  277.3261f  277.3261f  242.5760f
  cgs       4.7092f    4.7092f  205.0018f  205.0018f   82.2131f
  cgd     719.2680a  719.2680a   35.2164f   35.2164f   37.5577f
```

```
**** voltage sources

subckt
element  0:vin       0:vbs       0:vbs1      0:vdd       0:vss
 volts     0.       525.0000m   521.0000m    1.8000      0.
 current   0.         0.          0.       -230.6590u  230.6590u
 power     0.         0.          0.        415.1863u    0.

    total voltage source power dissipation=  415.1863u       watts
```

MR	cdtot	cdb	cdg	cgtot	cgb	cgs	cstot	csb
	2.1661E-15	1.44683E-15	7.19268E-16	5.7066E-15	2.78132E-16	4.7092E-15	7.4446E-15	2.7354E-15
MX	cdtot	cdb	cdg	cgtot	cgb	cgs	cstot	csb
	1.35442E-13	1.00225E-13	3.52164E-14	2.80466E-13	4.0248E-14	2.05002E-13	3.30007E-13	1.25005E-13
MS	cdtot	cdb	cdg	cgtot	cgb	cgs	cstot	csb
	1.48769E-13	1.11211E-13	3.75577E-14	1.3966E-13	1.98894E-14	8.22131E-14	1.96277E-13	1.14064E-13

ro,r	ro,x	ro,tail	gm,r
129843.1495	21405.988	351.19758	1.96E-04
1/gmr//ror	gm,x	gms	1/gm,r
4910.0431	2.26E-03	0.0035854	5103.014555

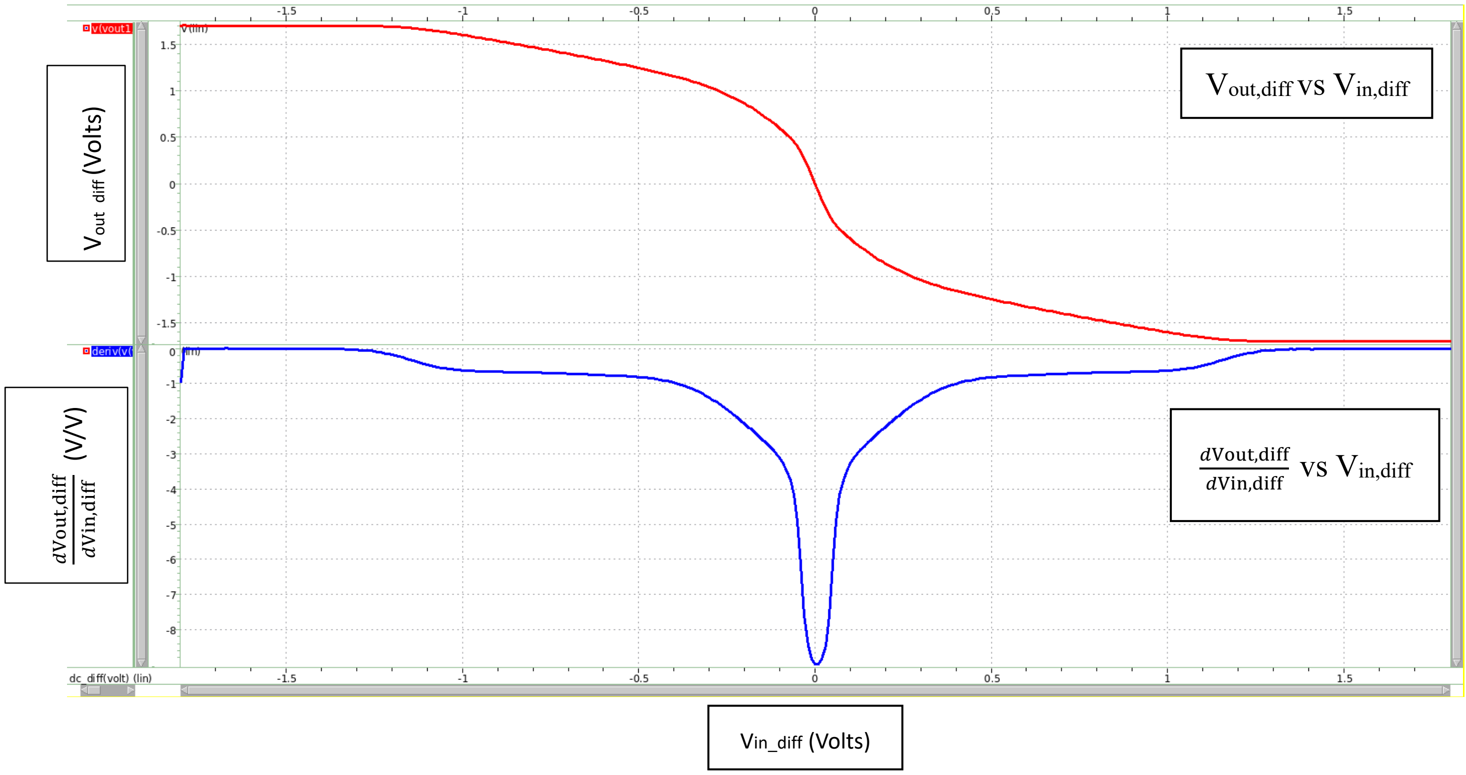
CL
2E-12

MR	W	L	m
	2µm	0.4µm	1
MX	W	L	m
	95µm	0.5µm	1
MS	W	L	m
	93µm	0.18µm	1

Where the unit of the capacitance is Farad (F), the unit of the resistance is Ohm (Ω), and the unit of transconductance is Siemens(S).

2. Differential Mode

Please run .DC then plots the differential output – differential input transfer curve. And compare the gain value from .tf with hand calculation using the small-signal parameters from question 1.




```
****     small-signal transfer characteristics

     v(vout1,vout2)/vin1                         =   -9.0207
     input resistance at              vin1       =  1.000e+20
     output resistance at v(vout1,vout2)         =    7.9898k
```

Hand Calculation-Differential Gain

ro,r	ro,x	ro,tail	gm,r
129843.1495	21405.988	351.19758	1.96E-04
1/gmr//ror	**gm,x**	**gms**	**1/gm,r**
4910.0431	2.26E-03	0.0035854	5103.014555

$$-g_{m,X} \times \left(\frac{1}{g_{mR}} // r_{o,R} // r_{o,X}\right) = 2.2582 + \times 10^{-3} \times \frac{-1}{(195.9626 \times 10^{-6} + 7.7016 \times 10^{-6} + 46.7159 \times 10^{-6})}$$

$$= -9.019087\ (V/V)$$

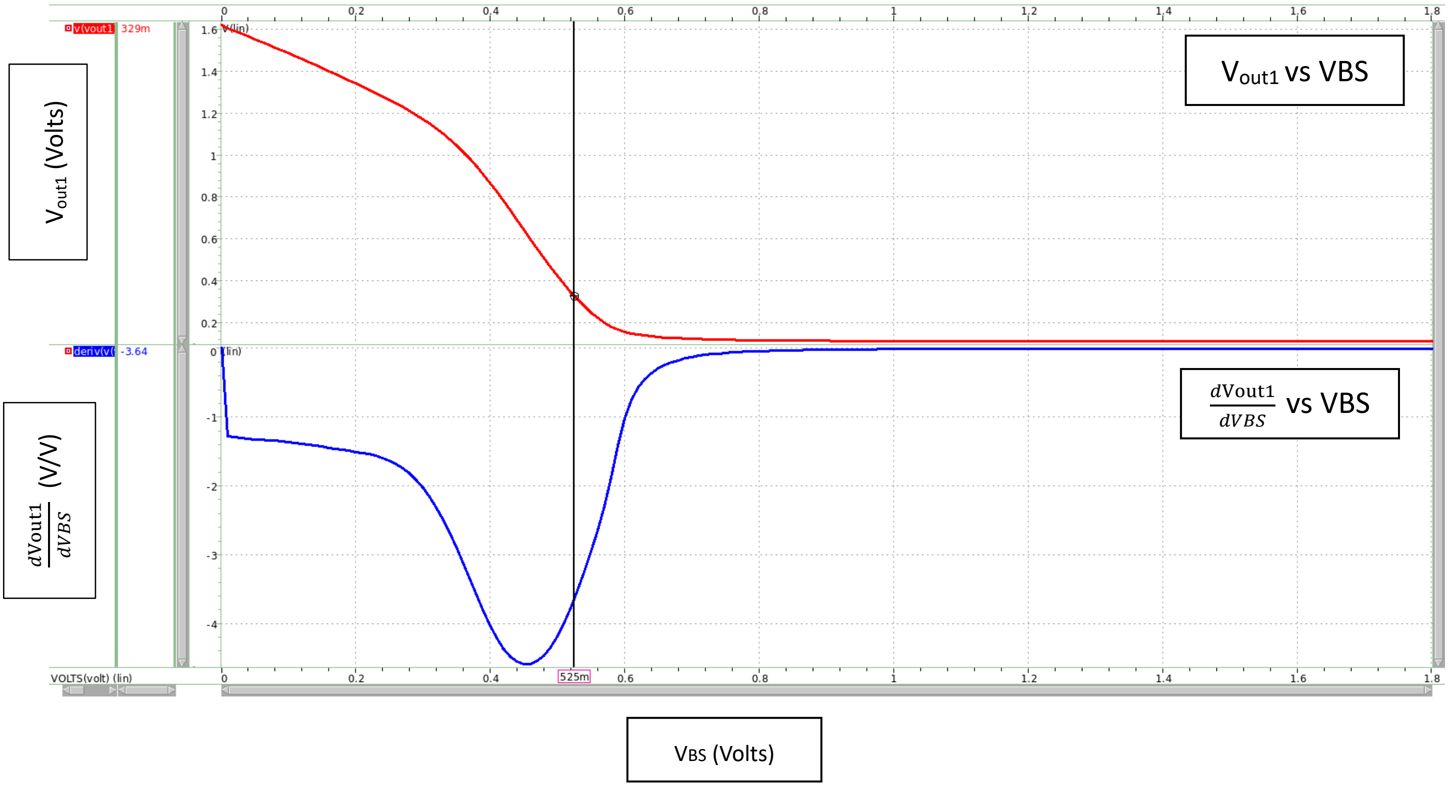
differential gain	hand calculate	simulation	error
	-9.0191	-9.0207	-0.02%

Comment:

The gain from hand calculation and simulation is almost the same.

3.Common Mode

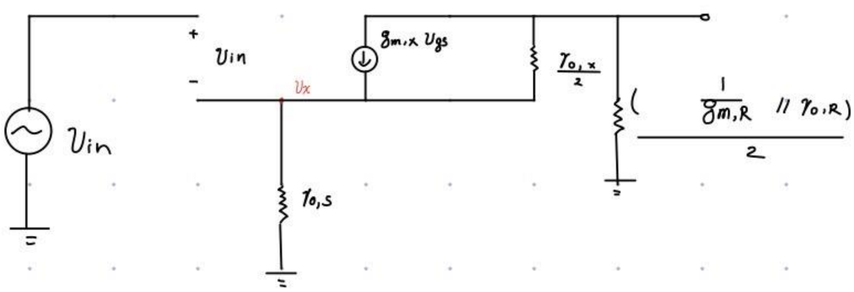
Please also run .DC to plot the common-mode output – common-mode input transfer curve. And compare the gain value from .tf with hand calculation using the small-signal parameters from question 1.




```
****     small-signal transfer characteristics

     v(vout1)/vbs                              =   -3.5215
     input resistance at          vbs          =  1.000e+20
     output resistance at v(vout1)             =    4.2743k
```

Hand calculation-Common mode gain

Common Source Degeneration (Folded Method)



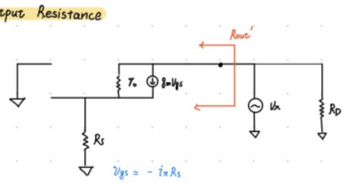
Let

$$\frac{(\frac{1}{g_{m,R}} // r_{o,R})}{2} = R_D$$

$$r_{o,s} = R_s$$

$$\frac{r_{o,x}}{2} = r_o$$

Output Resistance



$$v_x = r_o \cdot (i_x - g_m v_{gs}) + i_x R_s$$

$$= r_o \cdot (i_x + g_m i_x R_s) + i_x R_s$$

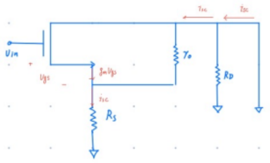
$$= i_x R_s (1 + g_m r_o) + i_x r_o$$

$$R_{out}' = \frac{v_x}{i_x} = r_o + (1 + g_m r_o) R_s$$

$$\Rightarrow R_{out} = R_{out}' \,/\!/\, R_D$$

$$R_{out} = \frac{[r_o + R_s + g_m r_o R_s]\, R_D}{[r_o + R_s + g_m r_o R_s + R_D]}$$

Total Conductance



$$\begin{cases} v_{in} = v_{gs} + i_{sc} R_s \\ 0 + (i_{sc} - g_m v_{gs})\, r_o + R_s i_{sc} = 0 \end{cases}$$

$$\Rightarrow i_{sc} r_o - g_m r_o (v_{in} - i_{sc} R_s) + i_{sc} R_s = 0$$

$$\Rightarrow i_{sc} [r_o + R_s (1 + g_m r_o)] = g_m r_o v_{in}$$

$$\Rightarrow G_m = \frac{i_{sc}}{v_{in}} = \frac{g_m \cdot r_o}{r_o + R_s (1 + g_m r_o)}$$

Gain

$$A_v = \frac{-g_m r_o}{r_o + R_s (1 + g_m r_o)} \times \frac{[r_o + R_s + g_m r_o R_s]\, R_D}{[r_o + R_s + g_m r_o R_s + R_D]}$$

$$= \frac{-g_m r_o R_D}{[r_o + R_D + R_s [1 + g_m r_o]]}$$

Substitute back $R_D = \frac{\frac{1}{g_{m,R}} \| r_{o,R}}{2}$ $R_S = r_{o,s}$ $r_o = \frac{r_{o,x}}{2}$ $g_m = 2 g_{m,x}$

ro,r	ro,x	ro,tail	gm,r
129843.1495	21405.988	351.19758	1.96E-04
1/gmr//ror	**gm,x**	**gms**	**1/gm,r**
4910.0431	2.26E-03	0.0035854	5103.014555

$$\text{Gain} = \frac{-2 g_{m,X} \times \frac{r_{o,X}}{2} \times \frac{\left(\frac{1}{g_{m,R}} \| r_{o,R}\right)}{2}}{\frac{r_{o,X}}{2} + \frac{\left(\frac{1}{g_{m,R}} \| r_{o,R}\right)}{2} + r_{o,s} \times \left(1 + 2 g_{m,x} \times \frac{r_{o,x}}{2}\right)} = \frac{-2 \times 2.2582 \times 10^{-3} \times \frac{21405.998}{2} \times \frac{4910.0431}{2}}{\frac{21405.998}{2} + \frac{4910.0431}{2} + 351.1976 \times \left(1 + 2 \times 2.2582 \times 10^{-3} \times \frac{21405.998}{2}\right)}$$

$$= -3.8927 (\text{V/V})$$

common mode gain	hand calculate	simulation	error
	-3.8927	-3.5215	10.54%

Comment:

The hand calculation is larger than simulation with 10% of the error rate. Comparing to others that uses the same method of folding half circuit but resulting with single digit error rate. My error rate might be larger because the design of my amplifier has larger effect caused by other small signal parameter, thus neglecting it causes the error to be larger, from previous experience since the source of the NMOS and the bulk has voltage difference, so it might come from the neglection of body conductance.

4. Frequency Response/Pole and Zero

The -3dB bandwidth of differential-mode has to be larger than 15MHz. Please simulate and plot the differential mode frequency response of this gain stage. And use .pz to simulate and mark the poles/zeros on this curve. Compare with hand calculation.

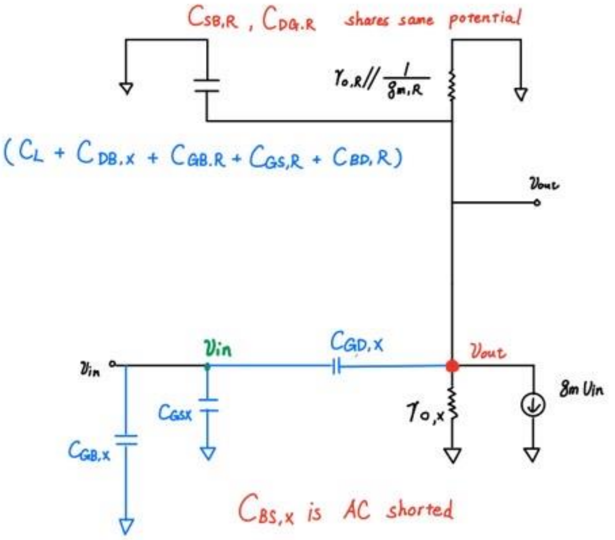
```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  19.1048
bw=  18.5532x
```

```
*************************************************************
  ******    pole/zero analysis

   input =  0:vin             output = v(vout1,vout2)

        poles (rad/sec)                   poles ( hertz)
real              imag            real              imag
-116.869x         0.              -18.6003x         0.

        zeros (rad/sec)                   zeros ( hertz)
real              imag            real              imag
59.2295g          0.              9.42666g          0.
```

Amplitude/Phase vs frequency

Frequency (Hz)

Hand Calculation



Use half circuit and view the tail current node as AC ground

Let $C_{out} = (C_L + C_{DB,x} + C_{GB,R} + C_{GS,R} + C_{BD,R})$

$$\begin{cases} V_{in} \cdot C_{GB,x} \cdot S + V_{in} \cdot C_{GS,x} \cdot S + (V_{in} - V_{out}) \cdot C_{GD,x} \cdot S = 0 \\[2ex] \dfrac{V_{out}}{r_{o,x}} + g_m V_{in} + \dfrac{V_{out}}{r_{o,R} /\!/ \frac{1}{g_{m,R}}} + V_{out} \cdot C_{out} \cdot S + (V_{out} - V_{in}) \cdot C_{GD,x} \cdot S = 0 \end{cases}$$

$$\frac{V_{out}}{r_{o,x}} + \frac{V_{out}}{r_{o,R} /\!/ \frac{1}{g_{m,R}}} + V_{out} \cdot (C_{out} \cdot s + C_{GD,x} \cdot s) = V_{in} \cdot C_{GD,x} \cdot s$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{C_{GD,x} \cdot S - g_{m,x}}{\dfrac{1}{r_{o,x} /\!/ r_{o,R} /\!/ \frac{1}{g_{m,R}}} + (C_{out} + C_{GD,x}) \cdot S}$$

Pole :

$$0 = \frac{1}{r_{o,x} /\!/ r_{o,R} /\!/ \frac{1}{g_{m,R}}} + (C_{out} + C_{GD,x}) \cdot s$$

$$S = \frac{-1}{(C_{GD,x} + C_{out})\left(r_{o,x} /\!/ r_{o,R} /\!/ \frac{1}{g_{mR}}\right)}$$

Zero.

$$C_{GD,x} \cdot S - g_{m,x} = 0$$

$$S = \frac{g_{m,x}}{C_{GD,x}}$$

Using the capacitance from. lis and the above calculation to get the pole and zero. Where the transfer function is $\frac{V_{out}(s)}{V_{in}(s)} = \frac{C_{gd,X} \times s - g_{m,X}}{\frac{1}{r_{o,X} \| r_{o,R} \| \frac{1}{g_{m,R}}} + (C_{out} + C_{gd,X}) \times s}$

calculated zero	simulation zero	error rate
1.02E+10	9.43E+09	8%
calculated pole	**simulation pole**	**error rate**
1.86048E+07	1.86003E+07	0.02%

The unit is in Hz

The calculated zero is 10.2 GHz and the calculated pole is 18.6048 MHz

The bandwidth can be approximated by the pole which is 18.6048 MHz

approximate BW	simulation BW	error rate
1.860E+07	1.8553E+07	0.28%

The unit is in Hz

If Using the transfer function to calculate the bandwidth

$$\left|\frac{V_{out}(j\omega)}{V_{in}(j\omega)}\right| = \sqrt{\frac{(C_{gd,X} \times \omega)^2 + g_{m,X}{}^2}{\left(\frac{1}{r_{o,X} \| r_{o,R} \| \frac{1}{g_{m,R}}}\right)^2 + ((C_{out} + C_{gd,X}) \times \omega)^2}}$$

利用 excel 的目標搜尋可以找到在幾 radian/s 的時候會讓 gain 到原先的$\frac{1}{\sqrt{2}}$，再來換算到 frequency。

radian/s	gain	-3db gain
116848063.1	9.0207	6.378598141
frequency	**分子**	**分母**
1.8597E+07	2.26E-03	0.000354016

The frequency unit is in Hz

calculated BW	simulation BW	error rate
1.8597E+07	1.8553E+07	0.24%

Calculated bandwidth is 18.597 MHz

Comment

The pole calculated has nearly the same result as simulation, and using the single pole as the bandwidth approximation is very accurate. But the zero has the same issue from last homework, acquiring from the transfer function has a larger value than simulation, and the numerator has similar structure which is a $C_{label} \times s - g_{m,label}$.

5. THD

Please input differential sinusoidal waveforms with 8mv linear range at 1MHz to estimate the harmonic distortion. Please use .four to simulate the THD performance. The THD has to be better than -60dB at 1MHz. Please print out the THD results of differential output and single-ended output. Discuss the result.

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=-560.0000
bw=    failed
fourier components of transient response v(vout1)
dc component =   328.2957m

harmonic frequency  fourier    normalized phase      normalized
no        (hz)      component  component  (deg)      phase (deg)
1           1.0000x   35.9866m    1.0000    86.9174     0.
2           2.0000x  114.9002u    3.1929m  157.9281    71.0107
3           3.0000x   14.6652u  407.5178u   78.6690    -8.2483
4           4.0000x  201.4890n    5.5990u  -15.8081  -102.7255
5           5.0000x   55.5238n    1.5429u -108.2703  -195.1877
6           6.0000x    1.1047n   30.6966n  155.0394    68.1220
7           7.0000x    5.5473n  154.1491n   29.2667   -57.6507
8           8.0000x   48.4259p    1.3457n   95.8343     8.9170
9           9.0000x    3.1285n   86.9350n  133.9147    46.9973

total harmonic distortion =   0.321876  percent
fourier components of transient response v(vout1,vout2)
dc component =   946.7365f

harmonic frequency  fourier    normalized phase      normalized
no        (hz)      component  component  (deg)      phase (deg)
1           1.0000x   71.9733m    1.0000    86.9174     0.
2           2.0000x    1.8948p   26.3263p  107.1976    20.2802
3           3.0000x   29.3304u  407.5178u   78.6690    -8.2483
4           4.0000x    1.8949p   26.3277p -145.5152  -232.4326
5           5.0000x  111.0476n    1.5429u -108.2703  -195.1877
6           6.0000x    1.8957p   26.3393p  -38.3014  -125.2187
7           7.0000x   11.0946n  154.1488n   29.2667   -57.6506
8           8.0000x    1.8978p   26.3679p   68.9478   -17.9696
9           9.0000x    6.2570n   86.9348n  133.9147    46.9973

total harmonic distortion =   0.0407521  percent
```

Comment:

The harmonic distortion of the single output is diminished after using differential pair, where the component of the fundamental frequency is doubled from 35.9866 mV to 71.9733 mV.

The dc component is diminished when using differential pair where the DC component drops from 328.2957 mV to 946.7365 fV which is close to zero.

If the circuit is linear, then the output of the input sine wave will be only amplified and have a 180-degree phase shift and amplification due to its common source structure, but since it has nonlinearity, so the periodic wave after the amplifier will have signal components of only harmonic frequencies of the fundamental frequencies, since it's still periodic.

For a linear common source structure amplifier: $A_C \sin(\omega t) \rightarrow kA_C \sin(\omega t + \pi)$

For a nonlinear common source structure amplifier: Input : $A_C \sin(\omega t) \rightarrow$ *Output* : $a_1 kA_C \sin(\omega t + \pi) + a_2 k^2 {A_C}^2 \sin^2(\omega t + \pi) + a_3 k^3 {A_C}^3 \sin^3(\omega t + \pi) + \dots\dots$ where a_1 is usually way larger than a_n , $n \neq 1$.

Then the output can be rewritten as

$$\frac{1}{2}k^2a_2 + (a_1k + \frac{3k^2a_3}{4})A_C\sin(\omega t+\pi) + \frac{-a_2k^2{A_C}^2}{2}\cos(2(\omega t+\pi)) + \frac{-a_3k^3{A_C}^3}{4}\sin(3(\omega t+\pi)) + \dots\dots$$

Meanwhile the other side of differential output demonstrate the same thing where the linear amplification looks like $\mathit{Input}:\ A_C\sin(\omega t+\pi) \rightarrow \mathit{Output}:\ kA_C\sin(\omega t)$

So, the nonlinear output should look like

$$\frac{1}{2}k^2a_2 + (a_1k + \frac{3k^2a_3}{4})A_C\sin(\omega t) + \frac{-a_2k^2{A_C}^2}{2}\cos(2\omega t) + \frac{-a_3k^3{A_C}^3}{4}\sin(3\omega t) + \dots\dots$$

we can observe that the even harmonic frequency components are in phase for the two-side output and the odd harmonic frequency components are out of phase for the two-side output, so after the differential output, the even harmonic component are canceled by each other and the fundamental frequency and the odd harmonic frequency are doubled, thus the distortion is strongly reduced because the fundamental component is doubled.

THD calculation (differential output)

The calculation is using the square root value of the sums of square value of the nth harmonic components divided by the fundamental frequency component in volts, indicating a degree of how the input periodic signal is distorted after the nonlinear system.

	1st harmonic	2nd harmonic	3rd harmonic	4th harmonic	5th harmonic	6th harmonic	7th harmonic	8th harmonic	9th harmonic
component	0.0719733	1.8947E-12	2.93304E-05	1.8951E-12	1.11048E-07	1.8967E-12	1.10946E-08	1.8981E-12	6.257E-09
square value	0.0719733	3.58989E-24	8.60272E-10	3.5914E-24	1.23316E-14	3.59747E-24	1.2309E-16	3.60278E-24	3.915E-17

$$THD = \frac{\sqrt{{V_2}^2+{V_3}^2+{V_4}^2+{V_5}^2+{V_6}^2+{V_7}^2+{V_8}^2+{V_9}^2}}{V_1} = 0.0407521\%\ \text{(V/V)}$$
$$= 20\log(0.00047521) = -67.79700\ (dB)$$

Performance Table

Working Item	Specification	Simulation	Calculation
Tail Current	(mA)	0.230659	
Differential Gain	> 9(V/V)	9.0207	9.0191
Input common mode	VBS(V)	0.525	
Tail Current Bias	VBS1(V)	0.521	
Common-mode gain	(V/V)	3.5215	3.8927
Mx size	W/L/m	95μm/0.5μm/m=1	
Ms size	W/L/m	93μm/0.18μm/m=1	
MR size	W/L/m	2μm/0.4μm/m=1	
Bandwidth	>15MHz	18.5532 MHz	18.597 MHz
THD	-60dB	-67.797 dB	-67.797 dB