EE3235 Analog Integrated Circuit Analysis and Design I

Homework 5
Feedback

Due date: 2021.12.08 (Wed.) 13:20 (upload to eeclass system)

Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

(a) (b)

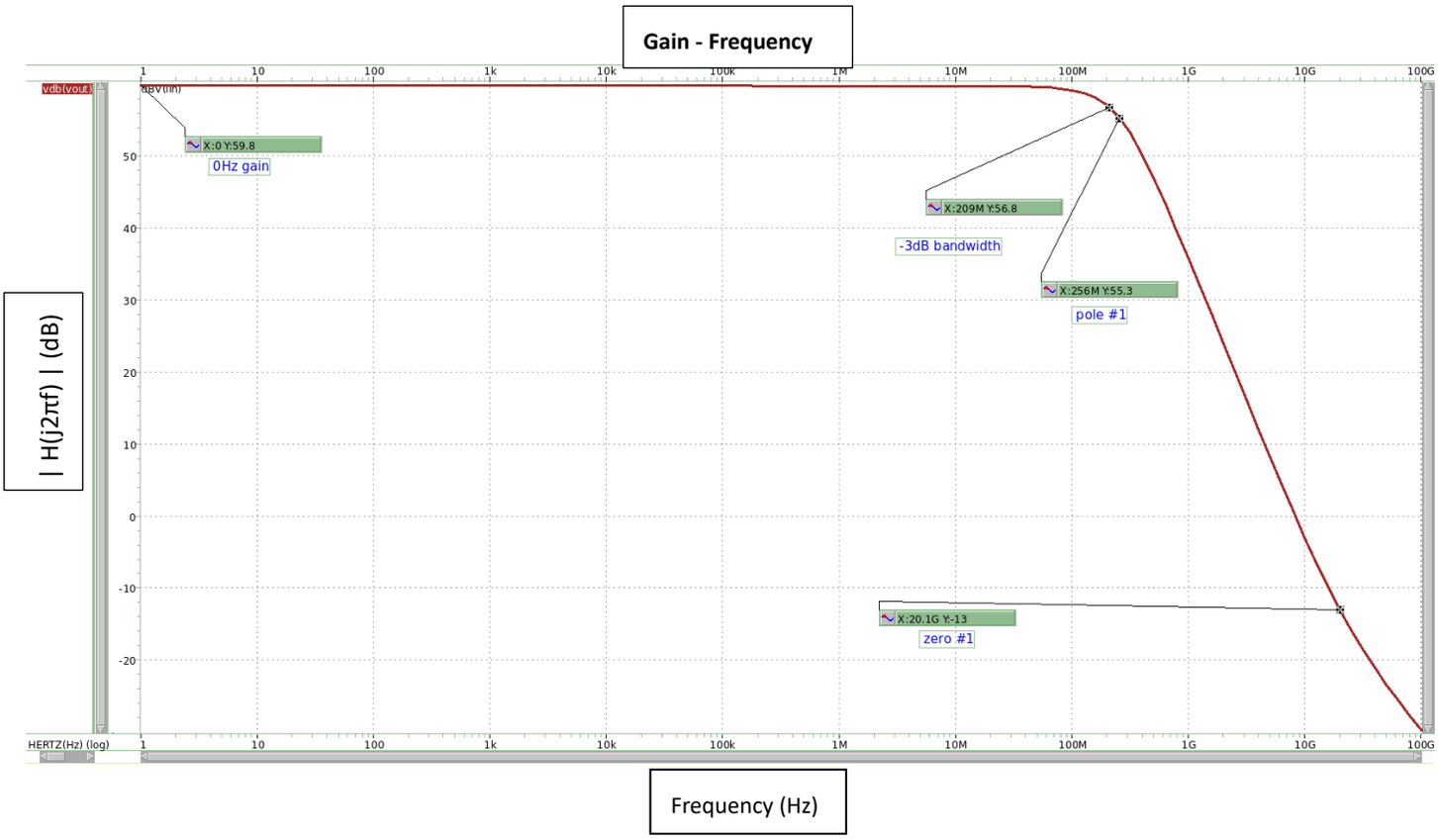
```
****      small-signal transfer characteristics

     v(vout)/iin                               = -975.0498
     input resistance at                iin    =   24.4610
     output resistance at v(vout)              =   10.0766
```

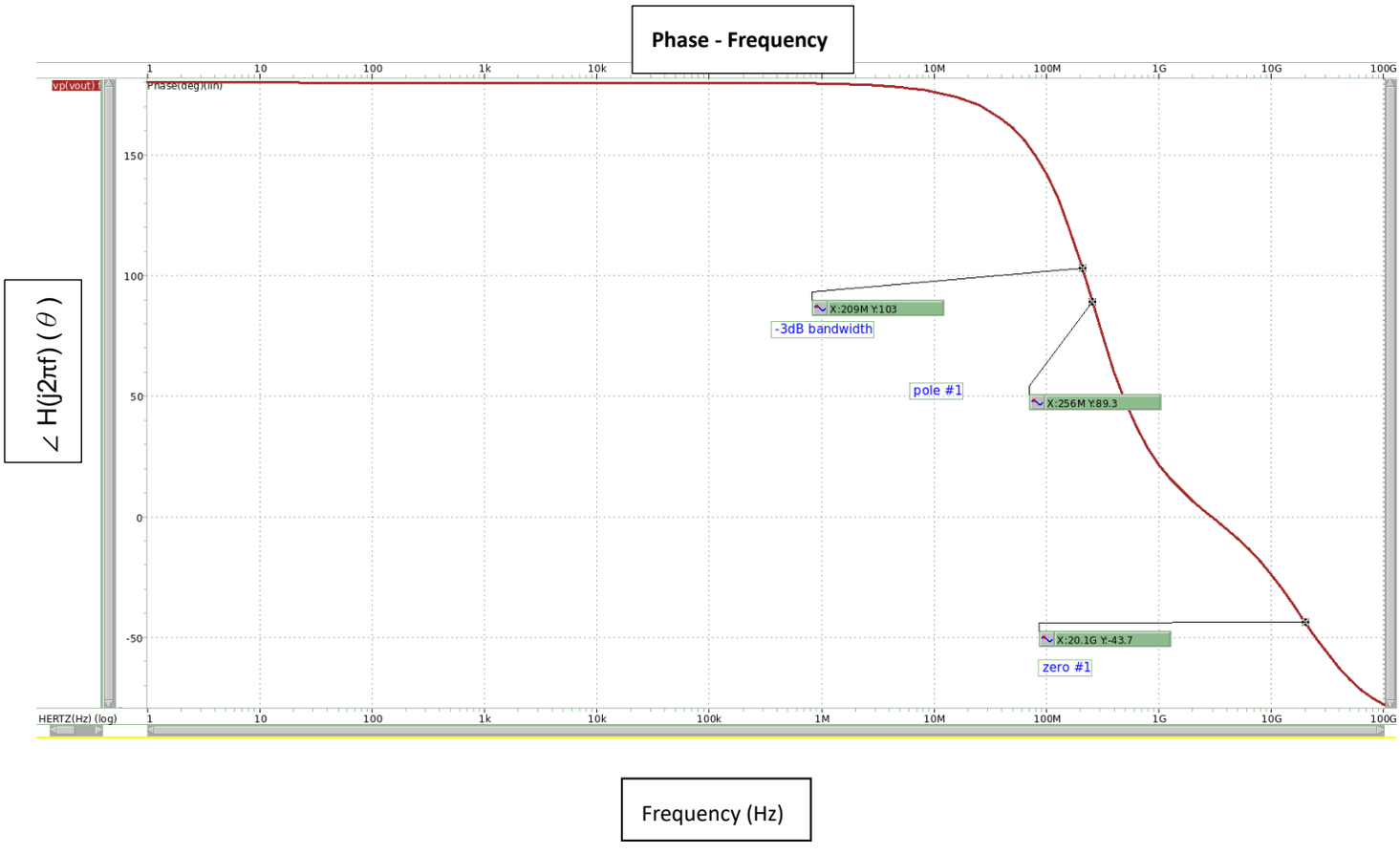
```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  59.7805
bw= 209.4107x
ugb=   8.3391g
```

(d) (swap order of (c) and (d))

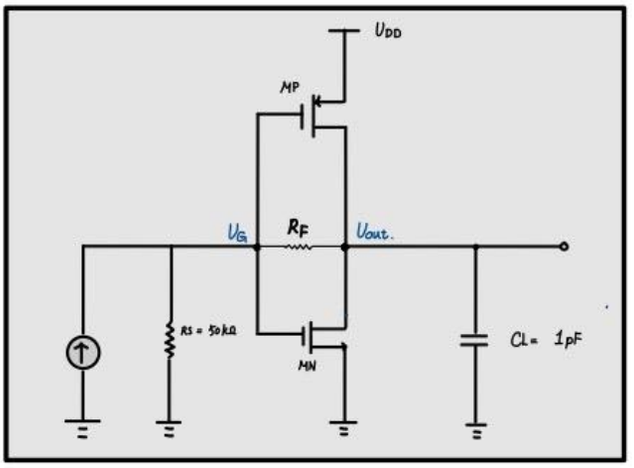
```
The 1th iter
>temperature = 25

     poles (rad/sec)                poles ( hertz)

real           imag           real           imag

-1.34252g          880.731x          -213.669x          140.173x
-1.34252g          -880.731x          -213.669x          -140.173x


     zeros (rad/sec)                zeros ( hertz)

real           imag           real           imag

126.280g           0.          20.0981g           0.
```

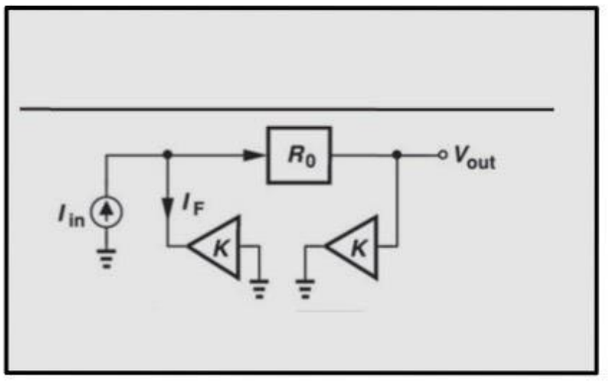
Pole: the magnitude, which is $\sqrt{-213.669^2 + 140.173^2}$ = 255.544 MHz

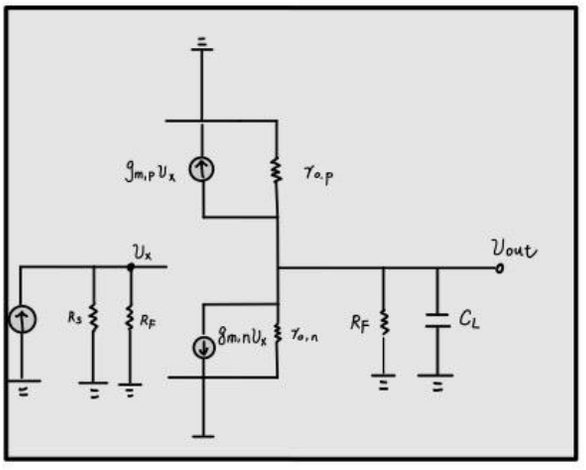


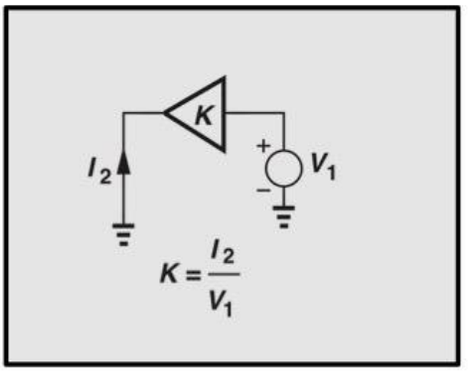


(g)-1 (duplicate this part (g) to front for later parameter discussion)









$v_g = i_{in}(R_S \parallel R_F)$ $\quad g_{m,n}v_g + g_{m,p}v_g + \frac{v_{out}}{(R_F \parallel r_{o,p} \parallel r_{o,n})} = 0$

$i_{in}(g_{m,n} + g_{m,p})(R_S \parallel R_F) + \frac{v_{out}}{(R_F \parallel r_{o,p} \parallel r_{on})} = 0$

$\Rightarrow \frac{v_{out}}{(R_F \parallel r_{o,n} \parallel r_{o,p})} = -i_{in}(g_{m,n} + g_{m,p})(R_S \parallel R_F)$

$\Rightarrow \frac{v_{out}}{i_{in}} = -(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{o,p})$

$K = \frac{v_{out}}{i_{RF}} = \frac{v_{out}}{-\left(\frac{v_{out}}{R_F}\right)} = \frac{1}{-R_F}$

The close-loop gain is $\frac{R_o}{1 + KR_o} = \frac{-(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{op})}{1 + \frac{1}{R_F}(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{o,p})}$

(c)

```
**** mosfets

subckt
element  0:mp          0:mn
model    0:p_18.1      0:n_18.1
region   Saturation    Saturation
 id       -12.8897m     12.9223m
 ibs        1.1869a     -1.9629a
 ibd       66.1582f    -31.8145f
 vgs     -932.7461m    867.2539m
 vds     -965.4010m    834.5990m
 vbs        0.            0.
 vth     -498.7165m    366.5620m
 vdsat   -385.9248m    407.4407m
 vod     -434.0296m    500.6919m
 beta     149.0873m    123.4714m
 gam eff  557.0845m    507.4474m
 gm        51.7103m     48.0043m
 gds      713.1158u    763.1698u
 gmb       16.3836m      9.0428m
 cdtot      1.6894p    686.3421f
 cgtot      7.2014p      4.6033p
 cstot      8.6466p      5.0704p
 cbtot      4.5739p      2.1253p
 cgs        6.2411p      4.1219p
 cgd      557.8335f    187.2105f
```

Closed-loop gain:

$$\frac{R_0}{1+KR_0} = \frac{-(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})}$$

$$= \frac{-(51.7103\times10^{-3}+48.0043\times10^{-3})\times 980.3922\times 403.8306}{1+\frac{1}{1000}\times(51.7103\times10^{-3}+48.0043\times10^{-3})\times 980.3922\times 403.8306} = -975.2954\ (V/A)$$

Closed-loop input resistance

$$\frac{opened-loop\ input\ resistance}{1+KR_0} = \frac{(R_S \,//\, R_F)}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})} = 24.2202\ \Omega$$

Closed-loop output resistance

$$\frac{opened-loop\ output\ resistance}{1+KR_0} = \frac{(R_F \,//\, r_{o,n} \,//\, r_{o,p})}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})} = 9.9765\ \Omega$$

Calculated	.tf	relative error rate
closed loop gain (V/A)	**closed loop gain(V/A)**	
-975.2954	-975.0498	0.0252%
closed loop input resistance (Ω)	**closed loop input resistance (Ω)**	
24.2202	24.4610	-0.9843%
closed loop output resistance (Ω)	**closed loop output resistance (Ω)**	
9.9765	10.0766	-0.9935%

Comment:

The three parameters acquired from hand calculation and spice simulation are almost identical, the gain hand calculated is slightly larger, and the input/output resistance are slightly smaller.

(e)

This time I use direct analysis with counting every capacitance and resistance that involves with the whole circuit. The following value for capacitance is in Farad and for resistance is Ohm.

gm	51.7103m	48.0043m
gds	713.1158u	763.1698u
gmb	16.3836m	9.0428m
cdtot	1.6894p	686.3421f
cgtot	7.2014p	4.6033p
cstot	8.6466p	5.0704p
cbtot	4.5739p	2.1253p
cgs	6.2411p	4.1219p
cgd	557.8335f	187.2105f

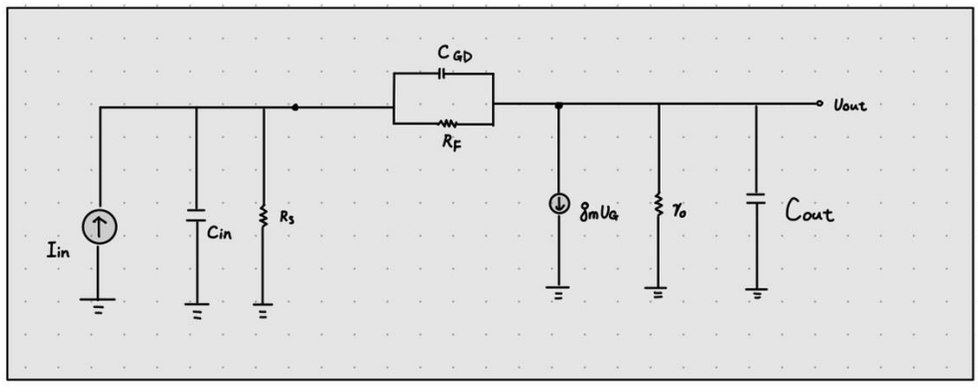
cgtot p	cgtot n	cgtot,total	cgd p	cgd n	cgd total	cgs+cgb
7.2014E-12	4.6033E-12	1.18047E-11	5.57834E-13	1.87211E-13	7.45044E-13	1.10597E-11

CL	cdtot,n	cdtot,p	cdb
1E-12	1.6894E-12	6.86342E-13	1.6307E-12

Ron	rop	ron//rop
1402.296794	1310.324387	**677.3757056**
gm,n	**gm,p**	**gm,total**
0.0517103	0.0480043	0.0997146
Rf	Rs	
1000	50000	

For the below direct analysis, some procedure helps for neat calculation, such as two same kind of parasitic capacitance are combined to one due to symmetry and some renamed capacitor like below.

$$C_{in} = C_{gs,total} + C_{gb,total}$$
$$C_{\text{out}} = C_{db,total} + C_{L,total}$$
$$r_o = r_{o,n} \,//\, r_{o,p}$$
$$g_m = g_{m,n} + g_{m,p}$$



$$I_{in} = \frac{V_G}{R_S \,//\, \frac{1}{C_{in}\,s}} + \frac{V_G - V_{out}}{R_F \,//\, \frac{1}{C_{GD}\cdot s}}$$

$$\frac{V_{out}}{r_o \,//\, \frac{1}{C_{out}\,s}} + \frac{V_{out} - V_G}{R_F \,//\, \frac{1}{C_{GD}\cdot s}} + g_m V_G = 0$$

$$V_{out}\left(\frac{1}{r_o \,//\, \frac{1}{C_{out}\cdot s}} + \frac{1}{R_F \,//\, \frac{1}{C_{GD}\cdot s}}\right) = \left(\frac{1}{R_F \,//\, \frac{1}{C_{GD}\cdot s}} - g_m\right) V_G$$

$$I_{in} = \frac{1}{\left(R_S // \frac{1}{C_{in}\cdot s}\right)} \times \frac{U_{out}\left(\frac{1}{r_o // \frac{1}{C_{out}\cdot s}} + \frac{1}{R_F // \frac{1}{C_{GD}\cdot s}}\right)}{\left(\frac{1}{R_F // \frac{1}{C_{GD}\cdot s}} - g_m\right)} + \frac{U_{out}}{\left(R_F // \frac{1}{C_{GD}\cdot s}\right)} \times \left(\frac{\left(\frac{1}{r_o // \frac{1}{C_{out}\cdot s}} + \frac{1}{R_F // \frac{1}{C_{GD}\cdot s}}\right)}{\left(\frac{1}{R_F // \frac{1}{C_{GD}\cdot s}} - g_m\right)} - 1 \right)$$

$$\frac{U_{out}}{I_{in}} = \frac{1}{\frac{1}{R_S // \frac{1}{C_{in}\cdot s}}\left(\frac{\left(\frac{1}{r_o // \frac{1}{C_{out}\cdot s}} + \frac{1}{R_F // \frac{1}{C_{GD}\cdot s}}\right)}{\left(\frac{1}{R_F // \frac{1}{C_{GD}\cdot s}} - g_m\right)}\right) + \left(\frac{\frac{1}{r_o // \frac{1}{C_{out}\cdot s}} + \frac{1}{R_F // \frac{1}{C_{GD}\cdot s}}}{\left(\frac{1}{R_F // \frac{1}{C_{GD}\cdot s}} - g_m\right)} - 1\right)\frac{1}{\left(R_F // \frac{1}{C_{GD}\cdot s}\right)}}$$

let $\quad a = \frac{1}{r_o // \frac{1}{C_{out}\cdot s}} \quad b = \frac{1}{R_F // \frac{1}{C_{GD}\cdot s}}, \quad c = \frac{1}{R_S // \frac{1}{C_{in}\cdot s}}$

$$\frac{U_{out}}{I_{in}} = \frac{1}{c\left(\frac{a+b}{b-g_m}\right) + b\left(\frac{a+b}{b-g_m} - 1\right)}$$

$$= \frac{b-g_m}{c(a+b) + b\left[(a+b) - b + g_m\right]}$$

$$= \frac{b-g_m}{c(a+b) + b\left[a+g_m\right]}$$

$$= \frac{\frac{1 + R_F C_{GD}\cdot s}{R_F} - g_m}{\left(\frac{1}{R_S} + C_{in}\cdot s\right)\left(\frac{1}{r_o} + C_{out}\cdot s + \frac{1}{R_F} + C_{DG}\cdot s\right) + \left(\frac{1}{R_F} + C_{GD}\cdot s\right)\left(\frac{1}{r_o} + C_{out}\cdot s + g_m\right)}$$

S^2 項：$C_{in}\cdot C_{out}$, $C_{in}C_{GD}$, $C_{GD}\cdot C_{out}$

S 項：$\frac{C_{in}}{r_o}$, $\frac{C_{in}}{R_F}$, $\frac{C_{DG}}{R_S}$, $\frac{C_{out}}{R_S}$, $\frac{C_{GD}}{r_o}$, $\frac{C_{out}}{R_F}$, $g_m\cdot C_{GD}$

常數項：$\frac{1}{R_S r_o}$, $\frac{1}{R_S\cdot R_F}$, $\frac{1}{R_F, r_o}$, $\frac{g_m}{R_F}$

s平方項	cin*cout	cin*cgd	cgd*cout				
	2.90946E-23	8.23993E-24	1.95999E-24				
s項	cin/ro	cin/Rf	cgd/Rs	cout/Rs	cgd/ro	cout/Rf	gm*cgd
	1.63272E-14	1.10597E-14	1.49009E-17	5.2614E-17	1.0999E-15	2.6307E-15	7.42918E-14
常數項	1/(Rs*ro)	1/(Rf*ro)	gm/Rf	1/(Rs*Rf)			
	2.95257E-08	1.47629E-06	9.97146E-05	2.00E-08			

For calculation of the poles. use $s = \frac{-b \pm \sqrt{b^2-4ac}}{2a}$ to calculate for direct pole. In this case $\sqrt{b^2-4ac}$ is smaller than 0, so there are two complex conjugate poles.

a		2a		b^2-4ac
3.92945E-23		7.85891E-23		-4.78744E-27
b		"-b/2a"		sqrt(|b^2-4ac|)/2a
1.05477E-13		-1.34E+09		8.80E+08
c		in frequency		in frequency
1.01E-04		-2.1361E+08		1.4012E+08

The hand calculate poles are $-213.61 \times 10^6 \pm j140.12 \times 10^6\ (Hz)$

For calculation of the zero, this comes from the numerator $\frac{1+R_F \times C_{GD} \times s}{R_F} - g_m$, make the numerator 0 to acquire the pole, so $f = \frac{g_m R_F - 1}{R_F C_{GD} \times 2\pi} = 21.087 \times 10^9\ (\text{Hz})$

ZERO	POLE REAL	POLE IMAG
2.1087E+10	-2.136066E+08	1.4012E+08

```
The 1th iter
>temperature = 25

      poles (rad/sec)                poles ( hertz)

real            imag           real            imag

-1.34252g          880.731x          -213.669x          140.173x
-1.34252g          -880.731x          -213.669x          -140.173x


      zeros (rad/sec)                zeros ( hertz)

real            imag           real            imag

126.280g          0.          20.0981g          0.
```

Comment:

The calculated are nearly identical to the value of simulation in terms of number of order and rough number.

The error rate of the real part of pole is $\frac{-213.6066-(-213.669)}{-213.669} = 0.0292\%$

The error rate of the imaginary part of pole is $\frac{140.12-140.173}{140.173} = 0.0378\%$

The error rate of the zero is $\frac{21.087-20.0981}{20.0981} = 4.92\%$, which has significant larger error rate comparing to the poles, from transfer function, the error might come from mere approximation of transconductance without considering body conductance.

For bandwidth calculation, since I acquired the transfer function from the direct analysis, so I can find frequency when the gain is in $\frac{1}{\sqrt{2}}$ of the original gain.

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{\frac{1+R_F \times C_{gd,total} \times s}{R_F} - g_m}{as^2+bs+c} \quad \text{where } a = 3.92945 \times 10^{-23}, b = 1.05477 \times 10^{-13}, c = 1.01 \times 10^{-4}$$

$$\text{Then} \quad \left|\frac{V_{out}(j\omega)}{I_{in}(j\omega)}\right| = \frac{\sqrt{(-g_m+\frac{1}{R_F})^2+(C_{gd,total} \times \omega)^2}}{\sqrt{(c-\omega^2 a)^2+(b\omega)^2}}$$

ω	(-gm+1/RF)^2	(Cgd*S)^2	(c-s^2*a)^2	(bs)^2
1321874268	0.009744572	9.69938E-07	1.06139E-09	1.94399E-08
3dB frequency	**分子**	**分母**	**Gain at 0Hz**	**GAIN**
210382823.9	0.098719513	0.000143183	975.0498	689.4654562

利用 Excel 的目標搜尋將目標值 Gain 設定在 $\frac{Gain\ at\ 0\ Hz}{\sqrt{2}} = \frac{975.0498}{\sqrt{2}} = 689.4643\ (V/A)$

求得 $\omega = 1321874268\ (\text{rad/s})$ 而可以得到 $f_{-3dB} = 210.382 \times 10^6\ (\text{Hz})$

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  59.7805
bw= 209.4107x
ugb=   8.3391g
```

Comment:

The result of calculating bandwidth is almost similar to simulation in terms of number of order and the rough value, where the error rate is $\frac{210.382-209.4107}{209.4107} = 0.4638\%$

(f)

Improvement of FoM is mentioned in part (g)

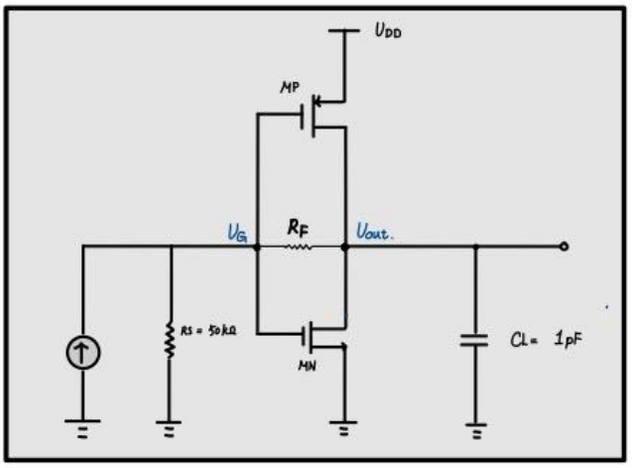
```
**** voltage sources

subckt
element  0:vdd      0:vss
 volts      1.8000     0.
 current  -12.8897m  352.0492f
 power     23.2014m    0.

    total voltage source power dissipation=   23.2014m       watts


**** current sources

subckt
element  0:iin
 volts   -867.2539m
 current   50.0000u
 power     43.3627u


    total current source power dissipation=  43.3627u       watts
```

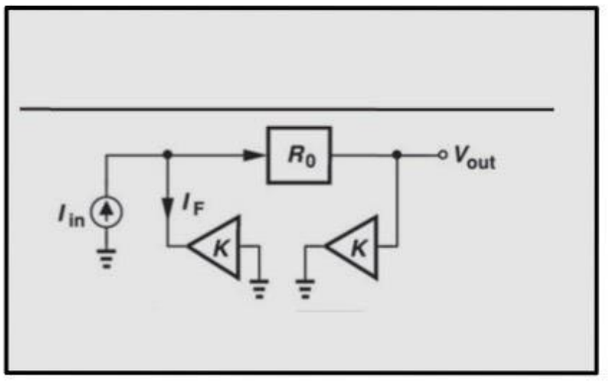
```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  59.7805
bw= 209.4107x
ugb=   8.3391g
```

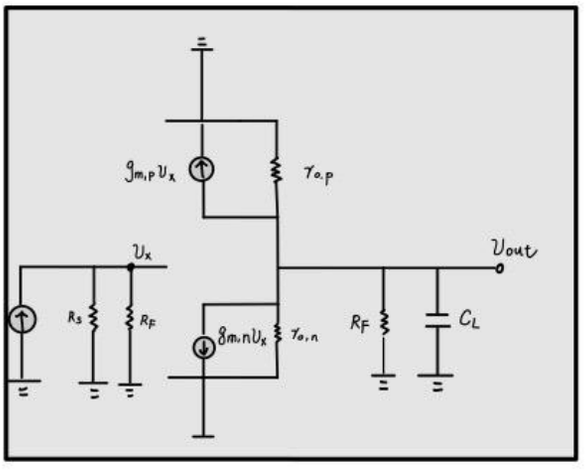
Bandwidth (MHz)	current (µA)
209.4107	12939.7

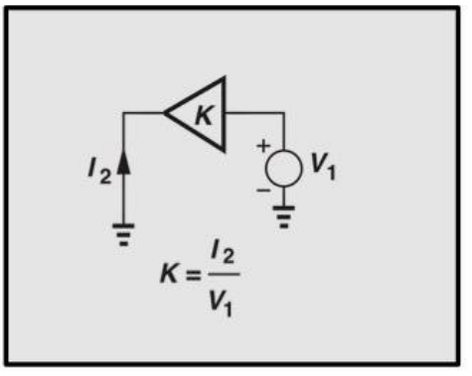
FoM (MHz/µA)	#2 / #1	0.0162

(g)-1 (duplicate this part (g) to front for later parameter discussion)









$v_g = i_{in}(R_S \parallel R_F)$ $\quad g_{m,n}v_g + g_{m,p}v_g + \frac{v_{out}}{(R_F \parallel r_{o,p} \parallel r_{o,n})} = 0$

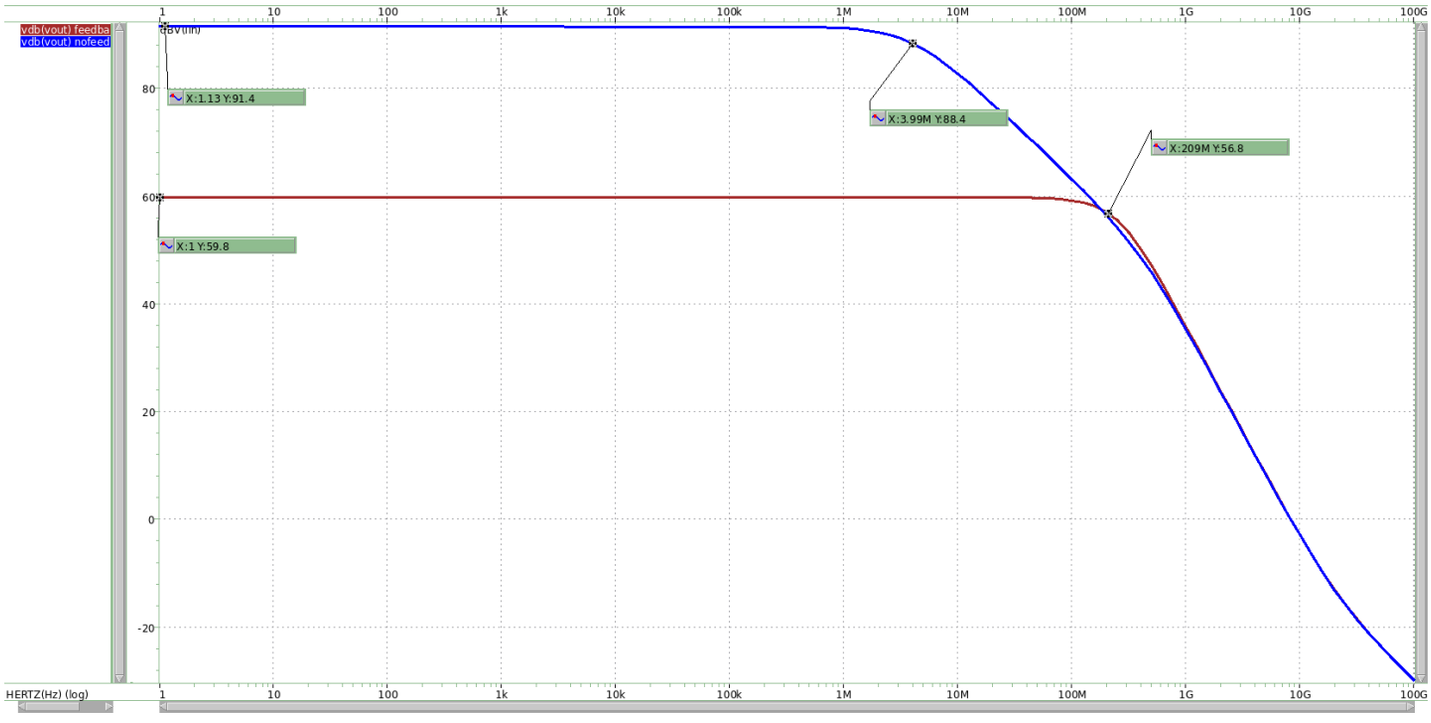
$i_{in}(g_{m,n} + g_{m,p})(R_S \parallel R_F) + \frac{v_{out}}{(R_F \parallel r_{o,p} \parallel r_{on})} = 0$

$\Rightarrow \frac{v_{out}}{(R_F \parallel r_{o,n} \parallel r_{o,p})} = -i_{in}(g_{m,n} + g_{m,p})(R_S \parallel R_F)$

$\Rightarrow \frac{v_{out}}{i_{in}} = -(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{o,p})$

$K = \frac{v_{out}}{i_{RF}} = \frac{v_{out}}{-\left(\frac{v_{out}}{R_F}\right)} = \frac{1}{-R_F}$

The close-loop gain is $\frac{R_o}{1 + KR_o} = \frac{-(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{op})}{1 + \frac{1}{R_F}(g_{m,n} + g_{m,p})(R_S \parallel R_F)(R_F \parallel r_{o,n} \parallel r_{o,p})}$




```
****     small-signal transfer characteristics

     v(vout)/iin                           = -975.0498
     input resistance at             iin   =   24.4610
     output resistance at v(vout)          =   10.0766
```

bw= 209.4107x

```
****     small-signal transfer characteristics

     v(vout)/iin                           =  -39.2943k
     input resistance at             iin   =  980.3922
     output resistance at v(vout)          =  402.0620
```

bw= 3.7953x

The blue curve is when feedback network is disconnected, and the red curve is with feedback network. The original gain is suppressed after the feedback network is connected, and the bandwidth is widened after feedback network is connected.

The current supplied in the non-feedback network amplifier is 875μm but the when the feedback forward is connected, the supplied current is only 50μm.

0.	24.5429	10.0799	-974.9662
5.0000u	24.5273	10.0795	-974.9821
10.0000u	24.5133	10.0791	-974.9964
15.0000u	24.5009	10.0788	-975.0090
20.0000u	24.4902	10.0784	-975.0200
25.0000u	24.4810	10.0781	-975.0293
30.0000u	24.4736	10.0778	-975.0369
35.0000u	24.4678	10.0775	-975.0428
40.0000u	24.4638	10.0772	-975.0469
45.0000u	24.4615	10.0769	-975.0493
50.0000u	24.4610	10.0766	-975.0498

In fact, given 0 input DC current can almost hit the SPEC gain value. This indicates that with the gain stage settled and feedback network connected, the gate voltage and the output voltage are fixed at the stage providing the similar gain with or without dc current value.

(g)-2

Working Item	Specification	Simulation result	Hand Calculation
VDD	1.8 V		
Current (μA)	(μA) #1	12939.7	
Transimpedance gain (KΩ)	> 0.975KΩ	-0.9750498	-0.975295372
core amp size (W/LN) (W/LP)		(29 μm/1.3 μm) , (86μm/0.7 μm)	
Bandwidth (-3db) (MHz)	> 170 MHz #2	209.4107 MHz	210.382 MHz
Closed-loop poles/zeros		'- 213.669± j140.173 MHz, 20.0981GHz	'- 213.606 ± j140.12Mhz, 21.087 GHz
Closed-loop input impedance		24.4610	24.2202
Closed-loop output impedance		10.0766	9.9765
FoM (MHz/μA)	#2 / #1	0.016	
		0.0162	

多取一位小數點
不知道會不會做排序
分毫必爭

Design flow:

This configuration has nonideal I/O impedance which mainly due to the low shunt-resistor, so that the feedback loads the forward amplifier. To analyze the circuit, the circuit has to be break down. Where the breakdown process is on part (g)-1.

From formulas

$$\text{Closed-loop gain } \frac{R_0}{1+KR_0} = \frac{-(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})},$$

$$\text{Closed-loop input resistance } \frac{opened{-}loop\ input\ resistance}{1+KR_0} = \frac{(R_S \,//\, R_F)}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})}$$

$$\text{Closed-loop output resistance } \frac{opened{-}loop\ output\ resistance}{1+KR_0} = \frac{(R_F \,//\, r_{o,n} \,//\, r_{o,p})}{1+\frac{1}{R_F}(g_{m,n}+g_{m,p})(R_S \,//\, R_F)(R_F \,//\, r_{o,n} \,//\, r_{o,p})}$$

Observing the term that both the numerator and denominator shared is $(R_F \,//\, r_{o,n} \,//\, r_{o,p})$ and $(g_{m,n} + g_{m,p})$. But the first term is fixed to around 1000 Ω for high r_o since the shunt resistor has small resistance comparing to both r_o, so if both g_m can grow as large as possible, the 1 in the denominator of the gain can be neglected, then the gain can eventually approach close to $\frac{1}{K} = 1000 > 975$. The input/output impedance of a Voltage-Current amplifier should ideally have both low input and output impedance, so increasing both g_m helps reaching the goal, since both impedances decreases when g_m is increased

Next, from formula

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

My approach is to let $g_{ds}, g_m, beta$ to stay close so that both can change in parallel. Since the mobility of holes and electron has difference, so some ratio test had been tried to find how beta changes. Also, experience from previous homework is that for this PMOS and NMOS connection stage, the W/L ratio should be larger for PMOS than NMOS for both MOS to work in saturation region. I found out that when $\frac{W}{L_P} : \frac{W}{L_N} = 5.5\sim6$ for $L_P = 0.7\mu m\ and\ L_N = 1.3\mu$, the beta value and g_{ds}, g_m are similar for both MOS. I set the PMOS channel length at 0.7μm and NMOS channel length at 1.3 μm because the PMOS width

had larger room to grow but meanwhile avoiding the $0.18\mu m \sim 0.5\mu m$ region because of possible short channel effect.

I first start from $\frac{W}{L_P} = \frac{9\mu m}{0.7\mu m}$ and $\frac{W}{L_N} = \frac{3\mu m}{1.3\mu m}$ and m = 1

But lot of problem occurred, the first is that for large g_m, large channel width has to be implemented, but there is a limit in this manufacturing process, so I seek help from classmates that have taken the courses of VLSI, they suggest that m should be increased since it can be seen equivalence as multiple MOS parallel but with same bias control and substrate. So, I increase the m and width for reaching the spec.

And the second thing is r_0, this value decreases to near to R_F as g_m increases. So, the best case is that this value should stay the same for both PMOS and NMOS, so that the parallel resistance value can reaches its maximum.

When reaching the expected gain, I calculated the transfer function through direct analysis. Then with knowing all the parasitic capacitance, I can calculate the bandwidth. The pole and zero can be calculated by the formula $\frac{-b \pm \sqrt{b^2-4ac}}{2a}$ mentioned in the previous part. By observation, the pole's magnitude is mainly dominated by the real part which is $\frac{-b}{2a}$, the numerator is dominated by $g_m C_{gd,total}$ and the denominator is the sum of multiple capacitor's product. The way to increase the bandwidth is that decrease the width size so that the capacitance will drop that makes the denominator(因次是 2) drops faster than the numerator(因次是 1) while not altering the g_m term too much so that the numerator can still remain the same. The large C_{gd} is mainly contributed from the PMOS, so the width of PMOS is decreased more comparing to NMOS.

So, as conclusion, the main flow can be sectioned into three part.

1. Increases the width and m of both MOS while width of 2 MOS staying at a ratio of 2.5~3 and length fixed.

2. Slightly adjust the channel width respectively for minor improvement after reaching spec, mostly increasing bandwidth and decreasing drain current for better FoM and r_0 matching.

For example, when at $\frac{W}{L_{,P}} = \frac{90\mu m}{0.7\mu m}$ and $\frac{W}{L_{,N}} = \frac{30\mu m}{1.3\mu m}$ and m = 18, it reaches the spec, but the bandwidth is about 200MHz, so I think that slightly decrease both widths to suppress gain can acquire larger bandwidth, and less gain implementing less drain current, this overall increases the FoM.

3. Then lastly is sweep the input current to look for a reasonable bias stage, where the input current can be smaller while still satisfying the SPEC gain, this can also improve FoM.