EE3235 Analog Integrated Circuit Analysis and Design I

Homework 4
Ideal OP circuit

Due date: 2021.11.24 (Wed.) 13:20 (upload to eeclass system)

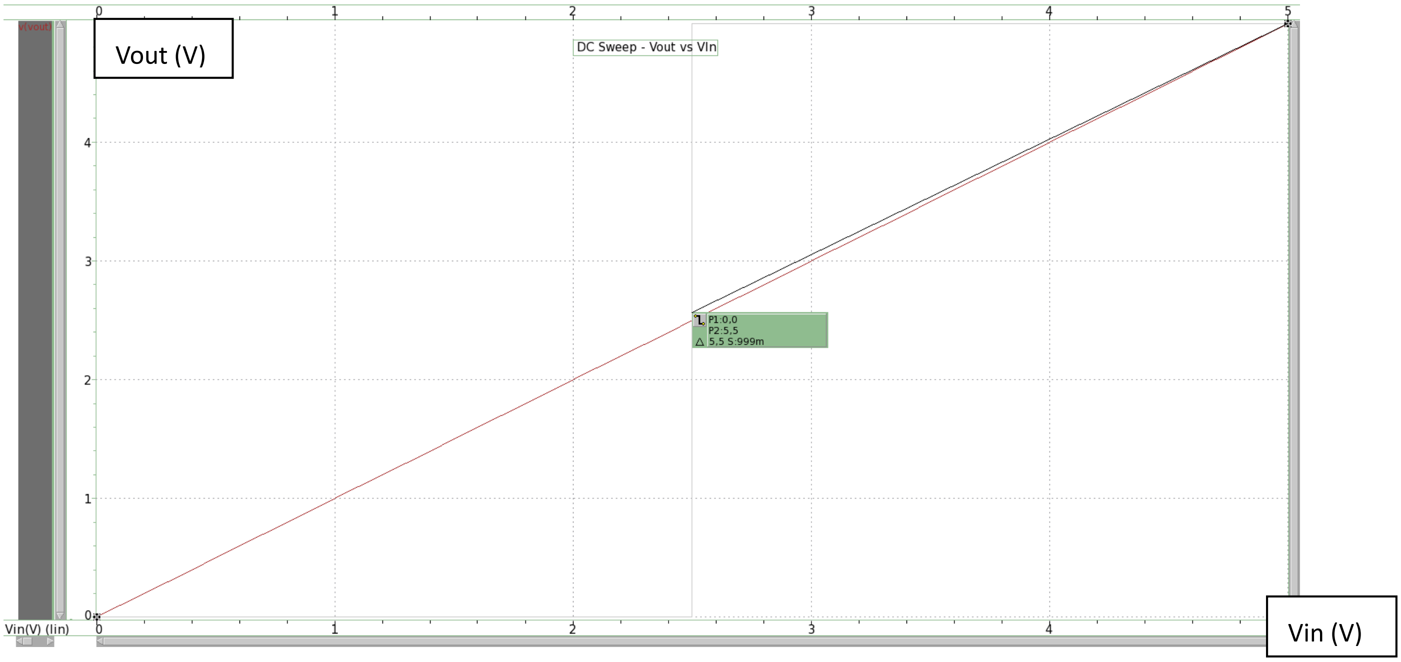
Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

1. Unity – gain Amplifier

(a) DC sweep




```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vout_derivative= 999.0010m
```

(b) TF analysis

```
****     small-signal transfer characteristics

     v(vout)/vin                                =  999.0010m
     input resistance at             vin        =  1.000e+20
     output resistance at v(vout)               =     0.
```

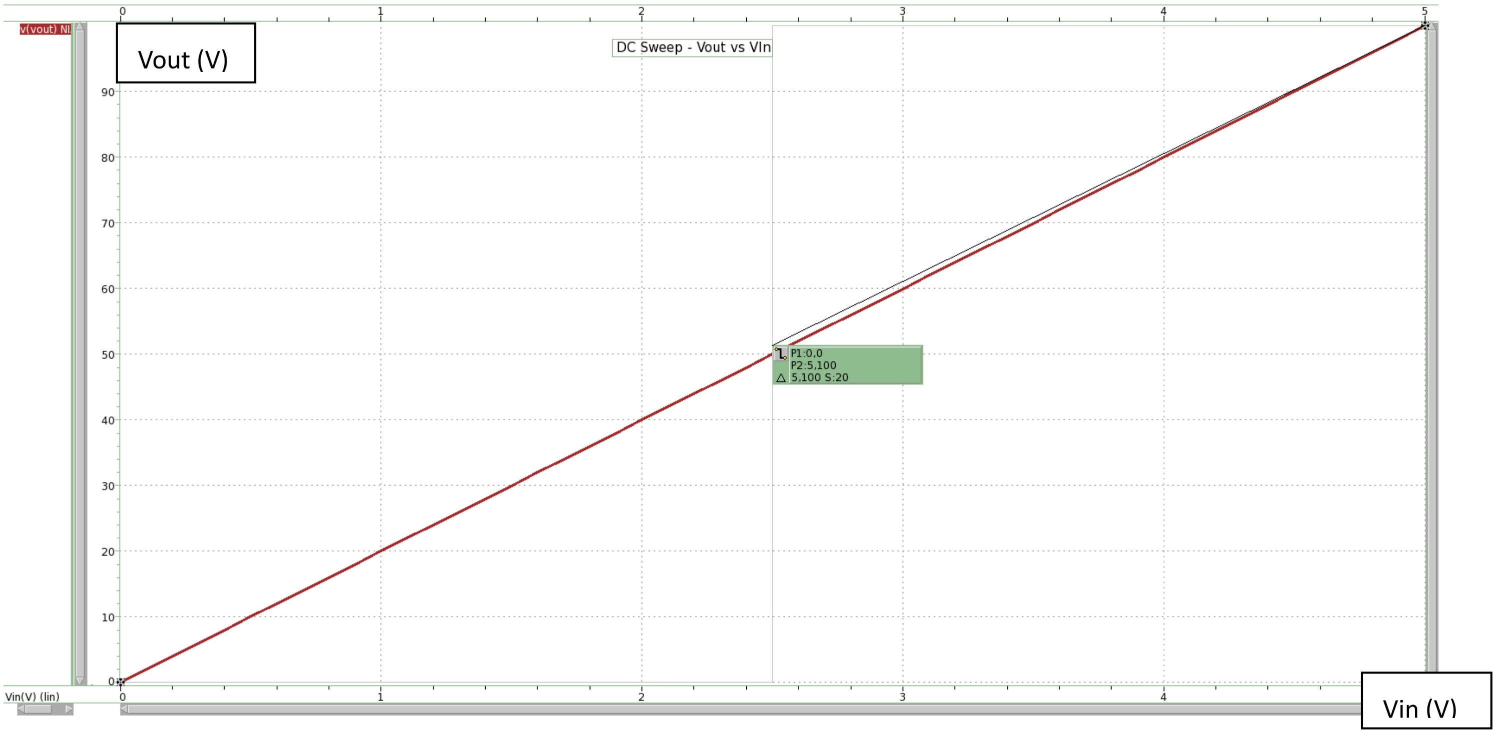
DC gain calculation

$$\frac{V_{out}}{V_{IN}} = \frac{A_0}{1 + A_0} = \frac{1000}{1 + 1000} = 0.999000999\ \left(\frac{V}{V}\right)$$

The simulation is exactly the same except the rounding figures, this simulation is based on considering finite gain with ideal op.

2. Noninverting amplifier

(a) DC Sweep




```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vout_derivative=  19.9922
```

(b) TF analysis

```
****     small-signal transfer characteristics

      v(vout)/vin                                 =   19.9922
      input resistance at             vin         =  1.000e+20
      output resistance at v(vout)                =   0.
```

(c) Design Consideration

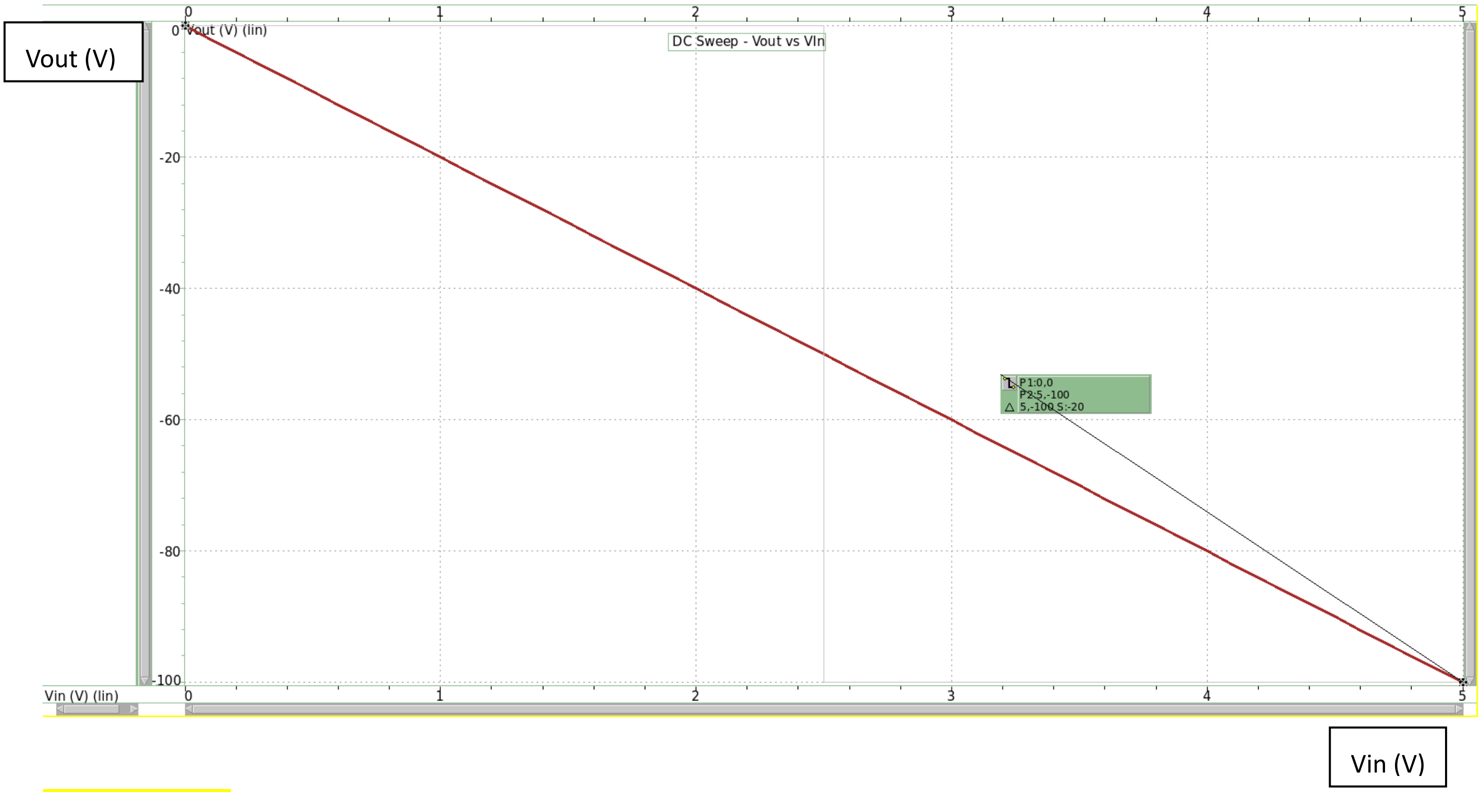
The gain of non-inverting amplifier without considering finite gain is $\frac{R_1+R_2}{R2}$, and considering finite gain is $\frac{R1+R2}{R2}\left(\frac{1}{1+\frac{R1+R2}{R2A_0}}\right)$, so if merely considering the infinite gain model, then the ratio between R_1 and R_2 is 19:1. Then, with the consideration of finite gain, I observe that increasing R_1 by small figure increases the $\frac{R1+R2}{R2}$ term but decreases $\left(\frac{1}{1+\frac{R1+R2}{R2A_0}}\right)$, so with this relationship, I increases 0.2k Ω to R1 every time to approach to the projected gain. Another consideration on the resistor is that courses from electric circuit says op amp usually work with resistors of kΩ, so I choose R1 = 38 kΩ and R2 = 2 kΩ originally and set for 38.8 kΩ and 2 kΩ. The reason of not using R1 = 19 kΩ and R2 = 1 kΩ, is that every 0.2k Ω increment on R1 has much more impact if using smaller R2.

The hand calculated gain of using the selected resistor is $\frac{R1+R2}{R2}\left(\frac{1}{1+\frac{R1+R2}{R2A_0}}\right) = \frac{38.8k\Omega+2k\Omega}{2k\Omega}\left(\frac{1}{1+\frac{38.8k\Omega+2k\Omega}{2k\Omega\times1000}}\right) =$ $19.99215994\ (\frac{V}{V})$, this is exactly the same with the simulation except the rounding figures.

```
**** resistors

subckt
element  0:r1        0:r2
 r value   38.8000k    2.0000k
 v drop    19.0122   980.0078m
 current  490.0039u  490.0039u
 power      9.3160m  480.2077u
```

3. Inverting amplifier

(a) DC Sweep



(b) TF Analysis

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vout_derivative= -20.0206
```

```
****     small-signal transfer characteristics

     v(vout)/vin                              =  -20.0206
     input resistance at          vin         =    4.0817k
     output resistance at v(vout)             =    0.
```

(c) Design Consideration

The gain of inverting amp without considering finite gain is $\frac{-R_1}{R_2}$, and the gain of considering finite gain is $\frac{-R_1}{R_2}\frac{1}{1+\frac{1}{A_0}(\frac{R1}{R2}+1)}$.

The absolute value of $\frac{-R_1}{R_2}$ increases when R_1 increases, but $\frac{1}{1+\frac{1}{A_0}(\frac{R1}{R2}+1)}$ decreases when R_1 increases.

With similar approach on last part, First choose ratio of $\frac{R1}{R2} = 20$ as a design start point and resistor of kΩ level. Then increases R_1 by 0.2 kΩ to observe the gain. I choose R_2 = 4 kΩ and R_1 = 80 kΩ as starting point, I use 4:80 instead of 1:20 because larger R_2 is less sensitive to every 0.2 kΩ increment on R_1. Eventually, I set for R_1 = 81.8kΩ and R_2 = 4 kΩ.

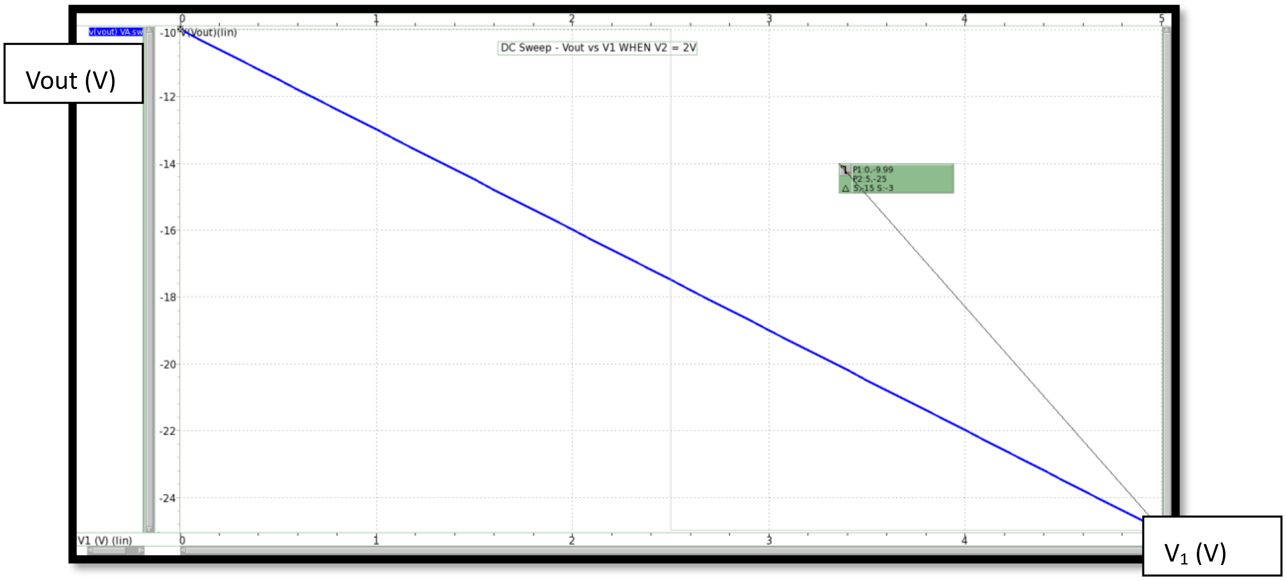
The hand calculated gain is $\frac{-R_1}{R_2}\frac{1}{1+\frac{1}{A_0}(\frac{R1}{R2}+1)} = \frac{-81.8k}{4k}\frac{1}{1+\frac{1}{1000}(\frac{81.8k}{4k})} = -20.02055901(\frac{V}{V})$

The hand calculated value is exactly the same with the simulated result except the rounding figures.

```
**** resistors

subckt
element  0:r2        0:r1
 r value    4.0000k   81.8000k
 v drop     0.         0.
 current    0.         0.
 power      0.         0.
```

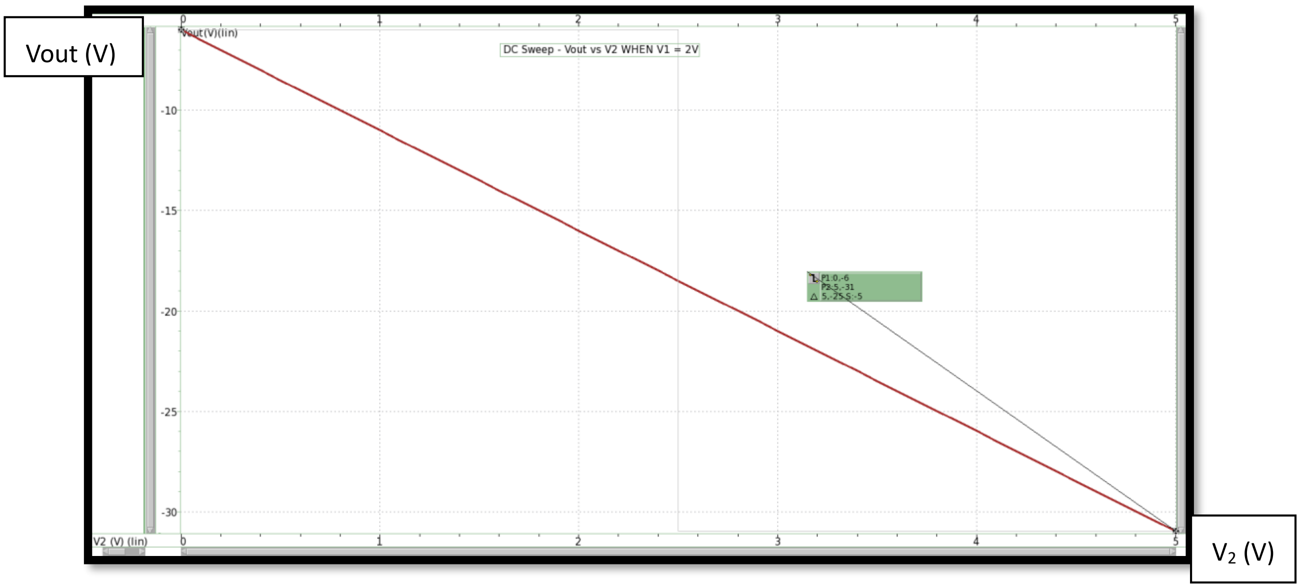
4. Voltage adder

(a) DC Sweep



	X1	Y1	X2	Y2	DeltaX	DeltaY	Slope	Show
1	0	-9.99	5	-25	5	-15	-3	☑

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
slope1=  -2.9978
******
```



	X1	Y1	X2	Y2	DeltaX	DeltaY	Slope	Show
1	0	-6	5	-31	5	-25	-5	☑

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
slope2=  -4.9964
```

The reason of using derivative of V_{out} at 2.5V instead of average of derivative of V_{out} from 0V to 5V in part(a) is because the derivative at boundary point (0V to be specific) doesn't follow the rest of the points on the straight slope which diluted the real slope.

(b)

Comments:

The relation is between slope1/slope2 and the function is that when V2 is fixed then the slope1 simply approaches to the negative value of the coefficient of V1 for the given function, and it goes the same for slope 2 and V2 when V1 being fixed.

$$\frac{V_1 - V_X}{R_1} + \frac{V_2 - V_X}{R_2} = \frac{V_X - V_{out}}{R_F}$$

$$V_{out} = A_0(0 - V_x) = -A_0 V_x$$

With above relation, we can get $\frac{V_1 + \frac{V_{out}}{A_0}}{R1} + \frac{V_2 + \frac{V_{out}}{A_0}}{R2} = \frac{\frac{-V_{out}}{A_0} - V_{out}}{R_F}$

$$\Rightarrow \quad -V_{out} = \frac{A_0 R_2 R_F}{(R_1+R_2)R_F+(1+A_0)R_1R_2} V_1 + \frac{A_0 R_1 R_F}{(R_1+R_2)R_F+(1+A_0)R_1R_2} V_2$$

For My design, I select R_1 = 20 kΩ, R_2 = 12 kΩ, R_F = 60.5 kΩ

For slope 1, since V_2 is fixed, the slope is simply the term $\frac{A_0 R_2 R_F}{(R_1+R_2)R_F+(1+A_0)R_1R_2} = \frac{1000 \times 12k \times 60.5k}{(20k+12k)\times 60.5k+(1+1000)12k\times 20k} = 2.9978$

For slope 1, since V_2 is fixed, the slope is simply the term $\frac{A_0 R_1 R_F}{(R_1+R_2)R_F+(1+A_0)R_1R_2} = \frac{1000 \times 20k \times 60.5k}{(20k+12k)\times 60.5k+(1+1000)12k\times 20k} = 4.9964$

The hand calculated value is identical to the simulation result except for a negative sign needed to be add in front, since the device is an inverting summer.

(c) design consideration

Although the above equations relation gives an exact approach of getting the desired R_F value for setting R_1 and R_2 constant ratio (e.g. R1 = 5x, R2 = 3x). But since it only has two voltage input, so I can view it as two inverting amplifiers with linear addition without huge difference to the simulation result. The function without considering finite gain is $-R_F(\frac{V_1}{R_1} + \frac{V_2}{R_2})$

So, I first considered the case of R_1 = 20 kΩ, R_2 = 12 kΩ, R_F = 60 kΩ where 60 is the lcm of 12 and 20 and $\frac{60}{20} = 3$, $\frac{60}{12} = 5$
Then combining the experience from the inverting amplifier, having a small amount of increment to R_F will make the gain value (considering finite gain) approaches to the requested value. So, I set R_1 = 20 kΩ, R_2 = 12 kΩ, R_F = 60.5 kΩ and gets the result that I wanted with slope error < 1%.

```
**** resistors

subckt
element  0:r1        0:r2        0:rf
 r value  20.0000k    12.0000k    60.5000k
 v drop    1.9840      1.9840     16.0044
 current  99.2006u   165.3343u   264.5349u
 power   196.8151u   328.0252u     4.2337m
```

5. Square-Root Amplifier

(a) DC sweep


```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vov1= 189.6916m
vov2= 280.3825m
vov3= 350.1854m
vov4= 409.5455m
vov5= 462.8839m
```

(b)

Vin	Simulation Vov (mV)	Calculation Vov(mV)	error	error square	ERR
1	189.6916	189.6916	0	0	0.02103
2	280.3825	268.2644334	0.04517	0.002040518	2.10%
3	350.1854	328.555489	0.06583	0.004334031	
4	409.5455	379.3832	0.0795	0.00632081	
5	462.8839	424.1633124	0.09129	0.008333313	

(c) design consideration

The first thought of setting the W/L value is that since the ideal formula discard the effect of channel length modulation, so for the neglection of channel length modulation, I set $\frac{W}{L} = \frac{2\mu m}{1\mu m}$ a common ratio with micrometer level of channel length.

Then, considering the NMOS in saturation and finite gain is put into consideration. The equation considering finite gain should look like $\frac{V_{in}+\frac{V_{out}}{A_0}}{R_1} = \frac{1}{2}\,\mu_n C_{ox}\frac{W}{L}(-V_{out} - V_{TH})^2$, neglecting channel length modulation when in saturation.

There are plenty to notice, the LHS of the equation tells that if V_{out} is large due to amplification then the device won’t be close to a square root amplifier, since the original design taught on course didn’t consider the term $\frac{V_{out}}{A_0}$. Making R_1 larger has same concepts of dropping the gain on output side of the inverting amplifier case. Consider that the MOSFETS in previous homework usually operates in microamps, combining that I want to make $\frac{V_{out}}{A_0}$ neglectable and the LHS can be simply viewed as $\frac{V_{in}}{R_1}$ by making R_1 large, so I set the starting R_1 to 50kΩ. The small signal parameters then can be found for detailed calculation.

But, at 50kΩ, the overdrive voltage doesn’t follow the square root growth when the input voltage is at 5V, this indicates that the source voltage is amplified negative to an extend that the drain current doesn’t grow in square order, so Resistance had to be increased.
Then few more increment on R_1 to make the overdrive voltage stays in square root growth and also making $\frac{V_{in}}{R_1}$ approaches close to the drain current for 1~5 V respectively. Eventually I stick for R_1 = 98kΩ and the ERR is 2.1%.

Another perspective provided by classmates is that increasing resistance also increases the voltage drop across R1, this then makes V_X approximately become a virtual short.

```
**** resistors

subckt
element   0:r1
 r value    98.0000k
 v drop      4.9993
 current    51.0128u
 power     255.0256u
```

M1 operating point from 1V – 5V

```
**** mosfets


subckt
element   0:m1
model     0:n_18.1
region    Saturation
  id          10.1990u
  ibs         66.8439n
  ibd        -1.052e-19
  vgs        502.5534m
  vds        503.0559m
  vbs        502.5534m
  vth        312.8618m
  vdsat      168.4131m
  vod        189.6916m
  beta       615.8308u
  gam eff    496.4716m
  gm          93.5025u
  gds          1.1099u
  gmb          9.6448u
  cdtot        3.2826f
  cgtot       14.0742f
  cstot       15.1596f
  cbtot        7.0839f
  cgs         12.9658f
  cgd        738.6390a
```

```
**** mosfets


subckt
element   0:m1
model     0:n_18.1
region    Saturation
  id          20.4022u
  ibs          1.5676u
  ibd        -1.203e-19
  vgs        583.6221m
  vds        584.2057m
  vbs        583.6221m
  vth        303.2395m
  vdsat      228.5102m
  vod        280.3825m
  beta       616.9924u
  gam eff    495.1403m
  gm         133.2467u
  gds          1.7331u
  gmb         11.8240u
  cdtot        3.2874f
  cgtot       14.1024f
  cstot       15.1584f
  cbtot        6.9936f
  cgs         13.0651f
  cgd        743.4892a
```

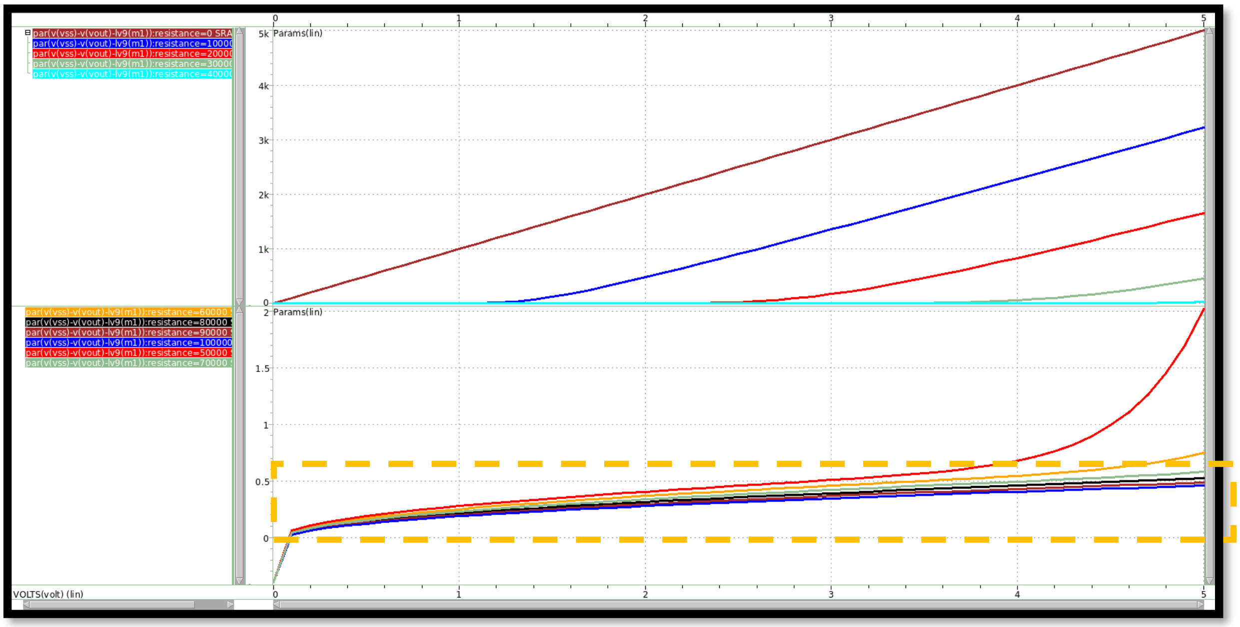
```
**** mosfets


subckt
element   0:m1
model     0:n_18.1
region    Saturation
  id          30.6056u
  ibs         18.1212u
  ibd        -1.314e-19
  vgs        646.5314m
  vds        647.1779m
  vbs        646.5314m
  vth        296.3460m
  vdsat      274.4311m
  vod        350.1854m
  beta       617.3257u
  gam eff    494.1689m
  gm         162.4146u
  gds          2.2364u
  gmb         12.7946u
  cdtot        3.2891f
  cgtot       14.1159f
  cstot       15.1532f
  cbtot        6.9382f
  cgs         13.1258f
  cgd        746.4820a
```

```
**** mosfets


subckt
element   0:m1
model     0:n_18.1
region    Saturation
  id          40.8092u
  ibs        146.5039u
  ibd        -1.407e-19
  vgs        700.3707m
  vds        701.0710m
  vbs        700.3707m
  vth        290.8252m
  vdsat      313.0758m
  vod        409.5455m
  beta       617.1953u
  gam eff    493.3787m
  gm         186.5183u
  gds          2.6710u
  gmb         13.2540u
  cdtot        3.2896f
  cgtot       14.1272f
  cstot       15.1523f
  cbtot        6.8995f
  cgs         13.1733f
  cgd        748.6610a
```

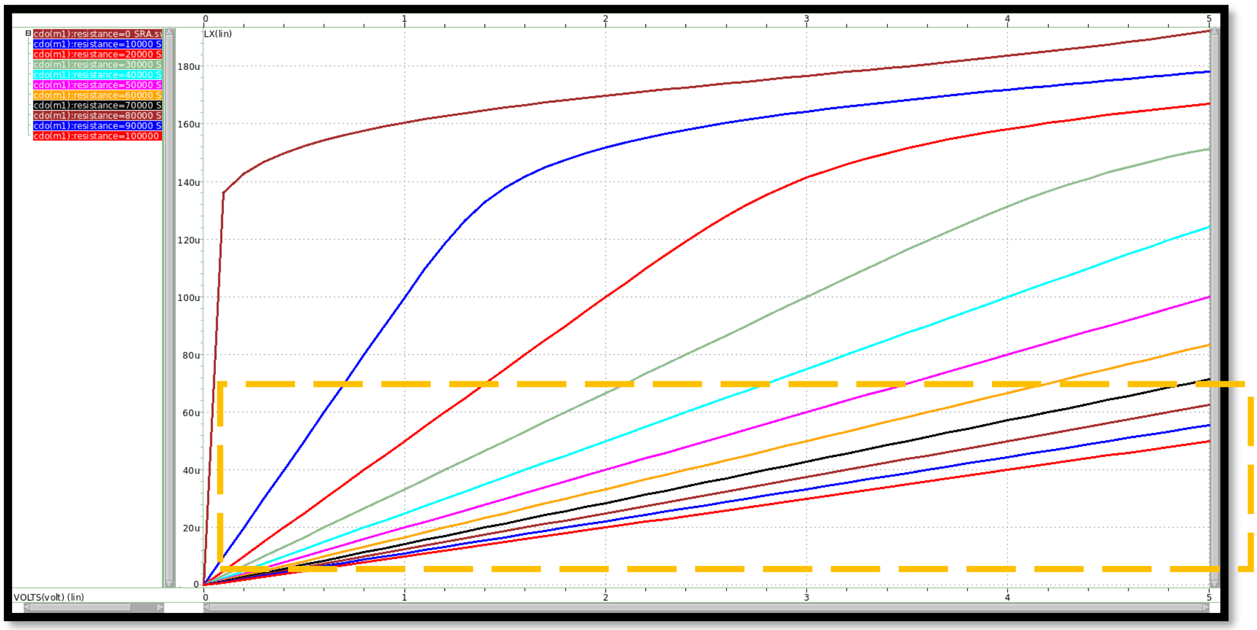
```
**** mosfets


subckt
element   0:m1
model     0:n_18.1
region    Saturation
  id          51.0128u
  ibs        943.2844u
  ibd        -1.488e-19
  vgs        749.0563m
  vds        749.8053m
  vbs        749.0563m
  vth        286.1723m
  vdsat      347.1276m
  vod        462.8839m
  beta       616.7504u
  gam eff    492.7028m
  gm         207.4606u
  gds          3.0575u
  gmb         13.4340u
  cdtot        3.2894f
  cgtot       14.1374f
  cstot       15.1543f
  cbtot        6.8712f
  cgs         13.2131f
  cgd        750.3939a
```

Observation after design

Overdrive voltage DC sweep for R1 = 0kΩ to 100kΩ with fixed $\frac{W}{L}$



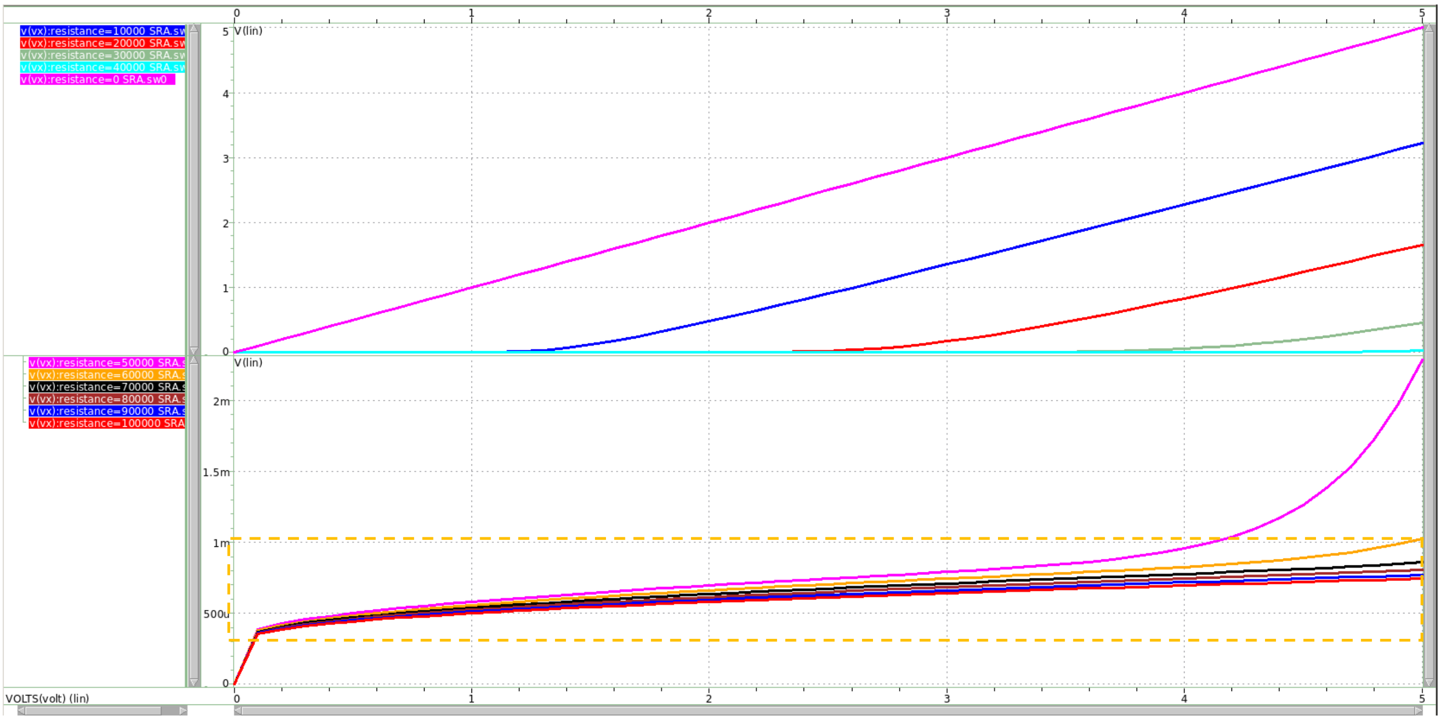
Drain current DC sweep for R1 = 0kΩ to 100kΩ with fixed $\frac{W}{L}$



The overdrive drive voltage and drain current that I boxed in yellow dashed line is the curve we are looking for to design a square root amplifier. First for my $\frac{W}{L}$ fixed，if the drain current is too high, it then grows in a flat curve, and the corresponding overdrive voltage blows up instead of growing in square root order.

This also occurs to me that when the source side is too negative, then the body diode is turned on. This causes leakage current which makes the overdrive voltage grows larger than normal. So using higher resistance also prevents this from happening.

V_X DC sweep for or R1 = 0kΩ to 100kΩ with fixed $\frac{W}{L}$



Having a small resistance also causes V_X to be large through feedback where the negative input port cannot approach to a virtual short. The region where the yellow dashed line boxed has small V_X and doesn't vary much for increasing V_{in}.