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EE3235 Analog Integrated Circuit Analysis and Design I

Homework 1
Process Analysis

Due date: 2021.10.13 (Wed.) 13:20 (upload to eeclass system)

In this homework, you are to run HSPICE and evaluate the device performance with threshold voltage V_{th}, transconductance g_m, output conductance g_{ds}, saturation drain voltage V_{dsat}, intrinsic gain $g_m r_O$, power efficiency g_m/I_D, speed g_m/C_g, drain current I_D, and body effect as the benchmarks.

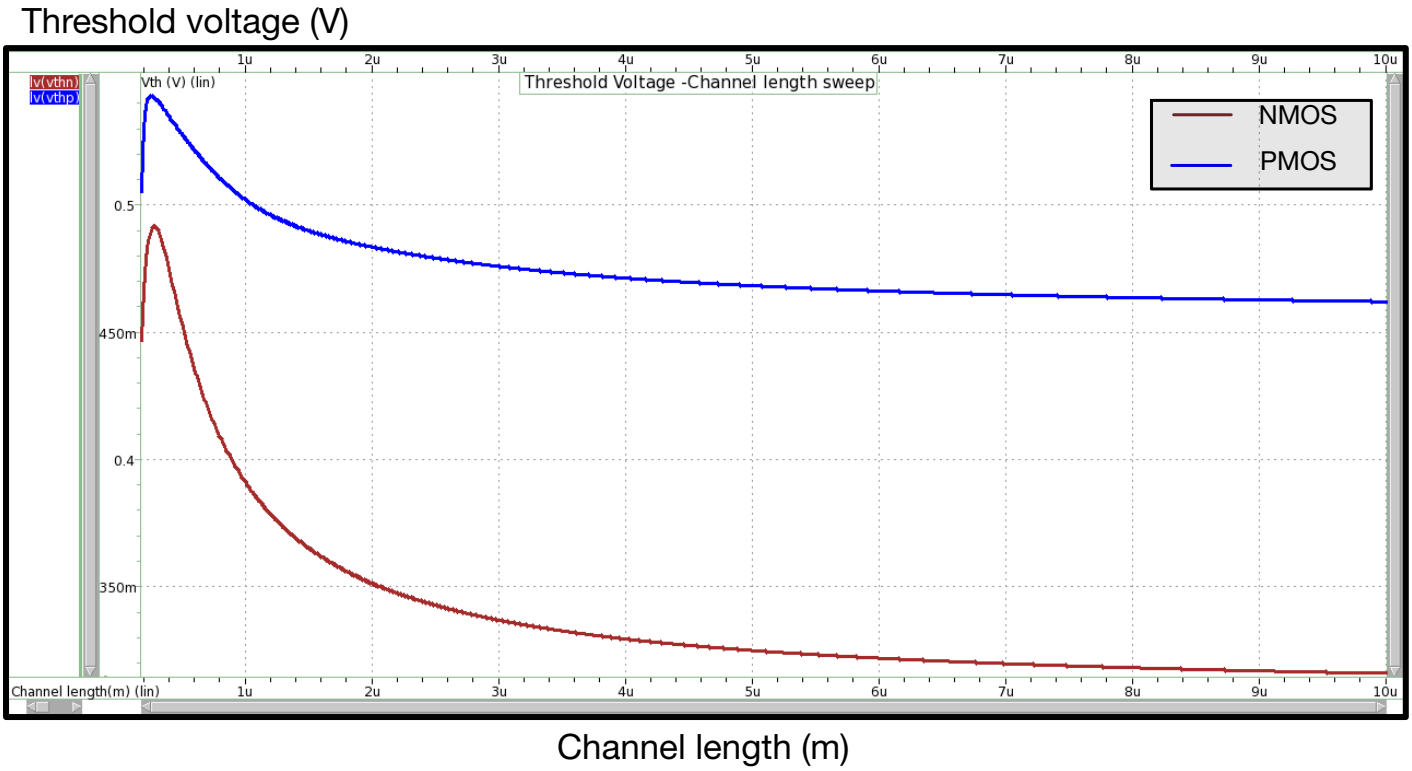
Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

Part 1. Analyze with Diode Connected Structure

(1) Threshold Voltage V_{th}



Comment:

With the sweeping channel length increasing in the $(180\text{nm} - 300\text{nm})$ region, the threshold voltage rises as the channel length increases for both diode-connected NMOS and PMOS with the W/L ratio stays at 2, but after that they hit a peak *(491 mV for the NMOS and 543 mV for the PMOS)* and began to drop as the channel length increases, even goes lower than the starting sweep length (0.18 um) for both cases.

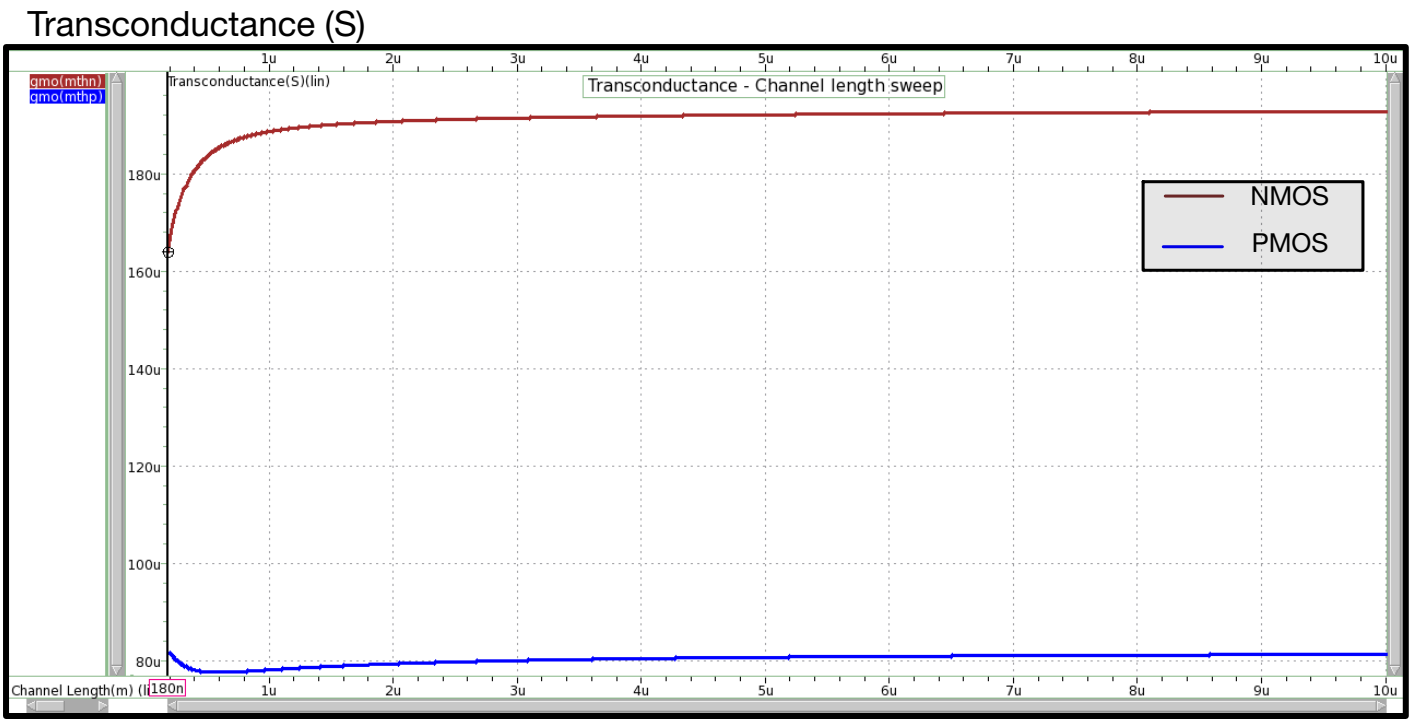
From the formula of the V_{TH} roll-off of short channel effect:

$\Delta V_{TH} = \frac{-qN_A W_T}{C_{ox}} \frac{L-L'}{2L}$ where L stands for upper channel length and L' stands for lower channel length, this is more significant for shorter channel length since the relative difference between two lengths is larger, causing the threshold voltage rises when the channel length increases for short channel.

Also, when channel length is small with same V_{DS} and V_G, the inversion charge density is more concentrated at the channel so that less threshold voltage needs to be overcome to make the MOS be on, so in the region of 180nm – 300nm this can be observed.

But after that the threshold voltage decreases for increasing channel length, this is because there exists reverse short channel effect.

(2) Transconductance g_m



Comment:

From known formula:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$g_m = \mu_{n(p)} C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)$$

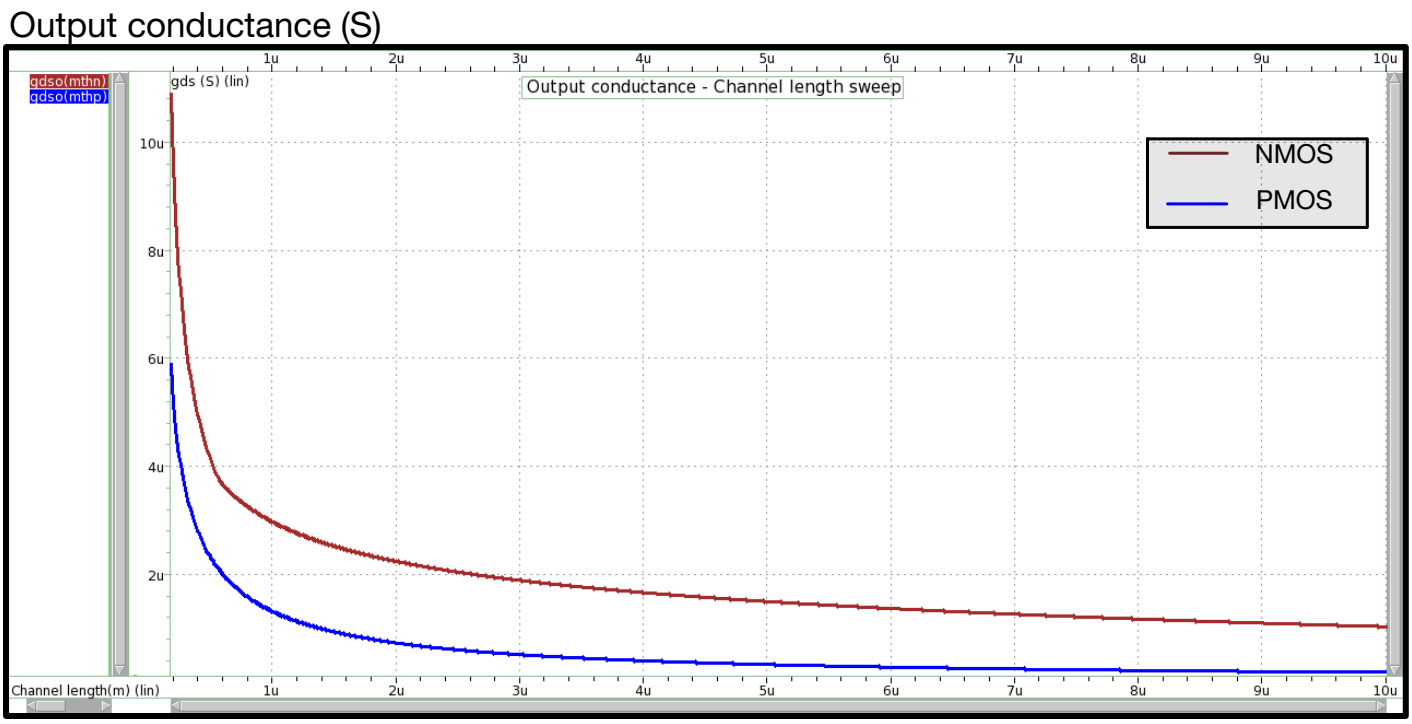
The transconductance of the diode-connected NMOS has increased with the channel length as it increases and the slope has reduced and after 2um. Indicating that the drain current change rate with respect to V_{GS} will be less affected by channel length after it reaches 2um.

The transconductance of the diode-connected PMOS has a slight drop in the $(180\text{nm} - 400\text{nm})$ region and then start rising with a relatively small slope. The whole curve indicates that the transconductance of PMOS diode connected is less sensitive with respect to the channel length change comparing to the diode connected NMOS in the $(180\text{nm} - 400\text{nm})$ region.

Also, since the transconductance of the NMOS is larger than the PMOS in the graph, so it indicates that the change of drain current with respect to V_{GS} change is larger for NMOS than the PMOS throughout the sweeping length.

The transconductance supposedly should grow linearly with channel length increasing, because the previous simulation shows that $|V_{TH}|$ decreases with channel lengths increases. After probing $|V_{GS}|$, I found out that $|V_{GS}|$ has similar pattern parallel with $|V_{TH}|$, $|V_{GS}|$ first increases for increasing channel length for small channel, but after hitting a value, $|V_{GS}|$ then drops. So that with $|V_{GS}|$ and $|V_{TH}|$ decreases together causing the transconductance doesn't grow linearly.

(3) Output conductance g_{ds}



Comment:

From known formula:

$$r_o^{-1} = \frac{\partial I_D}{\partial V_{DS}} \quad \text{and} \quad r_o^{-1} = \frac{1}{2}\mu_{n(p)} C_{ox} \frac{W}{L}(|V_{GS}| - |V_{TH}|)^2 \times \lambda$$

The Output Conductance drops as channel lengths increases, and the drop in the (180nm − 1um) region is immense, and after that the slope decreases for both diode-connected PMOS and NMOS. Another thing to notice is that the output conductance of the NMOS remains higher than the PMOS throughout the sweep. The graph indicates that the drain current change with respect to the V_{DS} change is larger for the NMOS than the PMOS.

The output conductance is related to the channel length modulation effect, the effect is negligible for long channel length so that the output conductance decreases.

The decrease rate of the output conductance of the NMOS in the (180nm − 1um) region is

$$\frac{-9.67S\ (output\ conductance)}{1\mu m\ (channel\ length)}$$

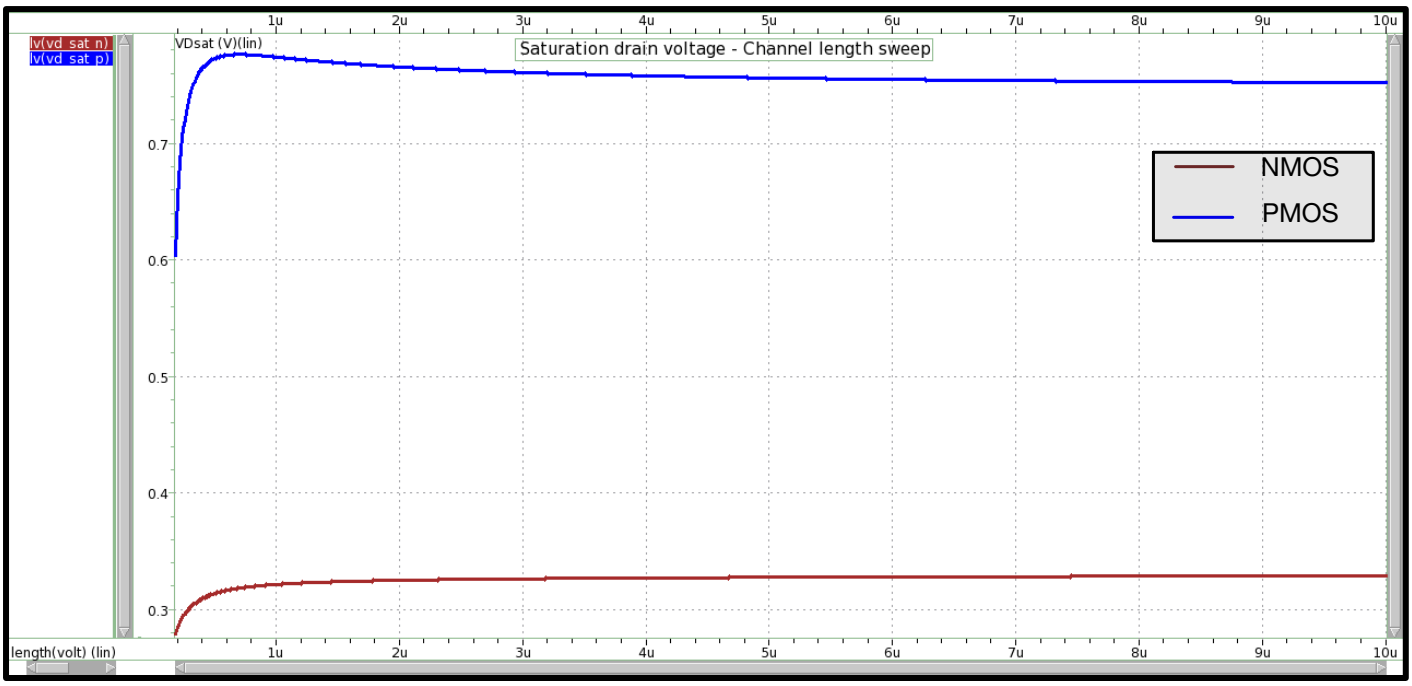
The decrease rate of the output conductance of the PMOS in the (180nm − 1um) region is

$$\frac{-5.56S\ (output\ conductance)}{1\mu m\ (channel\ length)}$$

This also indicates that the change is more sensitive for NMOS with respect to the change of channel length comparing to PMOS in the (180nm − 1um) region.

(4) Saturation drain voltage V_{dsat}

Saturation drain voltage (V)



Channel length (m)

Comment:

The saturation voltage rises at first in the 180nm - 600nm of sweeping channel length for the diode-connected PMOS, and after that it has a slight drop and stay stable after the channel length is increased to 5um.

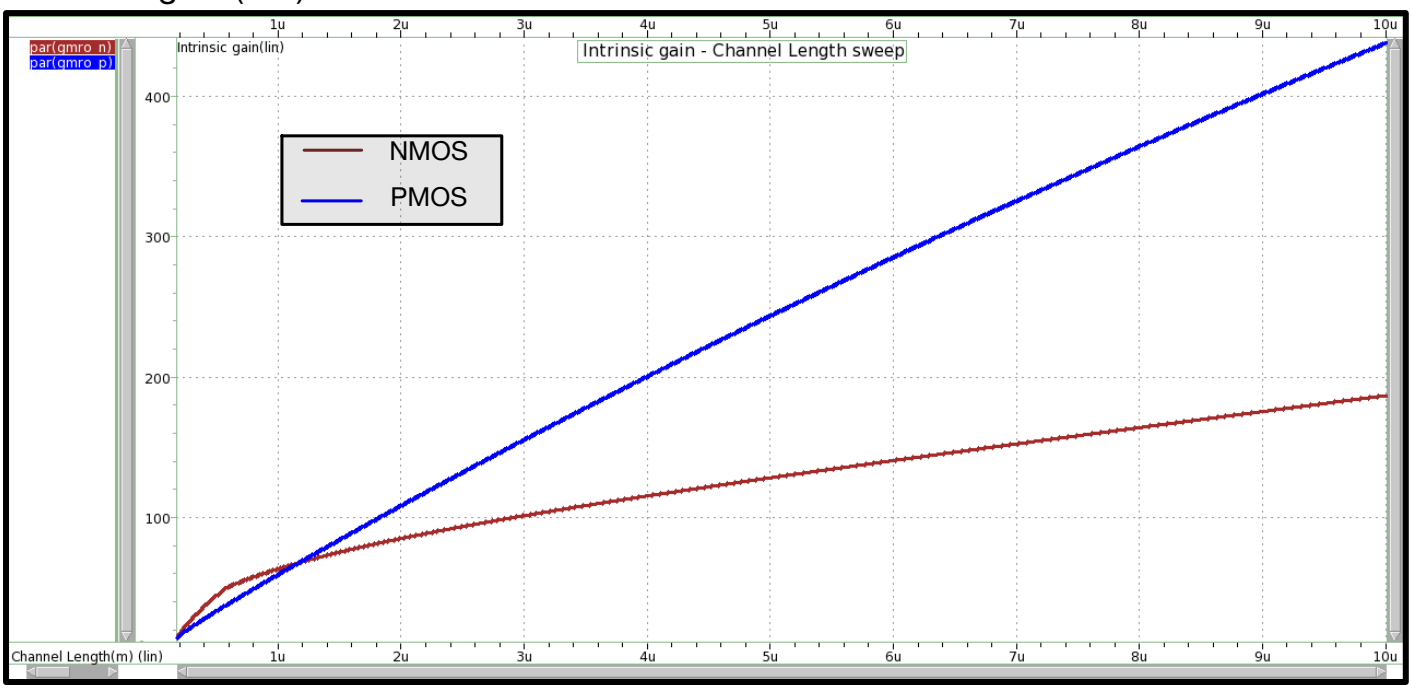
In contrast to the diode-connected PMOS, the counterpart NMOS has no drop throughout the sweep and quickly converge to a near-constant saturation drain voltage after the length is increased to 2um.

Both cases display that the saturation drain voltage becomes more channel length independent after the MOS' channel length has reached a certain length. But behaves different for smaller channel length.

Since $V_{D,sat} = V_{GS} - V_{TH}$, so the saturation drain voltage should rise if threshold voltage drops, the graph makes sense for the NMOS but acts differently for the PMOS, the saturation drain voltage acts parallel with the threshold voltage. So, there might be second order effect on saturation drain voltage if the channel length is increased that makes the V_{GS} changes parallel with threshold voltage also.

(5) Intrinsic gain $g_m r_o$

Intrinsic gain (V/V)



Channel length (m)

Comment:

The intrinsic gain of the diode connected NMOS is higher than the diode-connected PMOS before the cross-point (channel length of 1.18um where the intrinsic gain is 68.1 for both MOS). After that, the intrinsic gain of the diode-connected PMOS become larger than the diode connected NMOS, since it has a larger growing slope from the sweeping origin (0.18 um).

The increase rate of the intrinsic gain of PMOS is $\frac{41.92\ (intrinsic\ gain)}{1\mu m\ (channel\ length)}$ after the cross-point

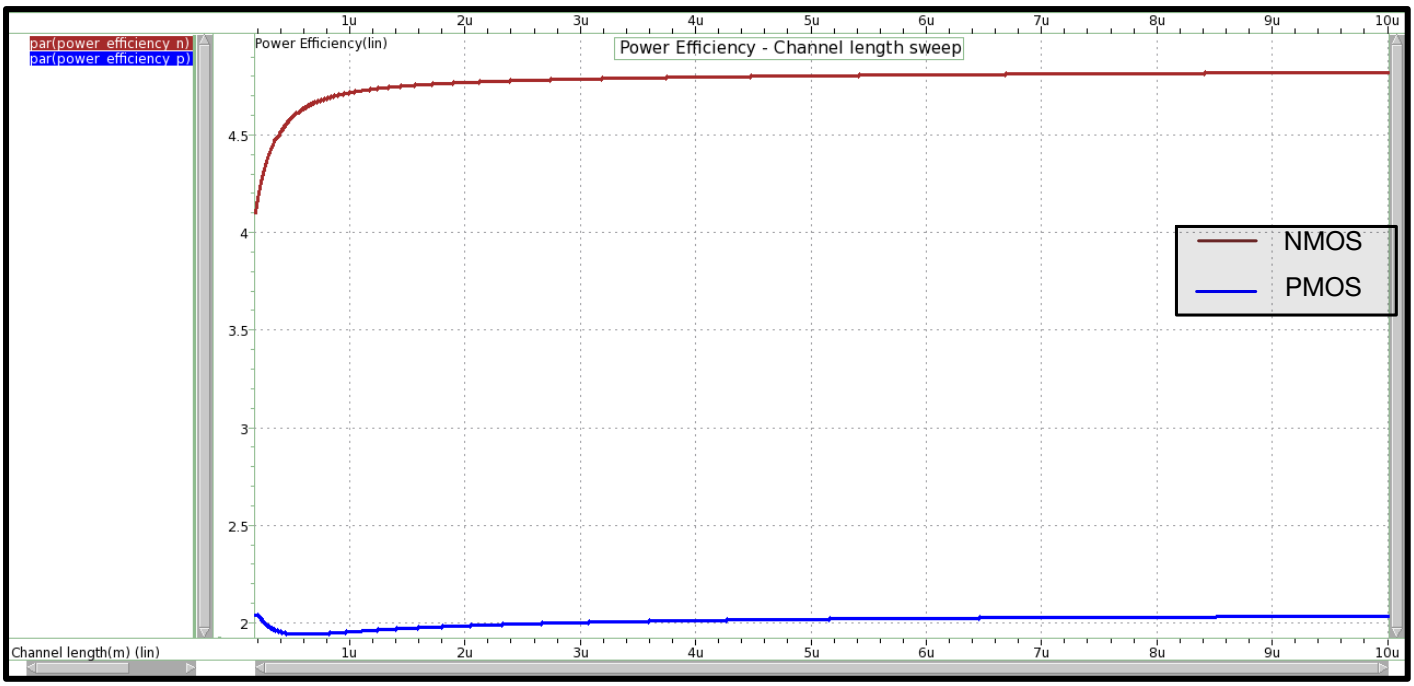
The increase rate of the intrinsic gain of NMOS is $\frac{13.5\ (intrinsic\ gain)}{1\mu m\ (channel\ length)}$ after the cross-point

It can be observed that there is a trade off between size of MOS and the intrinsic gain performance, with higher intrinsic gain acquired, more budget needs to be spent on the size.

And from the graph the intrinsic gain has a steady growing curve while the transconductance has a flat curve, so this means that the output resistance is growing with channel length increasing.

(6) Power Efficiency g_m/I_D

Power efficiency (1/V)



Channel length (m)

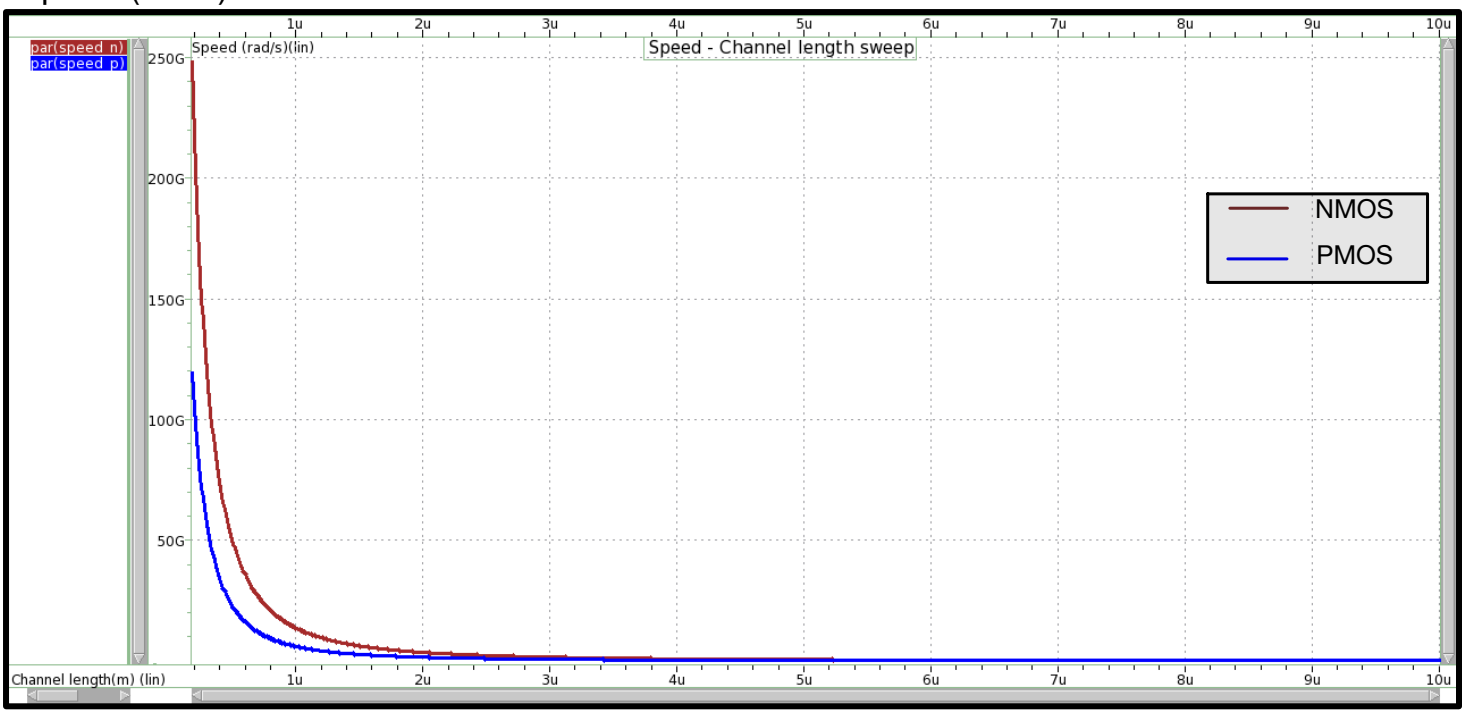
Comment:

The power efficiency behaves parallel with the transconductance since Power efficiency is transconductance divided by Drain current, and since in saturation region the drain current of both MOS can be written as $|I_D| = \frac{1}{2}\mu_{n(p)}C_{ox}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2(1 + \lambda|V_{DS}|)$, and everything remains constant throughout the sweep so that the power efficiency can show a parallel relationship with the transconductance.

Also, the intrinsic gain is $g_m r_o$, and is related to g_m, so we can see the power efficiency as a factor of how much gain we can attain for giving certain amount of drain current.

(7) Speed g_m/C_g

Speed (rad/s)



Channel length (m)

Comment:

The speed of the diode-connected NMOS is higher than the diode-connected PMOS in the $(180\text{nm} - 1\mu\text{m})$ region, but after that the both speeds drops with a small slope as channel length increases. I also observe that the speed drops drastically in the previous mentioned region $(180\text{nm} - 1\mu\text{m})$ with a steep slope.

From known formula

$$C_{GS} = \frac{2}{3}C_{ox} \times W \times L_{eff} + WL_{ov} \times C_{ox}$$

$$C_{GD} = WL_{ov} \times C_{ox}$$

So that the gate capacitance increases as W and L increases, so the speed drops as the sweeping channel length increases, since the W/L is fixed at 2, so the total gate capacitance increases leading to the speed decreasing.

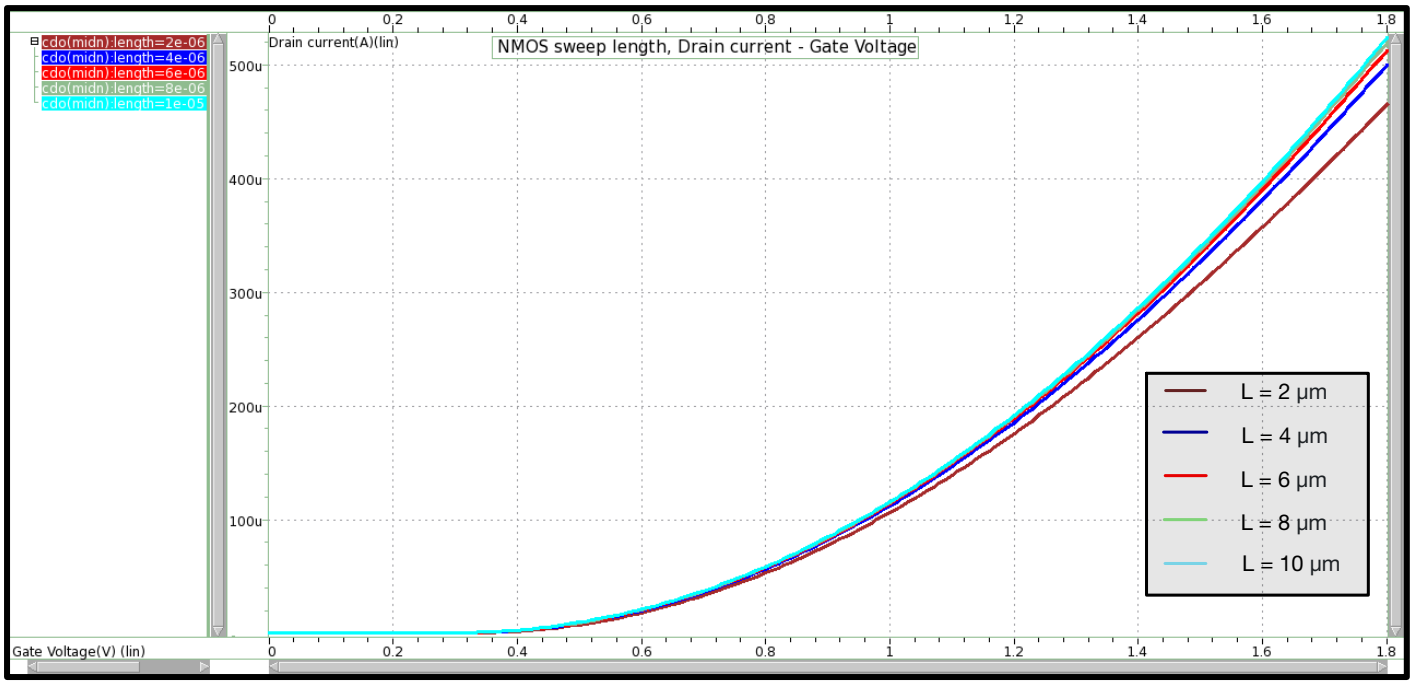
Since my past lecture hasn't covered about C_{GB} and further W/L modulation effect, but I think the reason that the speed is not decreasing that fast after 1um might be because the gate capacitance of MOS will become W and L independent once the channel length approaches a value (in this simulation is 1um).

$\left(\text{NMOS speed decrease rate: } \frac{-285.7G}{1\,\mu m}\ PMOS\ speed\ decrease\ rate: \frac{-137.8G}{1\mu m}\right)$ both for in the region $(180\text{nm} - 1\mu\text{m})$

Part 2. Drain Current I_D

(1) I_D vs V_G (NMOS)

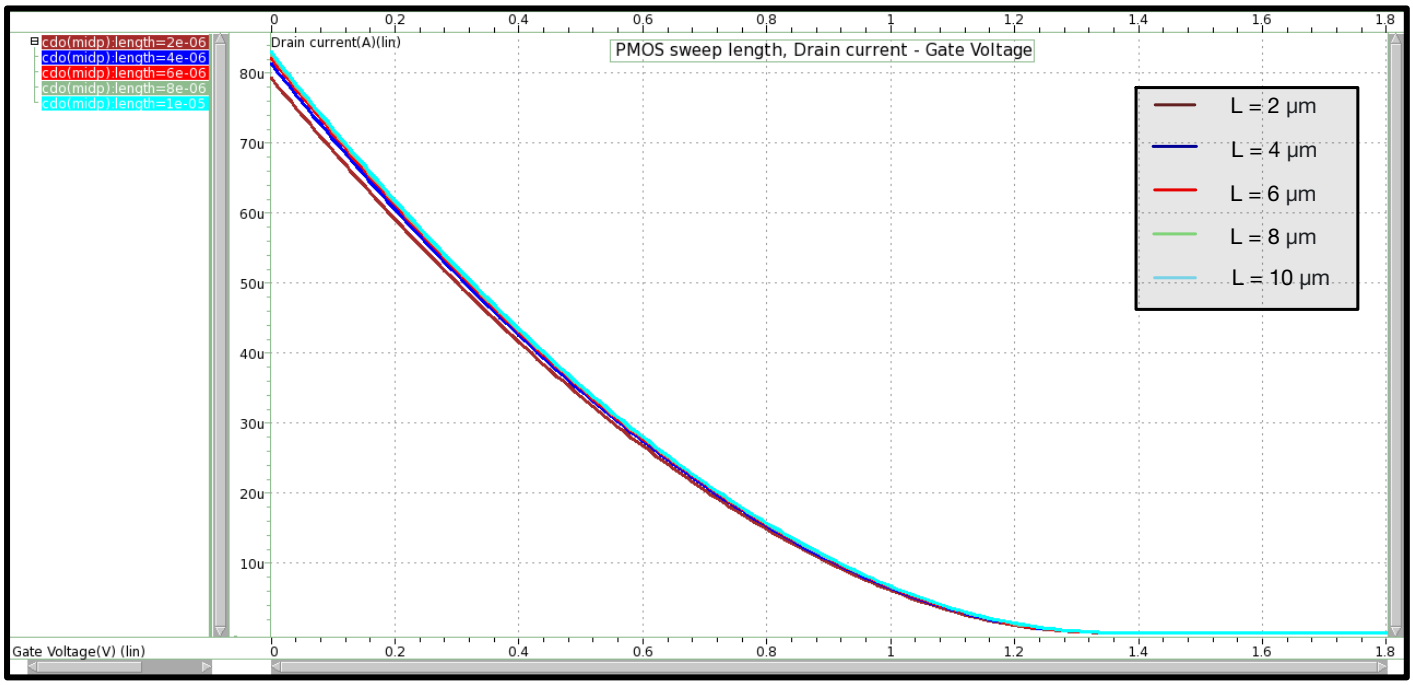
Drain current (A)



Gate voltage (V)

(2) I_D vs V_G (PMOS)

Drain current (A)



Gate voltage (V)

Comment:

In both NMOS and PMOS cases, I observed that the drain current doesn't varies much with its channel length, and both cases shows that with the W/L ratio fixed at 2, the drain current are slightly increased as the channel lengths increases, this shows that increasing channel width has more impact on increasing the drain current than increasing the channel length on decreasing the drain current when the W/L ratio is fixed.

From known formula and concepts:

1. $|V_{GS}|$ has to exceed some specific value of $|V_{TH}|$ so that the MOS are on.
2. Drain current of MOS in saturation regions is $|I_D| = \frac{1}{2}\mu_{n(p)}C_{ox}\frac{W}{L}(|V_{GS}| - |V_{TH}|)^2(1 + \lambda|V_{DS}|)$.

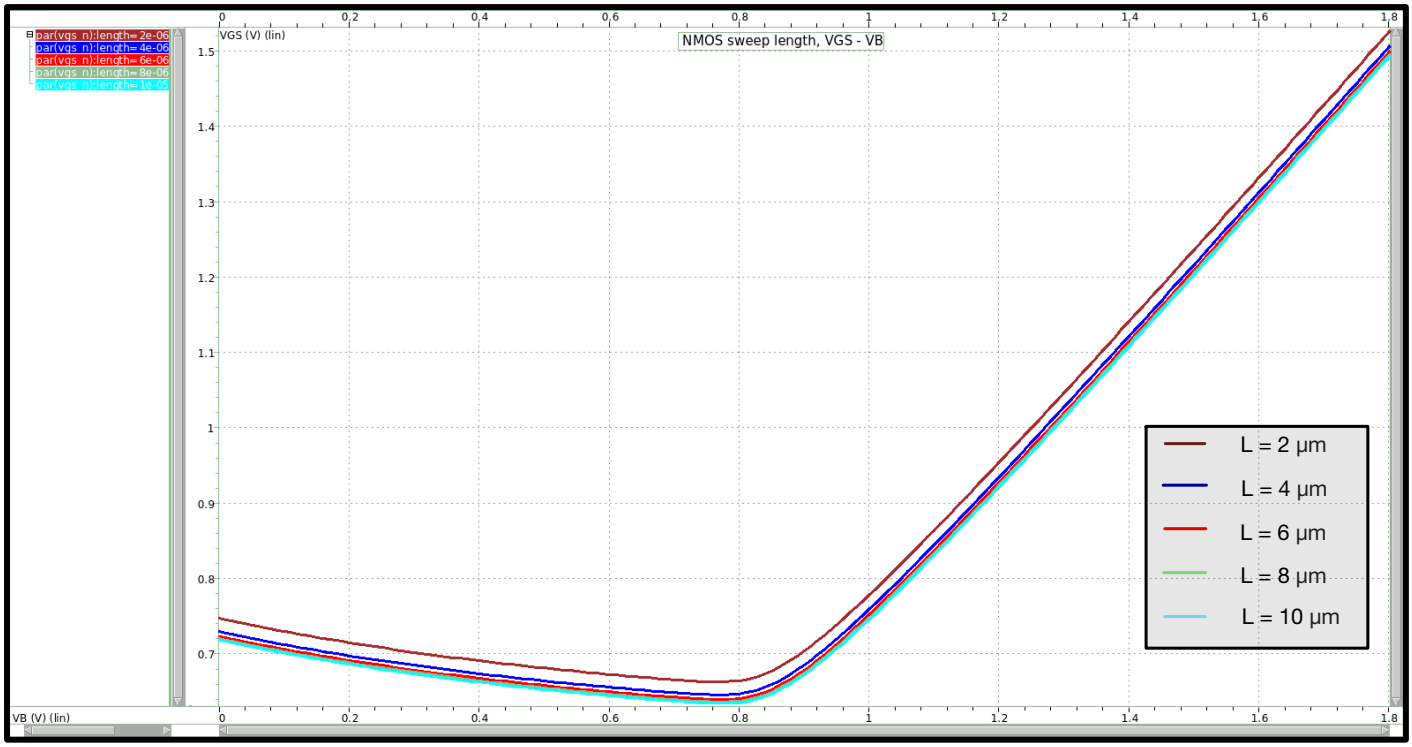
For the NMOS case, increasing the gate voltage until about 0.4V, then the NMOS started to provide drain current, indicating that the gate voltage has exceeded the built-in threshold voltage, and the NMOS are in saturation region since V_{GS} is always smaller than V_{DS} in the sweeping region (Where V_D is at 1.8V and V_G is sweeping from 0V to 1.8V) so that the drain currents grows in order of 2 after the gate voltage exceeds the threshold voltage.

For the PMOS case, increasing the gate voltage decreases the drain current, since the voltage difference between gate and voltage is getting smaller and is approaching to its threshold voltage (negative value). And when gate voltage is at around 1.2V, the PMOS is off. During the gate voltage region where PMOS is on, it is in saturation region since the drain is negative enough (using the source as reference point) contrast to (V_G – V_{TH}), and it shows that as gate voltage increases, the drain current falls as order of 2.

Part 3. Body Effect

(1) V_{GS} vs V_B (NMOS)

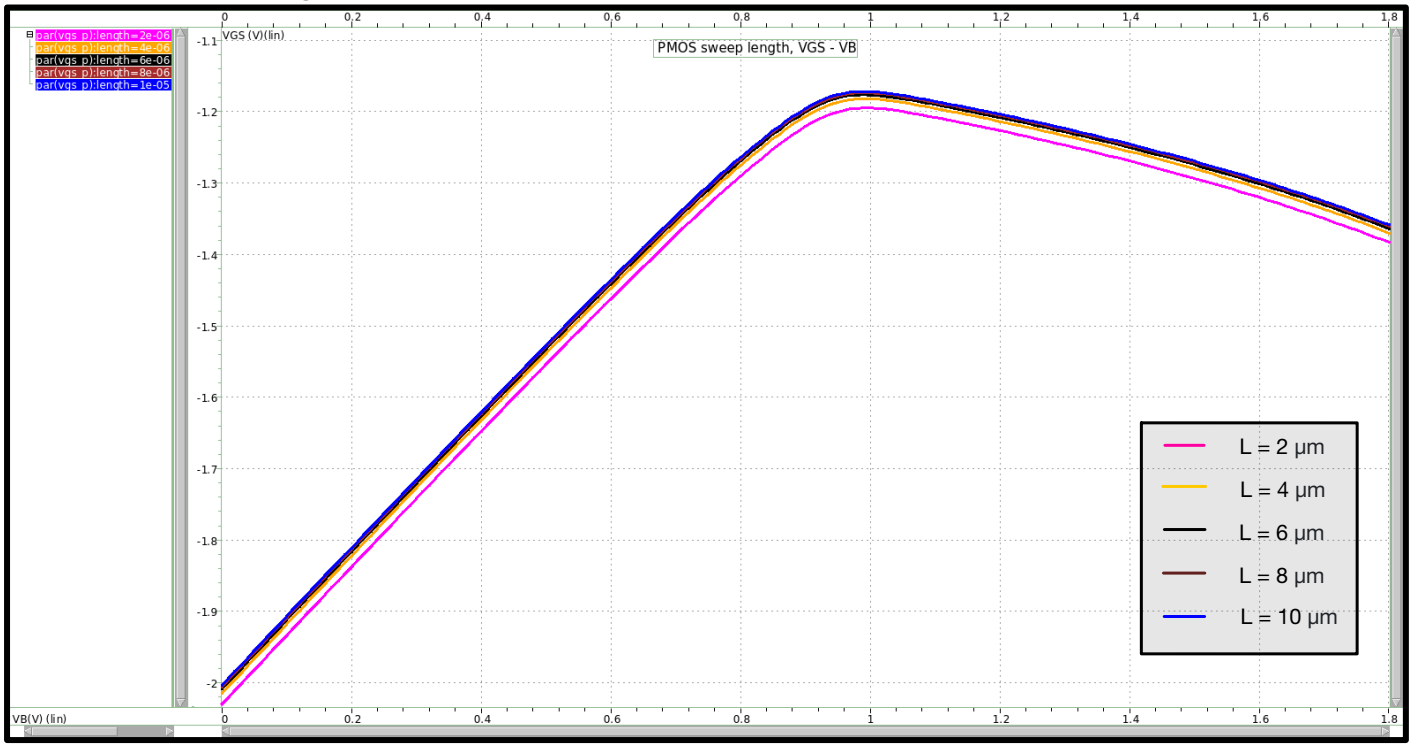
Gate-Source voltage (V)



Bulk Voltage (V)

(2) V_{GS} vs V_B (PMOS)

Gate-Source voltage (V)



Bulk Voltage (V)

Comment:

In both NMOS and PMOS cases I observed that MOS with smaller channel length has larger $|V_{GS}|$ throughout the sweeping V_B. The curves look like a boomerang, there is a turning point of the curve which the point is the minimum $|V_{GS}|$ (V_B = 780 mV for the NMOS and V_B = 994 mV for the PMOS)

While sweeping V_B in $0 - 0.8V$ for NMOS and $1V - 1.8V$ for PMOS, both two region displays similar traits, $|V_{GS}|$ drops as V_B approaches to turning point of each graph. This implies that either V_s increases or V_G decreases, but since the source is at the vicinity of the bulk so I think that the effect on the Source is the reason on this effect. More speculation will be that the source bulk junction tend to stay in reverse biased so that as bulk voltage increases, the source voltage reacts to it, causing $|V_{GS}|$ to drop.

Credits: The following part is contributed by brainstorming from EE23 108011244 王瑭毅, after discussing with him, we both lead to a conclusion that the explanation makes sense.

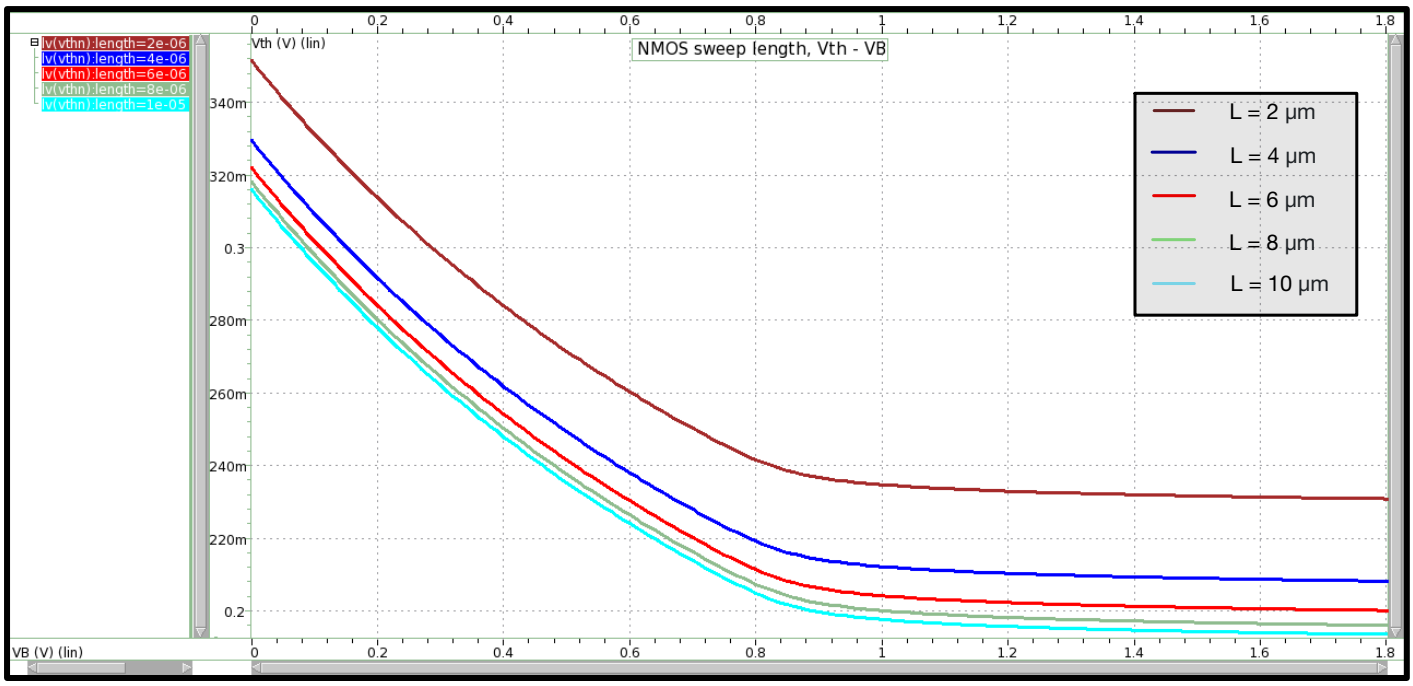
After both graphs hits the turning point, $|V_{GS}|$ then starts to increase again, from research journal, after the bulk source junction is in forward bias, the phenomenon of leakage current is observed. So 王瑭毅 made a conclusion and a hypothesis that $|V_{GS}|$ increases to sustain the drain current. After probing the drain current of both MOS, I found out that both drain current are saturated to a constant value in each region after the turning point, so that the hypothesis makes even more sense.

Reference:

Noorfazila Kamal, Nadhira Mohamad Fauzi , “Effect Of Body Biasing On 0.13 Um CMOS Transistor”, in International Journal of Innovative Technology and Exploring Engineering (IJITEE), Dec.2019, https://www.ijitee.org/wp-content/uploads/papers/v9i2/B7817129219.pdf

(3) V_{TH} vs V_B (NMOS)

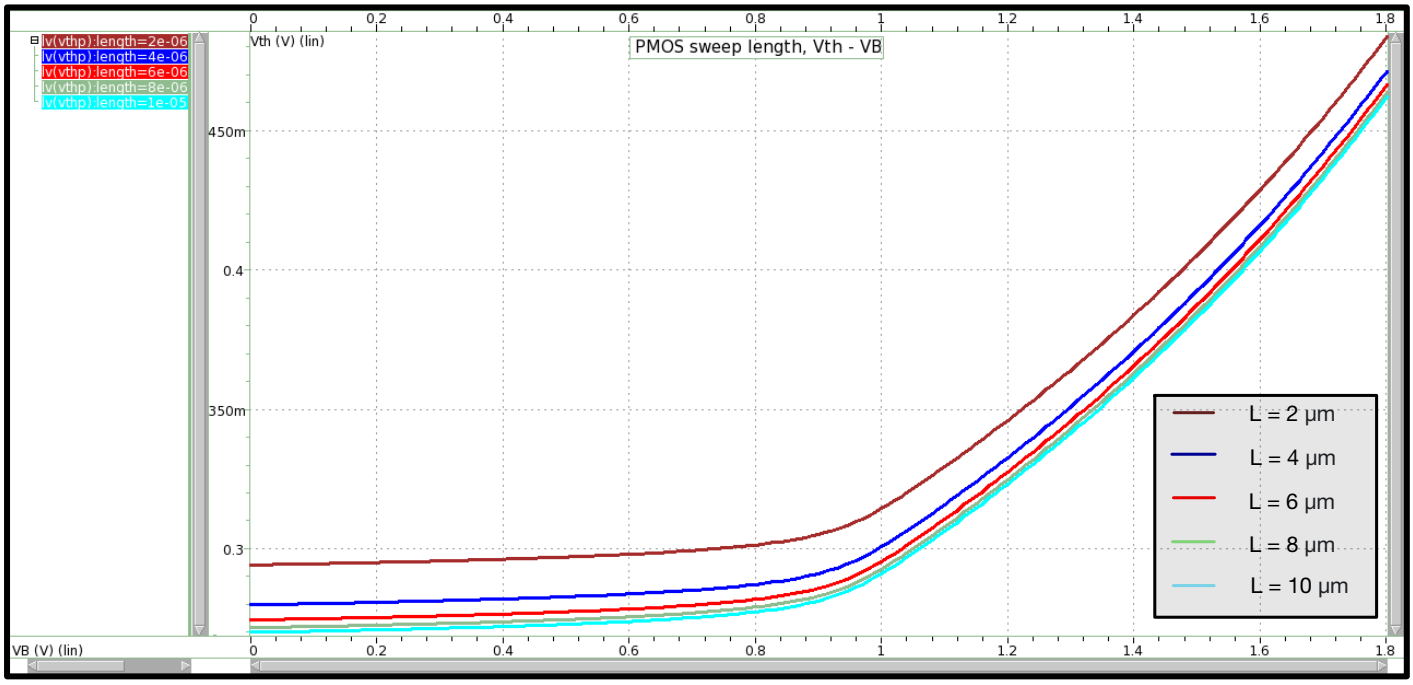
Threshold voltage (V)



Bulk Voltage (V)

(4) V_{TH} vs V_B (PMOS)

Threshold voltage (V)



Bulk Voltage (V)

Comment:

For both NMOS and PMOS cases, MOS with smaller channel length has larger absolute value of threshold voltage which corresponds to the (1) of part1 where the absolute value of threshold voltage drops as the channel length increases.

For known formula of body effect

$$\text{NMOS body effect: } V_{TH,N} = V_{TH0} + \gamma\left(\sqrt{|2\phi_f + V_{SB}|} - \sqrt{2\phi_f}\right)$$

$$\text{PMOS body effect: } V_{TH,P} = V_{TH0} + \gamma\left(\sqrt{|2\phi_f + V_{BS}|} - \sqrt{2\phi_f}\right)$$

From the formula, as the bulk voltage increases, V_{SB} decreases for NMOS, so the total threshold voltage drops, which we could see from the graph that the threshold voltage drops as bulk voltage increases.

Also, from the formula, as the bulk voltage increases, V_{BS} increases for PMOS, so the total threshold voltage rises, which we could also see from the graph that the threshold voltage rises as bulk voltage increase.

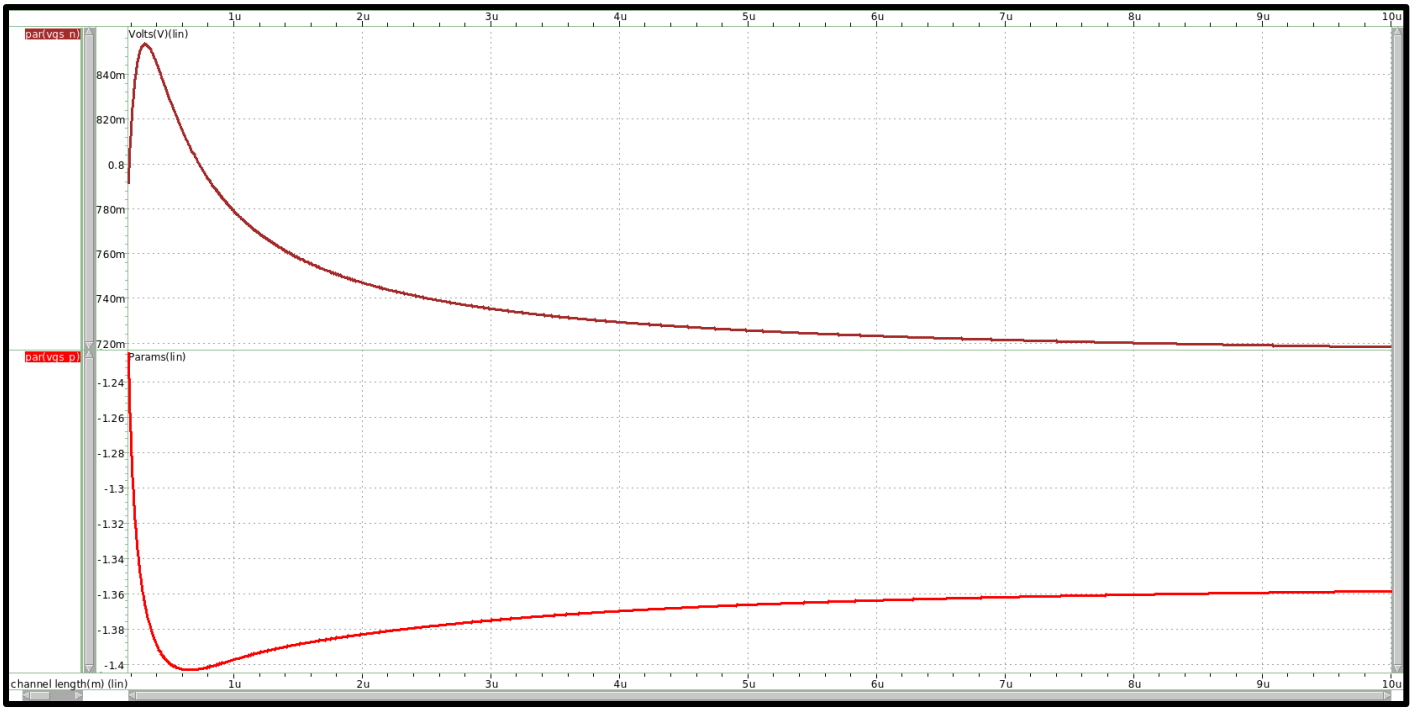
But one thing to notice is that NMOS doesn't keep a linear drop relation all along with increasing the bulk voltage, the body effect seems to be "saturated" after a specific bulk voltage. And for the PMOS, the threshold voltage doesn't increase immediately after adding the bulk voltage, instead it increases after the bulk voltage reaches a specific value.

For the NMOS case, the threshold voltage drops with an approximate rate of $\frac{-137\ mV\ (V_{TH})}{1\ V\ (Bulk\ voltage)}$ as bulk voltage increases for all the 5 sweeping channel length, but after the bulk voltage approaches 0.8V, then the threshold voltage started to converge to a value. (5 different value for 5 distinct length respectively).

For the PMOS case, the threshold voltage remains the same (or without significant change) when bulk voltage is below 0.8V for all 5 of the sweeping channel lengths, but after bulk voltage is larger than 0.8 V, then the threshold voltage starts to increase with a rate of $\frac{182\ mV\ (V_{TH})}{1\ V\ (Bulk\ voltage)}$.

Additional probe

V_{GS} throughout the sweeping length



Drain current of diode connected MOS (sweep length, VGS-VB)