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電機23
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EE3235 Analog Integrated Circuit Analysis and Design I

Homework 2

Elementary Gain Stages

Due date: 2021.10.27 (Wed.) 13:20 (upload to eeclass system)

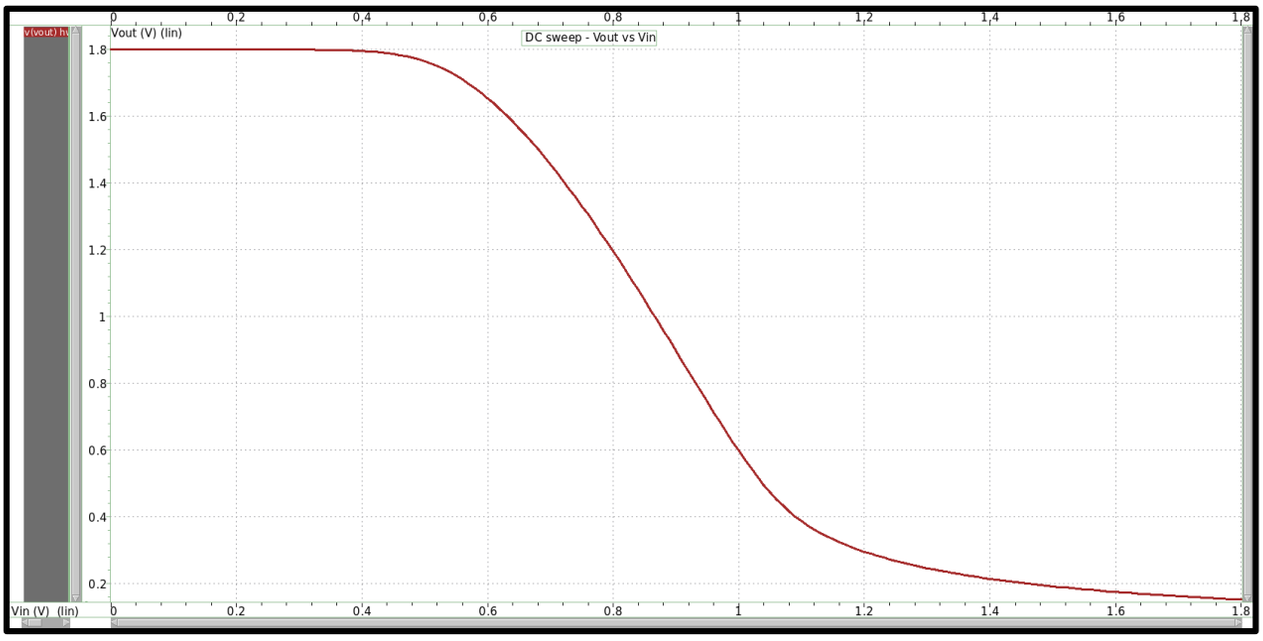
Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

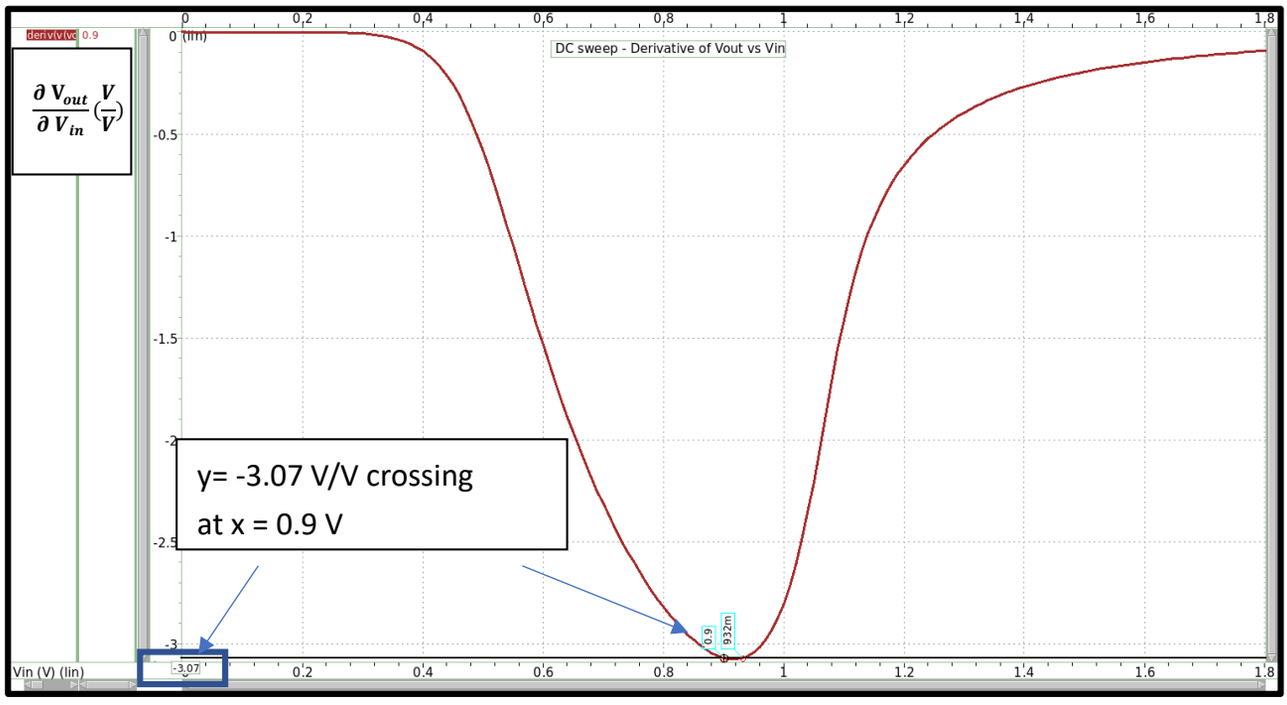
Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

Part 1 – Common Source Amplifier

(1) DC sweep






```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vout_derivative=  -3.0694
 **info** dc convergence successful at Newton-Raphson method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
 ******
```

Comment:

I acquired the derivative of V_{out} with respect to V_{in} where V_{in} = 0.9 V is -3.07 from the probe and -3.0694 from the .lis file, this is because the cursor from custom waveview rounds it to less decimal place.

(2) TF Analysis

```
****     small-signal transfer characteristics

     v(vout)/vin                                =   -3.0731
     input resistance at              vin       =  1.000e+20
     output resistance at v(vout)               =   16.3742k
```

Comment:

The values are close where the relative error is $\left|\frac{-3.0731-(-3.0694)}{-3.0694}\right| = 0.12\%$， the reason that the results are similar is because the biased voltage is close to the probing voltage. Also, the meaning of derivative of V_{out} with respect to V_{in} is for given small input change at bias point, the value indicates how output change respond to the small change, which is the definition of gain.

(3) Hand Calculation and Discussion

```
**** mosfets

subckt
element  0:ms
model    0:n_18.1
region   Saturation
 id        48.8227u
 ibs      -1.948e-20
 ibd      -103.2106a
 vgs       900.0000m
 vds       896.7792m
 vbs         0.
 vth       490.0856m
 vdsat     326.7695m
 vod       409.9144m
 beta      658.9948u
 gam eff   507.4507m
 gm        187.8304u
 gds         7.0231u
 gmb        29.1442u
 cdtot     878.3203a
 cgtot       1.4683f
 cstot       2.0675f
 cbtot       1.7458f
 cgs         1.1263f
 cgd       217.6025a
```

```
**** resistors

subckt
element  0:rd
 r value    18.5000k
 v drop    903.2208m
 current    48.8227u
 power      44.0977u
```

TABLE I

COMMON SOURCE PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.9V	0.9V	0.9V
$V_{out,DC}$	0.9V	0.8968 V	0.89678 V
Gain A_V	> 2.8 (V/V)	3.0731 V/V	3.07529 V/V
R_D	< 100KΩ	18.5 kΩ	-
I_D	< 50μA	48.8227 μA	-
M_S W/L, m	-	$\frac{0.6\mu m}{0.3\mu m}$, m = 1	-

From .lis file, $g_{ds} = 7.0231\ \mu S$ indicating that $r_o = \frac{1}{7.0231\times10^{-6}} = 142387.2649\ \Omega$

DC Gain

DC Gain for common source amplifier is $A_v = -g_m(r_0 || R_D) = 187.8304 \times 10^{-6}(18500||142387.2649) = -3.07529\ V/V$

The relative error of DC gain between hand calculation and design is $\left|\frac{-3.07529-(-3.0731)}{-3.0731}\right| = 0.07\%$ which is almost identical.

$V_{out,DC}$

The Drain-Source Voltage is

$V_{DS} = V_{DD} - I_D R_D = 1.8 - 48.8227 \times 10^{-6} \times 18500 = 0.89678\ \text{V}$

The relative error of $V_{out,}$ DC between hand calculation and design is $\left|\frac{0.89678-0.8967792}{0.8967792}\right| = 8.921 \times 10^{-5}\ \%$ which is almost identical.

Output resistance

The output resistance from the transfer function is $16.3742\ k\Omega$

And the hand calculate value is $(18500||142387.2649) = 16.37273\ k\Omega$

The relative error of Output resistance between hand calculation and design is $\left|\frac{16.3727\ k - 16.3742k}{16.3742\ k}\right| = 9.16075 \times 10^{-5}\ \%$ which is almost identical.

Other operating point information

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vdd     =   1.8000  0:vin     = 900.0000m 0:vout    = 896.7792m
+0:vss     =   0.


maximum nodal capacitance=   3.813E-15         on node     0:vss

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vdd     =   0.      0:vin     =   1.4683f 0:vout    = 878.3203a
+0:vss     =   3.8132f



**** voltage sources

subckt
element  0:vin      0:vdd      0:vss
 volts    900.0000m    1.8000     0.
 current    0.       -48.8227u   -6.1093a
 power      0.        87.8809u    0.

    total voltage source power dissipation=   87.8809u       watts
```

Comment:

The relative error of all kinds of variables are negligible for the common source amplifier, this indicates that the small signal model of the common source amplifier from the textbook is a great approximation for the real situation.

(設計過程在下一頁)

Comment and Discussion:

First, I need to know what goals and what condition I need to meet the SPEC.

From formula: $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$

$V_{out} = 1.8 - I_D R_D$ and gain $\cong g_m(r_o \,||\, R_D)$

I supposed that when drain current is precisely $50\mu A$ and $V_{out}\ is\ biased\ at\ 0.9\,V$, then I got $R_D = 18\ k\Omega$, considering that the drain current should be smaller, so I set $R_D = 18.5\ k\Omega$.

Then I use $\frac{5\mu m}{0.18\mu m}$ a common value seen in textbook as testing aspect ratio to test the $\mu_n C_{ox}\frac{W}{L}$, I acquired beta = 9.7885×10^{-3}, and drain current equals to $597.8761\ \mu A$.

Then I have to lower the aspect ratio, to neglect channel length modulation, I make the length larger approaching to width while adjusting the aspect ratio, so I make $L = 0.18 \times 15 = 2.7\ \mu m$ where I projected the $I_D = \frac{597.8761}{15} = 39.85\ \mu A$, but the value is $63.505\ \mu A$ causing the NMOS in linear region and doesn't meet the SPEC.

Then, the previous homework reminded me that with longer channel length there exists RSCE, so the threshold voltage drops, therefore the drain current still increases because V_{TH} is in the parentheses of a square order. From previous homework, SCE exists in channel lengths from $180nm\ to\ 300nm$ so I select $300nm$ as my channel length and channel width to be $\frac{5\mu m}{2.7\mu m} \times 300nm = 556\ nm$, so I select $600nm$ to make the aspect ratio equals to 2, an integer value. Then it meets the SPEC where

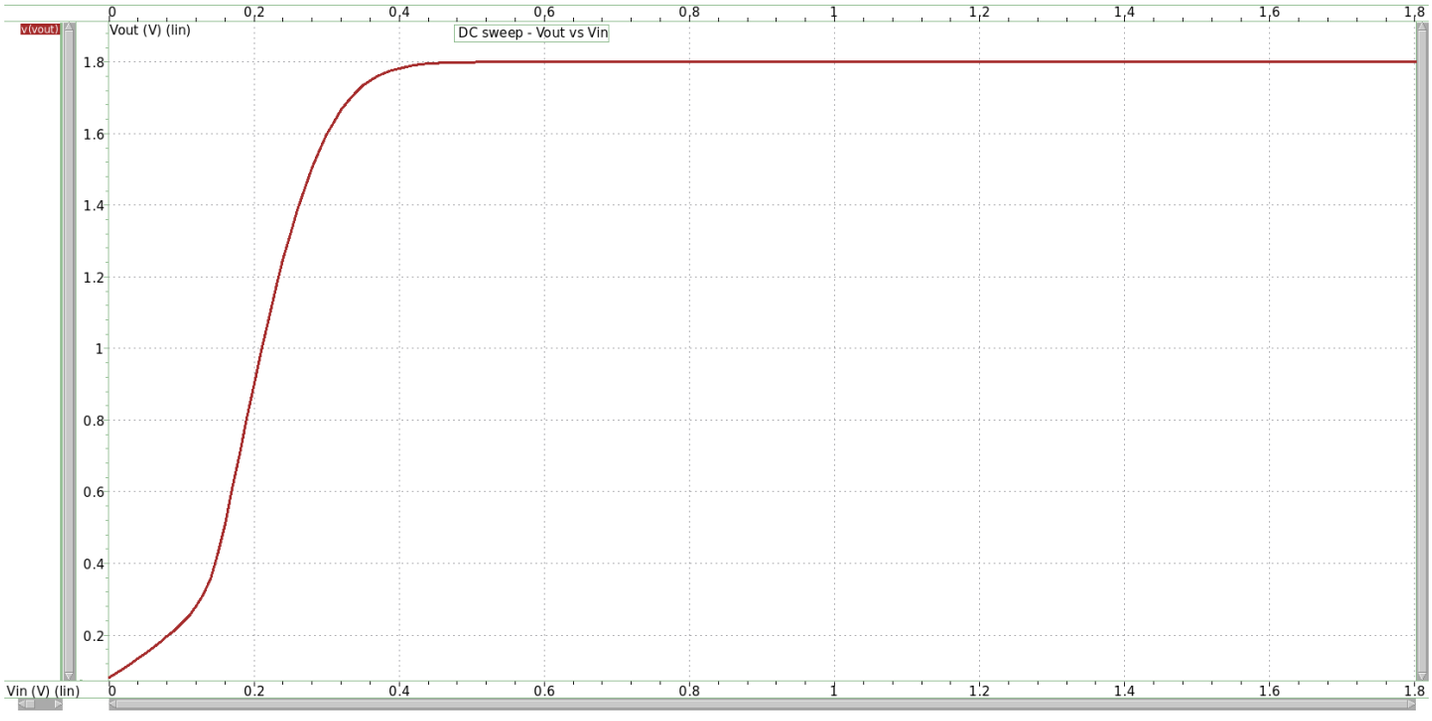
$|A_V| = |-3.0731| = 3.0731\frac{V}{V},\ I_D = 48.8227\mu A\ ,\ R_D = 18.5\ k\Omega,\ V_{DS} = 896.7792\ mV$

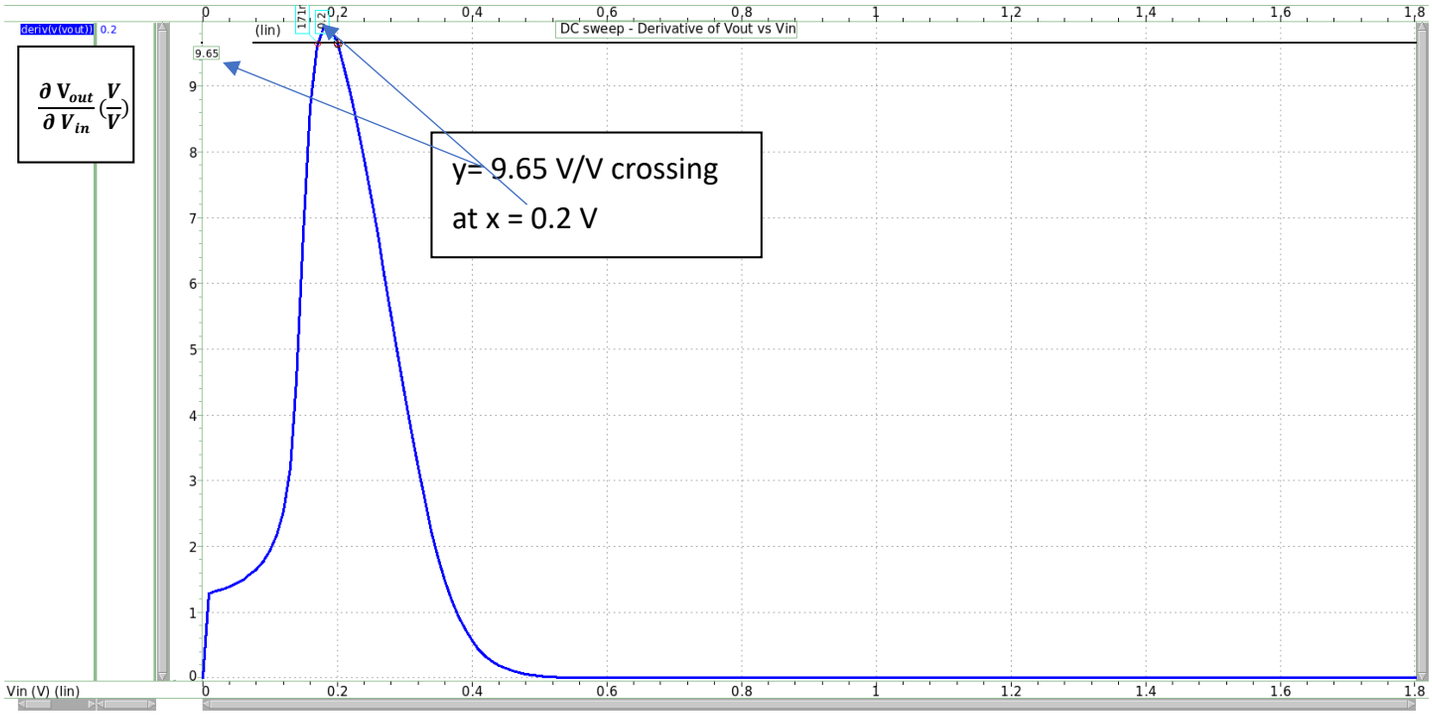
Since the drain current is a little close to the limit, so I try to lower the aspect ratio, so I set the W to $550\ nm$ and the drain current drops to $45.2094\mu A$, so I set $R_D = 20\ k\Omega$.
But the gain then drops to 3.0583 V/V, I then again set W = $500\ nm$ and $R_D = 21.5\ k\Omega$. The current then drops to $41.7170\mu A$ and the gain drops to 3.0146 V/V.
(Both adjustments meet the SPEC)

Trade-offs can be observed throughout the simulation, first I have to decrease my size to make the device in the RCE region. This needs to be supported by advanced technology. And then to achieve smaller drain current, it would impact my gain. So that the tradeoffs of power consumption and gain performance is then observed. If the company is asking for stable and limited power consumption, I would choose the latter case. But since there is no special notification on this design, so I will stick to the original design where a better gain performance is acquired.

Part 2 – Common gate

(1) DC sweep






```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vout_derivate=   9.6509
**info** dc convergence successful at Newton-Raphson method
1****** PrimeSim HSPICE -- R-2020.12-SP2 linux64 (May 24 2021 7074677) ******
 ******
```

Comment:

The derivative I acquired from probing and .lis file are almost the same, the only difference is the rounding figures, same as last part.

(2) TF Analysis

```
****     small-signal transfer characteristics

     v(vout)/vin                               =     9.4951
     input resistance at             vin       =    10.3737k
     output resistance at v(vout)              =    81.4848k
```

Comment:

The values are close where the relative error is $\left|\frac{-9.4951-(-9.6509)}{-9.6509}\right| = 1.61\%$， the reason that the results are similar is because the biased voltage is close to the probing voltage. Also, the meaning of derivative of V_{out} with respect to V_{in} is for given small input change at bias point, the value indicates how output change respond to the small change, which is the definition of gain.

(3) Hand Calculation and Discussion

```
**** mosfets

subckt
element  0:mb
model    0:n_18.1
region   Saturation
 id         9.1196u
 ibs       -27.2565a
 ibd      -122.8729a
 vgs       650.0000m
 vds       701.7212m
 vbs      -200.0000m
 vth       510.7269m
 vdsat     159.5498m
 vod       139.2731m
 beta      737.1800u
 gam eff   512.7680m
 gm         99.2682u
 gds         2.1205u
 gmb        15.1695u
 cdtot       1.2603f
 cgtot       2.7191f
 cstot       3.4299f
 cbtot       2.4985f
 cgs         2.1761f
 cgd       323.8626a
```

```
**** resistors

subckt
element  0:rd
 r value    98.5000k
 v drop    898.2788m
 current     9.1196u
 power       8.1919u
```

TABLE II

COMMON GATE PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.2V	0.2V	0.2V
$V_{out,DC}$	0.9V	0.90172 V	0.90172 V
Gain A_V	> 8.5 (V/V)	9.4951 V/V	8.0885 V/V
R_D	< 100KΩ	98.5 kΩ	-
I_D	< 50μA	9.1196 μA	-
V_b	-	0.85 V	-
M_b W/L, m	-	0.9μm / 0.4μm , m=1	-

From .lis file, $g_{ds} = 2.1205\ \mu S$ indicating that $r_o = \frac{1}{2.1205\times10^{-6}}$

$$= 471586.89\Omega$$

DC Gain

DC Gain for common gate amplifier is $A_v = g_m(r_o \,||\, R_D)$

$= 99.2682 \times 10^{-6}\ (471586.89 \,||\, 98500\ ) \cong 8.0885\ \text{V/V}$

The relative error of the DC gain between hand calculation and design is

$\left|\frac{8.0885-9.4951}{9.4951}\right| = 14.81\%$, which a significant difference can be noticed.

$V_{out,DC}$

$V_{out,DC} = V_{DD} - I_D R_D = 1.8 - 9.1196 \times 10^{-6} \times 98500$

$= 0.90172\ V$

The relative error of $V_{out,DC}$ is $\left|\frac{0.90172-(0.2+0.7017212)}{(0.2+0.7017212)}\right| = 1.3 \times 10^{-4}\ \%$,

which is almost identical between both values.

I/O impedance

$$R_{in} = \frac{r_o + R_D}{1 + g_m r_o} = \frac{471586.89 + 98500}{1 + 99.2682 \times 10^{-6} \times 471586.89}$$

$= 11923.12\ \Omega$

$R_{out} = (r_o \,||\, R_D) = 81481.1\Omega$

The relative error of $R_{in} = \left|\frac{11923.12-10373.7}{10373.7}\right| = 14.94\%$

And the relative error of $R_{out} = \left|\frac{81481.1-81484.8}{81484.8}\right| = 4.537 \times 10^{-3}\ \%$

The input impedance like the DC gain has a relative error around 15%, while the output impedances are almost identical for both value.

With body voltage connected to source voltage (一開始做錯)

```
**** mosfets

subckt
element  0:mb
model    0:n_18.1
region   Saturation
 id          9.3793u
 ibs      -2.667e-21
 ibd      -105.1954a
 vgs       600.0000m
 vds       699.5858m
 vbs         0.
 vth       474.4421m
 vdsat     147.0031m
 vod       125.5579m
 beta      902.9562u
 gam eff   507.4464m
 gm        109.5748u
 gds         2.1864u
 gmb        19.8498u
 cdtot       1.5667f
 cgtot       3.3342f
 cstot       4.3200f
 cbtot       3.2210f
 cgs         2.6664f
 cgd       398.1024a
```

```
**** resistors

subckt
element  0:rd
 r value    96.0000k
 v drop    900.4142m
 current     9.3793u
 power       8.4453u
```

TABLE II

COMMON GATE PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.2V	0.2V	0.2V
$V_{out,DC}$	0.9V	0.89959 V	0.89959 V
Gain A_V	> 8.5 (V/V)	8.8659 V/V	8.6943 V/V
R_D	< 100KΩ	96 kΩ	-
I_D	< 50μA	9.3979 μA	-
V_b	-	0.8 V	-
M_b W/L, m	-	$\frac{1.1\mu m}{0.4\mu m}$, m = 1	-

From .lis file, $g_{ds} = 2.1864\ \mu S$ indicating that $r_o = \frac{1}{2.1864\times10^{-6}}$

$$= 457372.8503\ \Omega$$

DC Gain

DC Gain for common gate amplifier is $A_v = g_m(r_o\ ||\ R_D)$

$= 109.5748 \times 10^{-6}\ (457372.8503\ ||\ 96000\ ) \cong 8.6943\ \text{V/V}$

The relative error of the DC gain between hand calculation and design is

$\left|\frac{8.6943-8.8659}{8.8659}\right| = 1.93\%$, which a small difference can be noticed.

$V_{out,DC}$

$V_{out,DC} = V_{DD} - I_D R_D = 1.8 - 9.3793 \times 10^{-6} \times 9600$

$= 0.8995872\ V$

The relative error of $V_{out,DC}$ is $\left|\frac{0.8995872-(0.2+0.6995858)}{(0.2+0.6995858)}\right| = 1.556 \times 10^{-4}$ %, which is almost identical between both values.

I/O impedance

$$R_{in} = \frac{r_o + R_D}{1 + g_m r_o} = \frac{457372.8503 + 96000}{1 + 109.5748 \times 10^{-6} \times 457372.8503}$$

$= 10825.71\ \Omega$

$R_{out} = (r_o\ ||\ R_D) = 79345.7677\Omega$

The relative error of $R_{in} = \left|\frac{10825.71-10828}{10828}\right| = 0.02\%$

And the relative error of $R_{out} = \left|\frac{79345.76677-79349.2}{79349.2}\right| = 4.326 \times 10^{-3}$ %

The I/O impedance between both values are almost identical

Other operating point information

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vb      = 850.0000m 0:vdd     =   1.8000  0:vin     = 200.0000m
+0:vout    = 901.7212m 0:vss     =   0.


maximum nodal capacitance=   3.430E-15         on node     0:vin

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vb      =   2.7191f 0:vdd     =   0.      0:vin     =   3.4299f
+0:vout    =   1.2603f 0:vss     =   0.


**** voltage sources

subckt
element  0:vin      0:vb       0:vdd      0:vss
 volts    200.0000m  850.0000m    1.8000     0.
 current    9.1196u    0.        -9.1196u   -1.1020p
 power     -1.8239u    0.        16.4152u    0.

    total voltage source power dissipation=   14.5913u       watts
```

Comment:

By observation, for NMOS that its body is grounded, the parameters calculated from small signal model related to g_m has large difference comparing to the simulation. Meanwhile, the NMOS that its body is connected to source has negligible difference between the parameters. This result can conclude that the existence of body effect will impact the small signal model especially g_m.

From calculation, I find out that g_m is the reason that causes the gain to be smaller and the input impedance to be larger, the small signal model of common gate amplifier with body effect should have adjustment on the g_m part where the total transconductance should be larger. This suggests that when there is body effect, body conductance should be considered as a factor of boosting total transconductance in common gate amplifier.

經過同學已知有了 Body effect 後的 small signal parameter

$$A_V = (g_m + g_{mb} + g_{ds})(R_D \,//\, r_o) = (99.2682 + 15.165 + 2.1205)\times 10^{-6}\,(98.5\times 10^3\,\Omega \,//\, 471586.89\,\Omega)$$

$$= 9.4969$$

relative error $\left|\frac{9.4969 - 9.4951}{9.4951}\right| = 0.019\% \Rightarrow$ becomes identical

$$R_{in} = \frac{r_o + R_D}{(g_m + g_{mb})\,r_o + 1} = \frac{471586.89 + 98500}{1 + (99.2682 + 15.165)\times 10^{-6} \times 471586.89} = 10371.78$$

relative error $\left|\frac{10371.78 - 10373.7}{10373.7}\right| = 0.019\% \Rightarrow$ becomes identical

Comment and Discussion

At first, I use aspect ratio $\frac{W}{L} = \frac{0.36\ \mu m}{0.18\ \mu m}$ and a large resistor first, since I need a large gain. Then I had drain current of $12\ \mu A$, but the gain is only around 3.

First Trial				
W/L	RD	VB		
0.36u/0.18u	75k	0.8		
ID	gds	beta	gm	Vth
12.1364	5.6269u	726.2551u	108.5494u	450.3757m

Then I think that I have to increase r_o so that the output resistance will be dominated by the drain resistor. I shift the same ratio but larger L, since from last homework a larger channel length gives smaller output conductance which makes r_o become larger and the gain got closer

third Trial							
W/L	RD	VB					
1.2u/0.6u	89k	0.81					
ID	gds	beta	gm	Vth		gain	vds
10.2188u	1.4825u	636.5166u	97.9919u	437.0727m		7.8198	690.5309

But still the gain is not over the expected value, so I think that I have to increase drain resistor and decrease drain current, but after trying lowering down the channel width and increasing drain resistance, I still can't achieve the gain.

So I think that I have to boost up g_m , but I still need small drain current, then it reminded me that the drain current is affected by V_{TH} by order of 2 but g_m is only affected by order of one, so I can increase the aspect ratio and increase V_{TH}, so that I get a great boost of g_m but a less boost of drain current to sustain the $I_D R_D$ at around 0.9 V. After some trials I achieved the goal.

sixth Trial							
W/L	RD	VB					
1.1u/0.4u	96k	0.8					
ID	gds	beta	gm	Vth		gain	vds
9.3793u	2.1864u	902.9562u	109.5748u	474.4421m		8.8659	699.5858

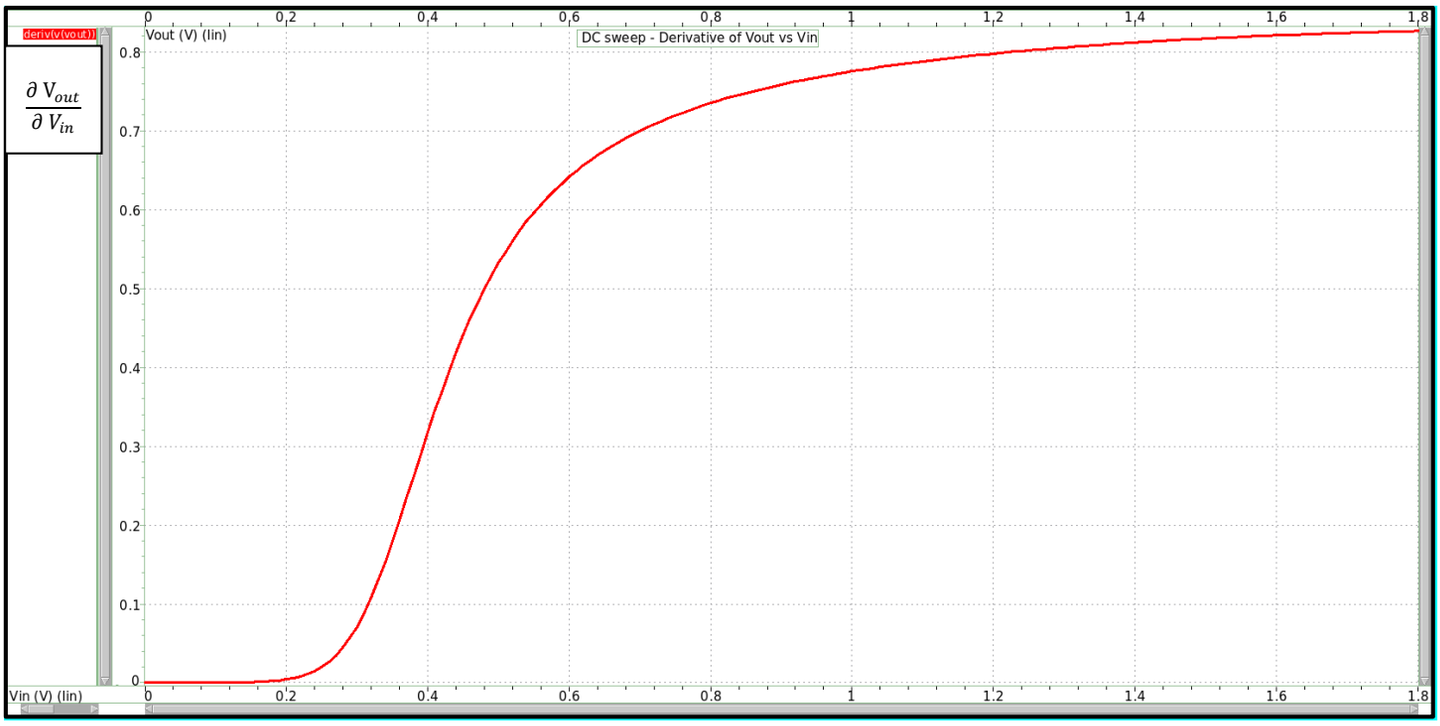
Then, I find out that the requirement for the homework is to keep the body of NMOS to ground, which I connected to the source at first, switching body voltage to ground causes V_{SB} become larger. Therefore, V_{TH} rises. This gives me some space to shift up the gate voltage, and then I can use this opportunity to size down my device. Eventually, I stick for $V_B = 0.85\ V,\quad \frac{W}{L} = \frac{0.9\ \mu m}{0.4\ \mu m}\ ,\ R_D = 98.5\ k\Omega$ where it meets the SPEC.

My design to me is still considered large since the channel length is 5 times of $0.18\ \mu m$. The resistance of drain resistor is quite large, this could cause more noise to the device, leakage current will also affect the output. But the good thing is my drain current is low, so the power consumption is low.

Common gate design let me find out that meeting an ideal SPEC often leads me to extreme value, in this case is large resistor and small drain current, but in real life, both should be avoided to create a dependable machine.

Part 3 - Source Follower

(1) DC sweep



Comment:

As input DC voltage becomes larger, the derivative of V_{out} with respect to V_{in} becomes larger, this indicates that the change of small signal input creates larger output change when the input DC voltage is biased at higher voltage. So, my design for smaller DC biased stage doesn't display the use for source follower where we need a unity gain. Also, the derivative growth become less steep after the input voltage is larger than 1.4V, we need the input bias stage to be larger than this voltage to make sure that the gain remains a constant.

(2) TF Analysis

```
****     small-signal transfer characteristics

     v(vout)/vin                              =  821.1060m
     input resistance at            vin       =  1.000e+20
     output resistance at v(vout)             =    9.5953k
```

(3) Hand Calculation and Discussion

```
**** mosfets

subckt
element  0:md
model    0:n_18.1
region   Saturation
 id          7.3234u
 ibs       -97.3412a
 ibd      -194.5047a
 vgs       699.2234m
 vds       899.2234m
 vbs      -900.7766m
 vth       587.4121m
 vdsat     156.1147m
 vod       111.8113m
 beta      683.9145u
 gam eff   528.3134m
 gm         85.6094u
 gds         2.8915u
 gmb         7.6268u
 cdtot     670.5263a
 cgtot       1.0629f
 cstot       1.3954f
 cbtot       1.1668f
 cgs       801.9791a
 cgd       178.2385a
```

```
**** resistors

subckt
element  0:rs
 r value   123.0000k
 v drop    900.7766m
 current     7.3234u
 power       6.5967u
```

TABLE III

SOURCE FOLLOWER PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	1.6V	1.6V	1.6V
$V_{out,DC}$	0.9V	0.90078 V	0.90078 V
Gain A_V	> 0.8 (V/V)	0.8211 V/V	0.8859 V/V
R_S	< 150KΩ	123 kΩ	-
I_D	< 30μA	7.3234 μA	-
M_d W/L, m	-	$\frac{0.5\mu m}{0.25\mu m}$, m=1	-

From .lis file, $g_{ds} = 2.8915$ μS indicating that $r_o = \frac{1}{2.8915 \times 10^{-6}}$

$= 345841.26\ \Omega$

DC Gain

DC gain for source follower is $A_v = \frac{r_o \,||\, R_S}{\frac{1}{g_m} + r_o \,||\, R_S} = 0.885942$ V/V

The relative error of DC gain between hand calculation and design is

$\left|\frac{0.885942 - 0.8211060}{0.8211060}\right| = 7.89\%$. which exists a significant difference where the hand calculated value is unexpectedly larger.

$V_{out,DC}$

$$V_{out,DC} = I_D R_S = 7.3234 \times 10^{-6} \times 1230000 = 0.9007782\ V$$

The relative error between hand calculation and design is

$\left|\frac{0.9007782 - 0.9007766}{0.9007766}\right| = -1.776 \times 10^{-4}\%$. Which is almost identical.

Output Impedence

R_{out} for source follower is $\frac{1}{g_m} \,||\, r_o \,||\, R_s =$

$$\frac{1}{85.6094 \times 10^{-6} + 2.8915 \times 10^{-6} + \frac{1}{123000}} = 10348.65\ \Omega$$

The relative error between hand calculation and design is

$\left|\frac{10348.65 - 9595.3}{9595.3}\right| = 7.85\%$ which exists a difference just like the DC gain where it is unexpectedly larger where the relative error is around 8%.

With body voltage connected to source voltage(一開始做錯)

```
**** mosfets

subckt
element  0:md
model    0:n_18.1
region   Saturation
 id        11.2505u
 ibs      -5.057e-21
 ibd       -97.2445a
 vgs       699.9589m
 vds       899.9589m
 vbs         0.
 vth       471.9536m
 vdsat     222.3949m
 vod       228.0053m
 beta      405.2284u
 gam eff   507.4472m
 gm         82.1898u
 gds         1.7514u
 gmb        14.0114u
 cdtot     749.4013a
 cgtot       1.5168f
 cstot       2.0429f
 cbtot       1.5749f
 cgs         1.2087f
 cgd       180.7153a
```

```
**** resistors

subckt
element  0:rs
 r value    80.0000k
 v drop    900.0411m
 current    11.2505u
 power      10.1259u
```

TABLE III

SOURCE FOLLOWER PERFORMANCE TABLE

Working Item	SPEC	Your Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	1.6V	1.6V	1.6V
$V_{out,DC}$	0.9V	0.90004 V	0.90004 V
Gain A_V	> 0.8 (V/V)	0.8522 V/V	0.8522 V/V
R_S	< 150KΩ	80 kΩ	-
I_D	< 30μA	11.2505 kΩ	-
M_d W/L, m	-	$\frac{0.5\mu A}{0.4\mu A}$, m = 1	-

From .lis file, $g_{ds} = 1.7514$ μS indicating that $r_o = \frac{1}{1.7514 \times 10^{-6}}$

$= 570971.794\ \Omega$

DC Gain

DC gain for source follower is $A_v = \frac{r_o \,||\, R_S}{\frac{1}{g_m} + r_o \,||\, R_S} = 0.8522271$ V/V

The relative error of DC gain between hand calculation and design is

$\left|\frac{0.8522271 - 0.8521810}{0.8521810}\right| = 0.11\%$. which is almost identical

$V_{out,DC}$

$V_{out,DC} = I_D R_S = 11.2505 \times 10^{-6} \times 80000 = 0.90004$ V

The relative error between hand calculation and design is

$\left|\frac{0.90004 - 0.9000411}{0.9000411}\right| = -1.2222 \times 10^{-6}$. Which is almost identical too.

Output Impedence

R_{out} for source follower is $\frac{1}{g_m} \,||\, r_o \,||\, R_s =$

$\frac{1}{82.1898 \times 10^{-6} + 1.7514 \times 10^{-6} + \frac{1}{80000}} = 10369.01\ \Omega$

The relative error between hand calculation and design is

$\left|\frac{10369.01 - 10372.8}{10372.8}\right| = 0.04\%$. Which is almost identical too.

Other operating point information

```
****** operating point information tnom=  25.000 temp=  25.000 ******
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vdd     =   1.8000  0:vin     =   1.6000  0:vout    = 900.7766m
+0:vss     =   0.


maximum nodal capacitance=   1.395E-15         on node     0:vout

   nodal  capacitance table

   node    =    cap      node    =    cap      node    =    cap

+0:vdd     = 670.5263a 0:vin     =   1.0629f 0:vout    =   1.3954f
+0:vss     =   0.


**** voltage sources

subckt
element  0:vin      0:vdd      0:vss
 volts      1.6000     1.8000     0.
 current    0.        -7.3234u   -2.7011p
 power      0.        13.1821u    0.

    total voltage source power dissipation=   13.1821u       watts
```

Comment:

The same difference can be observed between NMOS that its body is connected to source and the one that doesn't, the difference between parameters from small signal model is negligible if there is no body effect, but an observable difference when there is body effect.

From the calculation, the gain is overvalued comparing to the simulation, this tells that $\frac{1}{g_m}$ is undervalued, which leads to g_m is overvalued in the model, so this means that g_m in the small signal model of source follower with body effect has to be adjusted to a smaller value. This suggest that the body conductance should be considered when there is body effect in source follower that it lowers the total transconductance.

經過同學已知有了 Body effect 後的 small signal parameter

$$A_v = \frac{\frac{g_m r_o R_s}{r_o}}{1 + \frac{(g_m + g_{mb}) r_o R_s}{r_o}} = \frac{85.6094 \times 10^{-6} \times 123 \times 10^3}{1 + (85.6094 \times 10^{-6} + 7.6268 \times 10^{-6}) \times 123 \times 10^3} = 0.8446\ V/V$$

relative error $\left| \frac{0.8446 - 0.8211}{0.8211} \right| = 2.86\%$ ⇒ becomes closer if considering g_{mb}

$$R_{out} = \frac{1}{\frac{1}{R_s} + g_m + \frac{1}{r_o} + g_{mb}} = \frac{1}{\frac{1}{123 \times 10^3} + 85.6094 \times 10^{-6} + 2.8915 \times 10^{-6} + 7.6268 \times 10^{-6}} = 9323.33\ \Omega$$

relative error $\left| \frac{9323.33 - 9595.3}{9595.3} \right| = 2.83\%$ ⇒ becomes closer if considering g_{mb}

Comment and Discussion

To achieved a good performance of source follower, $A_v = \frac{r_o \,||\, R_s}{\frac{1}{g_m} + r_o \,||\, R_s}$, I think I have to increase g_m so that it affects the output resistance less, but then after some trials I find out that since I need the $I_D R_S$ to be around 0.9V so that the source resistance is limited, I find out that this is not a good tradeoff, because the gain performance still relies on source resistor more.

So I set the aspect ratio close to 1 and a larger source resistance. after adjusting g_m and R_s for performance, I have reached the goal and I set for the fourth trial.

Third Trial			Dropping the W/L ratio			
W/L	RS					
0.3u/0.3u	85000					
ID	gds	beta	gm	Vth		
11.312	2.1701E-06	330.3597	7.15409E-05	456.9426		
vds	gain		ro	ro // rd	1/gm	gain by divider
895.1463	836.9044m		460808.2577	71762.75066	13978.01817	0.836973492

Fourth Trial			Increasing the W/L ratio			
W/L	RS					
0.5/0.4	80000					
ID	gds	beta	gm	Vth		
11.2505u	1.7514E-06	405.2284u	8.21898E-05	471.9536m		
vds	gain		ro	ro // rs	1/gm	gain by divider
899.9589m	852.1810m		570971.794	70168.54484	12166.95989	0.852227056

But same as last part, I originally connected the body to source, so I have to switch it to ground. But the original source is projected to be around 0.9V, so this is a significant drop, this gives me chance to size down the device, I drop down the channel length, which makes drain current larger. I made some adjustment to the source resistor, making it larger. Then I stick to $R_S = 123\ k\Omega\,,\ \frac{W}{L} = \frac{0.5\mu m}{0.25\mu m}$ which meet the SPEC.

My device has same issue as the CG stage, my source resistor is large which it can cause large noise and the unstable output if leakage current occurs. But I think that the drain current and device is size is acceptable, power consumption is low. Last but not least, regardless of the conditions above, the desired good performance of the source follower is to remain the gain approaching to unity, but what I designed is about 0.82 V/V. This isn't considered a great performance especially I didn't make my device small enough, but since I made NMOS body connected to source accidentally, with lower resistance and length increase for $\frac{0.4-0.25}{0.25} = 60\%$, gain of 0.85 V/V is acquired. But considering the fact that 60% of length increase only boost up the gain a little bit, if the device is not asking unity gain for priority, then the device of body connecting to ground that I designed is an overall better one than the device body connected to the source.