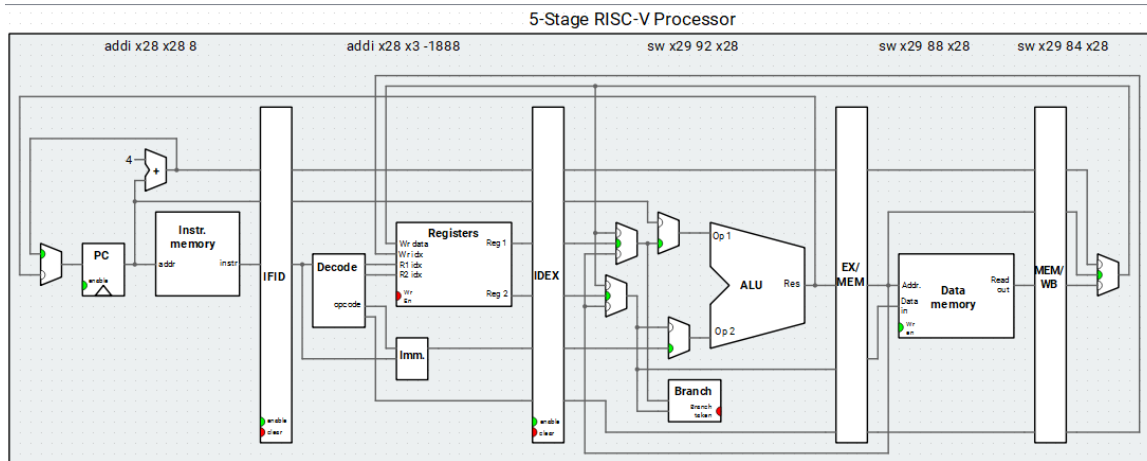
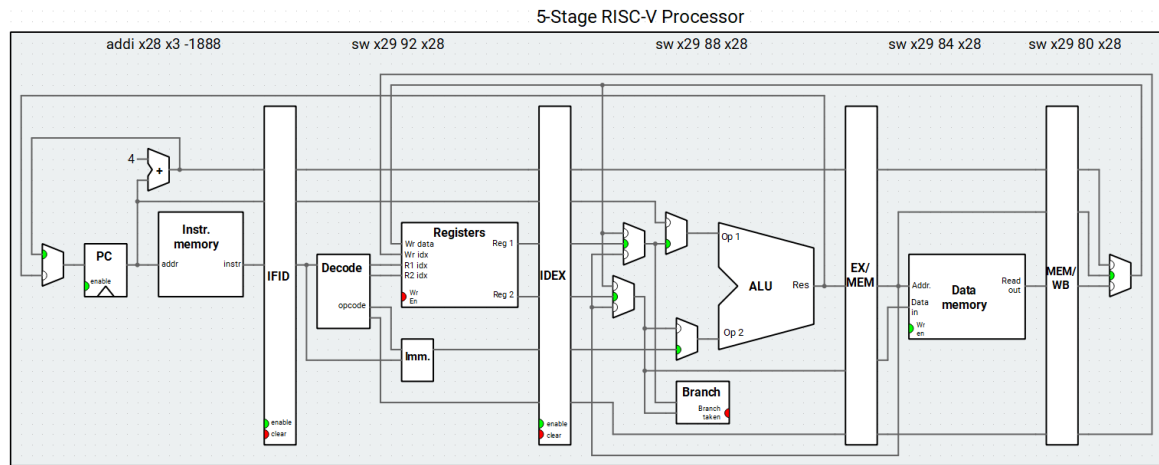


108011235 電機 23 陳昭維

When in cycle 18, all set has at least 1 way (way 0) occupied, and after the store word instruction, the set indexed by 01 has to be inserted data to another way where the tag 0x03ffffff is different from 0x0000089a. Also, the LRU of the 1st way (way 0) becomes 1 and the LRU of the 2nd way (way 1) becomes 0, indicating that the 2nd way (way 1) is the recent used way.

2. Replacement



The replacement of block with 4 way (way 0~3) occupied after the `sw x29 88 x28` instruction in EX stage pass through to MEM stage.

Access address 31 54321 0
000000000000000100010100100100

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	3	0x000008a0	0xffffffffe4	0xffffffffd8
0	1	1	2	0x000008a3	0xffffffffff	0x00000005
0	1	1	1	0x000008a4	0xffffffffff	0x00000000
0	1	1	0	0x000008a5	0xffffffffff	0x0000000c
0	1	0	3	0x000008a0	0x00000037	0xffffffffd5
1	1	1	2	0x03ffffff	0x00000000	0x00000000
1	1	1	1	0x000008a3	0xffffffffff	0x00000007
1	1	1	0	0x000008a4	0xffffffffff	0x00000000
1	1	0	3	0x0000089d	0xffffffffff	0x00000058
2	1	1	2	0x000008a2	0xffffffffff	0x00000001
2	1	1	1	0x000008a3	0xffffffffff	0x00000000
2	1	1	0	0x000008a4	0xffffffffff	0x00000000
3	1	0	3	0x0000089d	0x00000010	0xffffffffbd
3	1	1	2	0x000008a2	0xffffffffff	0x00000003
3	1	1	1	0x000008a3	0xffffffffff	0x00000000
3	1	1	0	0x000008a4	0xffffffffff	0x00000000

Cycle 53

Access address 31 54321 0
000000000000000100010100100100

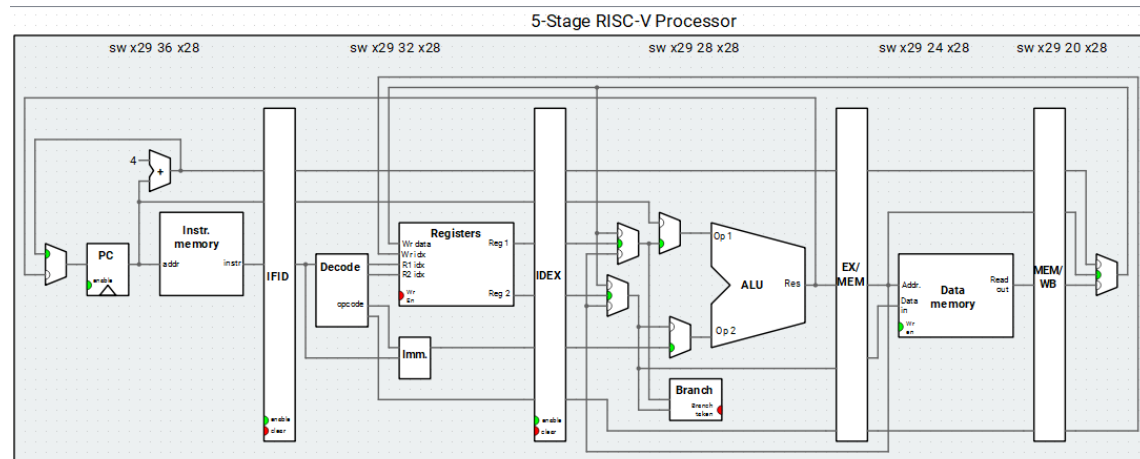
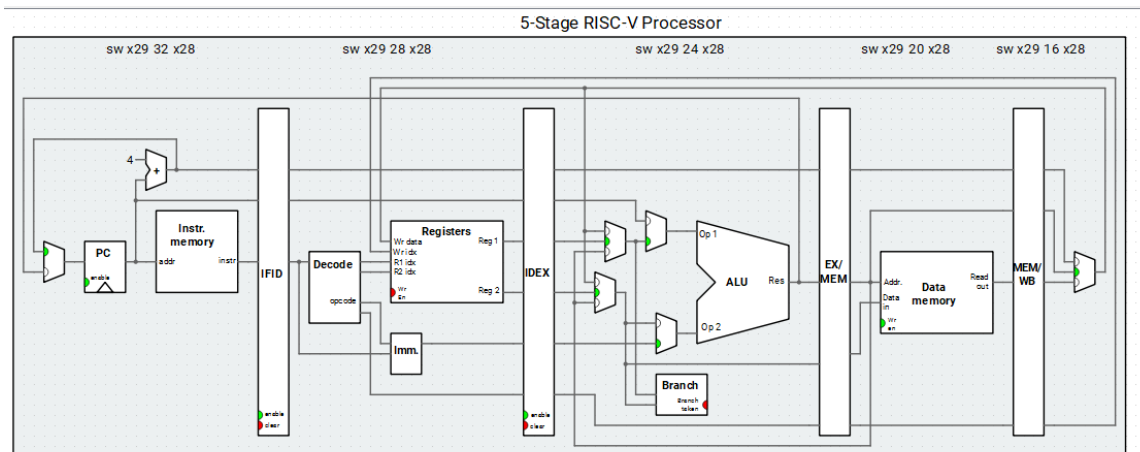
Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	3	0x000008a0	0xffffffffe4	0xffffffffd8
0	1	1	2	0x000008a3	0xffffffffff	0x00000005
0	1	1	1	0x000008a4	0xffffffffff	0x00000000
0	1	1	0	0x000008a5	0xffffffffff	0x0000000c
0	1	1	0	0x000008a5	0x00202820	0x00202920
1	1	1	3	0x03ffffff	0x00000000	0x00000000
1	1	1	2	0x000008a3	0xffffffffff	0x00000007
1	1	1	1	0x000008a4	0xffffffffff	0x00000000
1	1	0	3	0x0000089d	0xffffffffff	0x00000058
2	1	1	2	0x000008a2	0xffffffffff	0x00000001
2	1	1	1	0x000008a3	0xffffffffff	0x00000000
2	1	1	0	0x000008a4	0xffffffffff	0x00000000
3	1	0	3	0x0000089d	0x00000010	0xffffffffbd
3	1	1	2	0x000008a2	0xffffffffff	0x00000003
3	1	1	1	0x000008a3	0xffffffffff	0x00000000
3	1	1	0	0x000008a4	0xffffffffff	0x00000000

Cycle 54

The replacement of block occurs at cycle 54 when the 4 way of the 2nd set (set 1) are already occupied, but new tag 0x000008a5 occurs, so that there is block replacement where the 1st way (way 0) (whose LRU bit was 3) of the 2nd set (set 1) is replaced and the LRU becomes 0, indicating that the 1st way (way 0) is the most recently used, the LRU bit of other 3 way then are all incremented by 1.

3. Write Back

The write of the block is after the `sw x29, 24(x28)` instruction in EX stage pass through to MEM stage.



31 54321 0

address 000000000000000010001010001100100

Index V D LRU Tag Block 0 Block 1

0	1	0	1	0x0000008a0	0xffffffffe4	0xffffffffd8
0	1	1	0	0x0000008a3	0xffffffffff	0x000000005
0	0	0	3			
0	0	0	3			
1	1	0	1	0x0000008a0	0x000000037	0xffffffffd5
1	1	1	0	0x03ffffff	0x000000000	0x000000000
1	0	0	3			
1	0	0	3			
2	1	0	1	0x00000089d	0xffffffffed	0x000000058
2	1	1	0	0x0000008a2	0xffffffffff	0x000000001
2	0	0	3			
2	0	0	3			
3	1	0	1	0x00000089d	0x000000010	0xffffffffbd
3	1	1	0	0x0000008a2	0xffffffffff	0x000000003
3	0	0	3			
3	0	0	3			

cycle37

Diagram illustrating a 32-bit address and a 4x4 cache table. The address is 000000000000000010001010001101000. The cache has 4 rows and 4 columns: Index, V, D, LRU, Tag, Block 0, and Block 1. The second row (Index 1) is highlighted in red, showing a hit for Block 0 with address 0x00000006.

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	1	0x0000008a0	0xffffffe4	0xffffffd8
1	1	0	0	0x0000008a3	0xffffffff	0x00000005
2	0	0	3			
3	0	0	3			
0	1	0	2	0x0000008a0	0x00000037	0xffffffd5
1	1	1	1	0x03ffffff	0x00000000	0x00000000
2	1	1	0	0x0000008a3	0x00000006	0x00000007
3	0	0	3			
0	1	0	1	0x00000089d	0xffffffed	0x00000058
1	1	0	0	0x0000008a2	0xffffffff	0x00000001
2	0	0	3			
3	0	0	3			
0	1	0	1	0x00000089d	0x00000010	0xffffffb5
1	1	0	0	0x0000008a2	0xffffffff	0x00000003
2	0	0	3			
3	0	0	3			

cycle38

I can see that the 3rd way (way 2) of the 2nd set (set 1) is inserted data by a store instruction at cycle 38, thus the dirty bit becomes 1. And the LRU becomes 0 indicating that it is the most recent used way.

The diagram illustrates a 5-Stage RISC-V Processor and its state at cycle 100 and cycle 101.

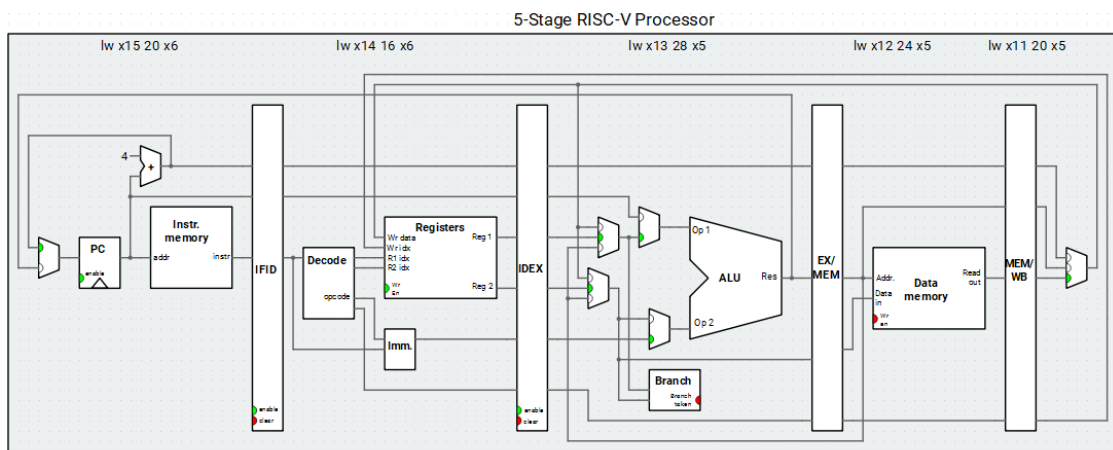
5-Stage RISC-V Processor: The processor consists of five stages: IFID, Decode, IDEX, ALU, and EX/MEM. The IFID stage includes a PC, Instr. memory, and a 4-bit adder. The Decode stage includes Registers (R1, R2), Imm, and op code. The IDEX stage includes a Branch unit. The ALU stage includes Op 1, Op 2, and a Branch unit. The EX/MEM stage includes Data memory and MEM/WB. The processor is shown with various data paths and control signals.

Cache State at cycle 100: The cache is a 4-set, 2-way LRU cache. The access address is 00000000000000000000000000000000. The cache state is as follows:

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	0	0x0000089e	0x00000007	0x00000007
1	1	1	3	0x000008a3	0xffffffff	0x00000005
2	1	1	2	0x000008a4	0xffffffff	0x00000000
3	1	1	1	0x000008a5	0xffffffff	0x00000000
4	1	1	1	0x000008a5	0xffffffff	0x00000000
5	1	1	0	0x03fffffff	0x00000000	0x000100a4
6	1	1	3	0x000008a3	0xffffffff	0x00000007
7	1	1	2	0x000008a4	0xffffffff	0x00000000
8	1	0	0	0x000008a5	0x0000000c	0x00202820
9	1	1	3	0x000008a2	0xffffffff	0x00000001
10	1	1	2	0x000008a3	0xffffffff	0x00000000
11	1	1	1	0x000008a4	0xffffffff	0x00000000
12	1	0	3	0x0000089d	0x00000010	0xffffffffbd
13	1	1	2	0x000008a2	0xffffffff	0x00000003
14	1	1	1	0x000008a3	0xffffffff	0x00000000
15	1	1	0	0x000008a4	0xffffffff	0x00000000

Cache State at cycle 101: The cache state is as follows:

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	0	0x0000089e	0x00000007	0x00000007
1	1	1	3	0x000008a3	0xffffffff	0x00000005
2	1	1	2	0x000008a4	0xffffffff	0x00000000
3	1	1	1	0x000008a5	0xffffffff	0x00202820
4	1	1	2	0x000008a5	0xffffffff	0x00202c20
5	1	1	1	0x03fffffff	0x00000000	0x000100a4
6	1	1	0	0x0000089e	0x00000007	0x00000007
7	1	1	3	0x000008a4	0xffffffff	0x00000000
8	1	0	3	0x0000089d	0xffffffffed	0x00000058
9	1	1	2	0x000008a2	0xffffffff	0x00000001
10	1	1	1	0x000008a3	0xffffffff	0x00000000
11	1	1	0	0x000008a4	0xffffffff	0x00000000
12	1	0	0	0x000008a5	0x69746172	0x00203a6f
13	1	1	3	0x000008a2	0xffffffff	0x00000003
14	1	1	2	0x000008a3	0xffffffff	0x00000000
15	1	1	1	0x000008a4	0xffffffff	0x00000000



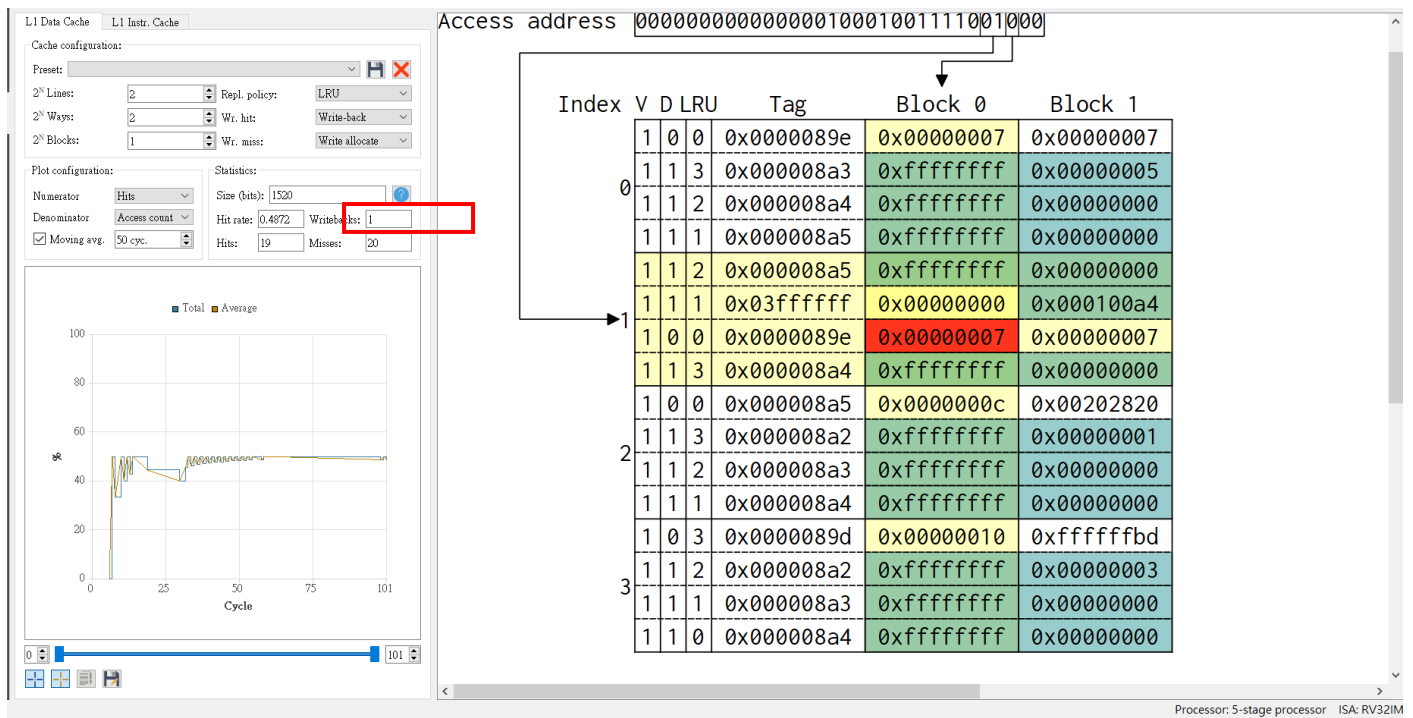
Access address 000000000000001000100111001000

Index 0 1 2 3

	V	D	LRU	Tag	Block 0	Block 1
0	1	0	0	0x00000089e	0x000000007	0x000000007
	1	1	3	0x0000008a3	0xfffffffff	0x000000005
	1	1	2	0x0000008a4	0xfffffffff	0x000000000
	1	1	1	0x0000008a5	0xfffffffff	0x00202820
	1	1	2	0x0000008a5	0xfffffffff	0x00202c20
	1	1	1	0x03ffffff	0x000000000	0x00100a4
	1	0	0	0x00000089e	0x000000007	0x000000007
	1	1	3	0x0000008a4	0xfffffffff	0x000000000
	1	0	3	0x00000089d	0xfffffffff	0x000000058
	1	1	2	0x0000008a2	0xfffffffff	0x000000000
	1	1	1	0x0000008a3	0xfffffffff	0x000000000
	1	0	0	0x0000008a4	0xfffffffff	0x000000000
	1	1	0	0x0000008a5	0x69746172	0x00203a6f
	1	1	3	0x0000008a2	0xfffffffff	0x000000003
	1	1	2	0x0000008a3	0xfffffffff	0x000000000
	1	1	1	0x0000008a4	0xfffffffff	0x000000000

cycle 101

After the load instruction goes to the MEM stage at cycle 101, the instruction makes the 3rd way (way 2) of the 2nd set (set 1) be replaced and then the previous data in the cache with dirty bit on was written back and we can observe that the dirty bit becomes 0 again since the load instruction doesn't need write back. And the LRU bit of the 3rd way (way 2) becomes 0 indicating that it is the most recent used way.



Simulation result

In previous homework, only one trial of finding centroid is performed, this time I performed 5 times and include some unrelated function to observe the block replace and writeback, such as storing value to array after every centroid is found.

