Programming Assignment #4 Cache Simulation

Calculate the nearest centroid of a set of points on 2D integer grid

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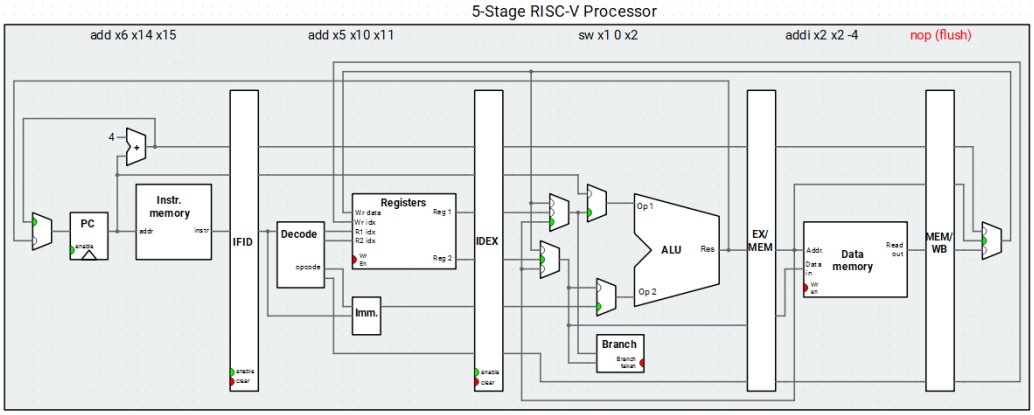
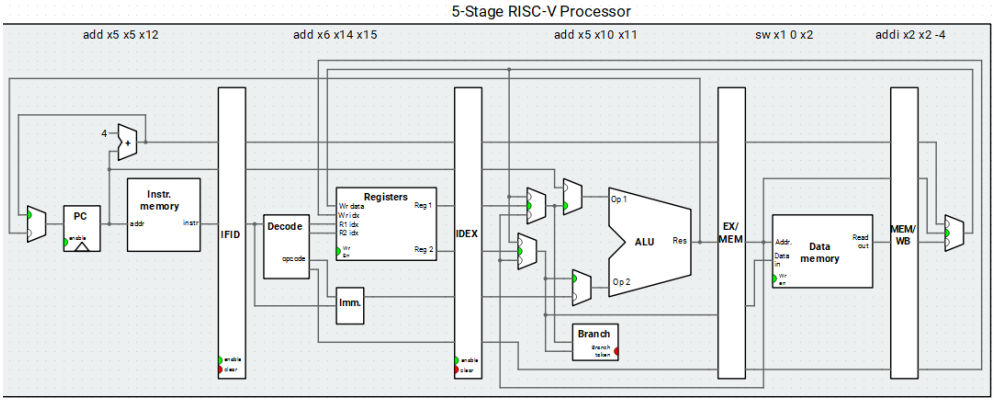
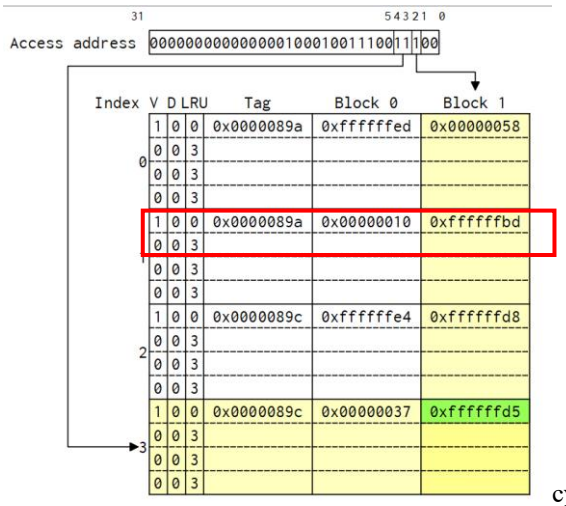
1. Insertion at an index with at least one way occupied

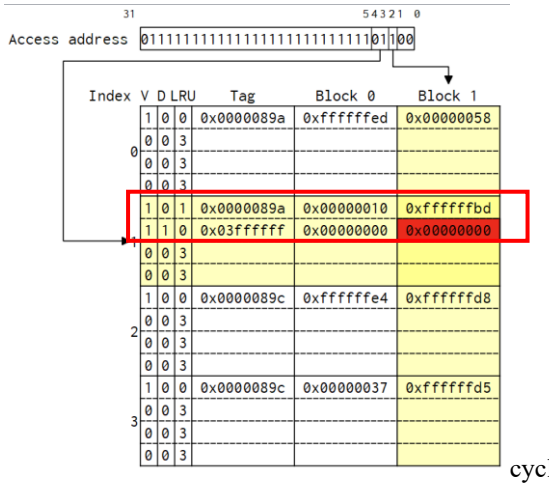




The insertion of cache with at least one way occupied after the sw x1 0 x2 instruction in EX stage pass to MEM stage.



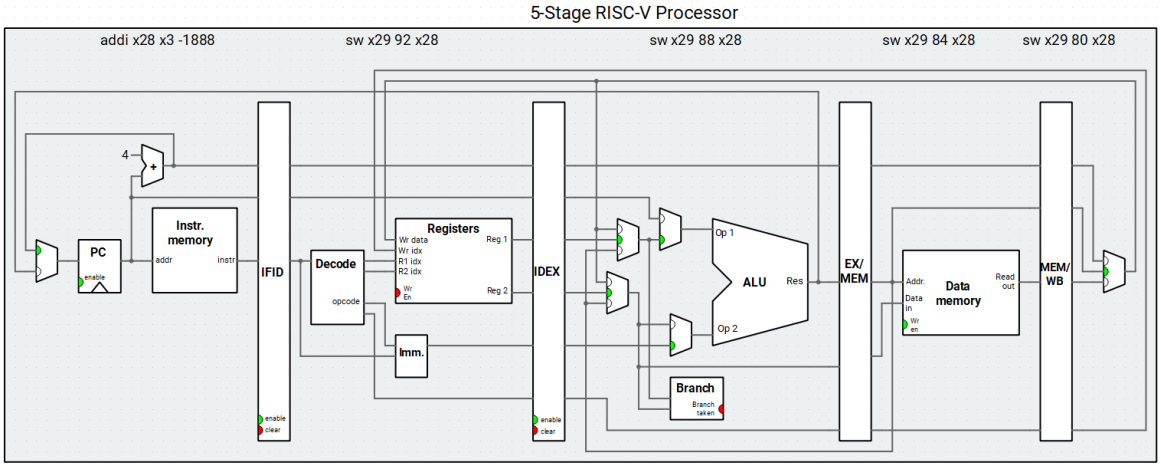
cycle 18

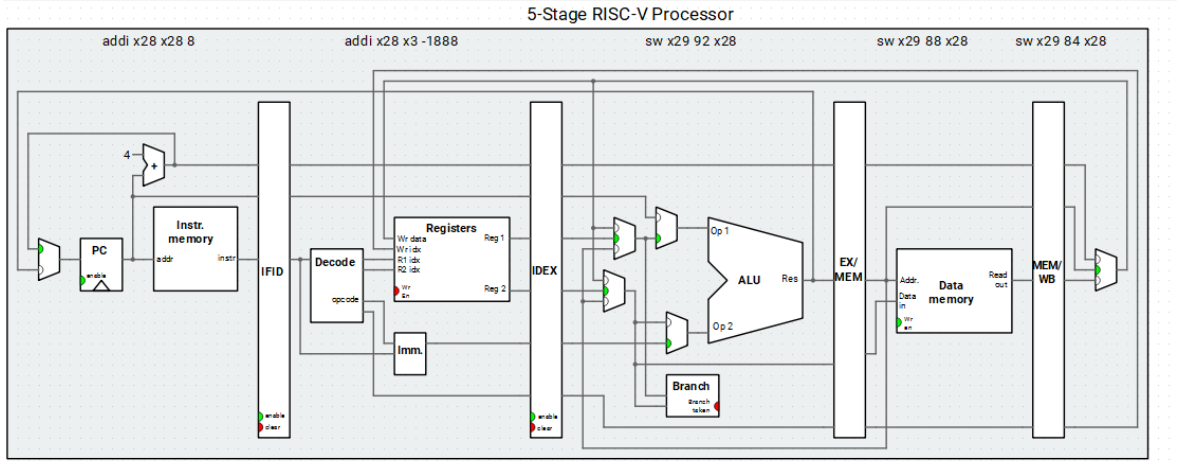


cycle 19

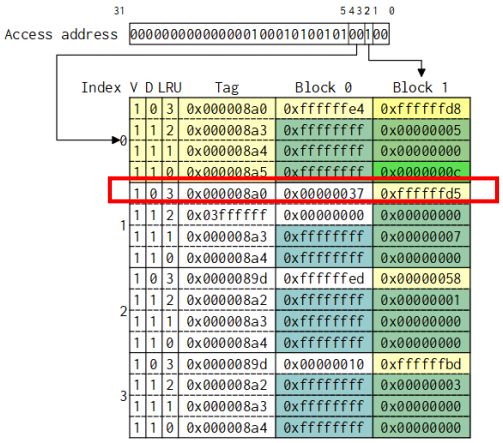
When in cycle 18, all set has at least 1 way (way 0) occupied, and after the store word instruction, the set indexed by 01 has to be inserted data to another way where the tag 0x03ffffff is different from 0x0000089a . Also, the LRU of the 1st way (way 0) becomes 1 and the LRU of the 2nd way (way 1) becomes 0, indicating that the 2nd way (way 1) is the recent used way.

2. Replacement

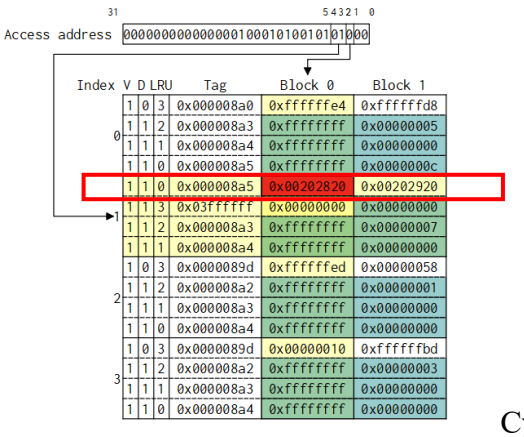




The replacement of block with 4 way (way 0~3) occupied after the sw x29 88 x28 instruction in EX stage pass through to MEM stage.



Cycle 53

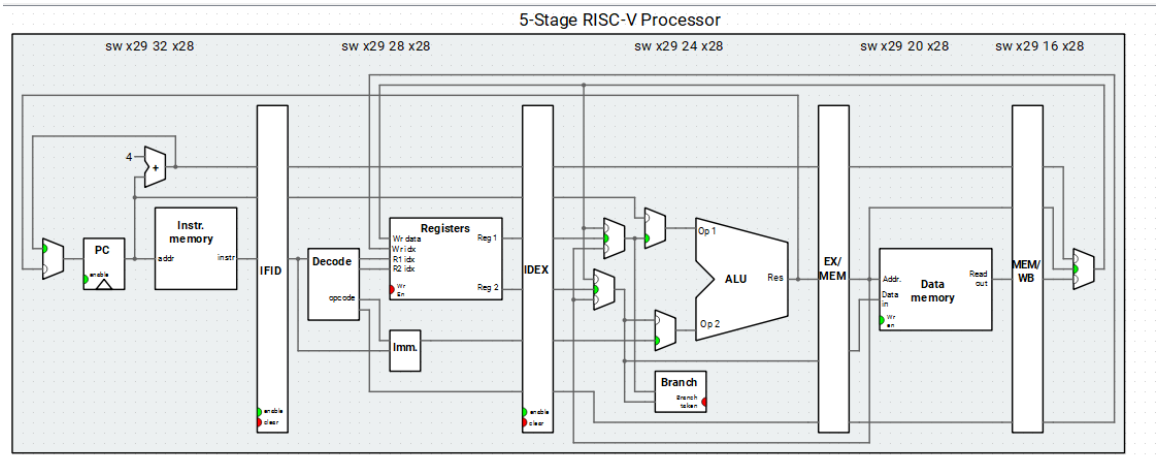


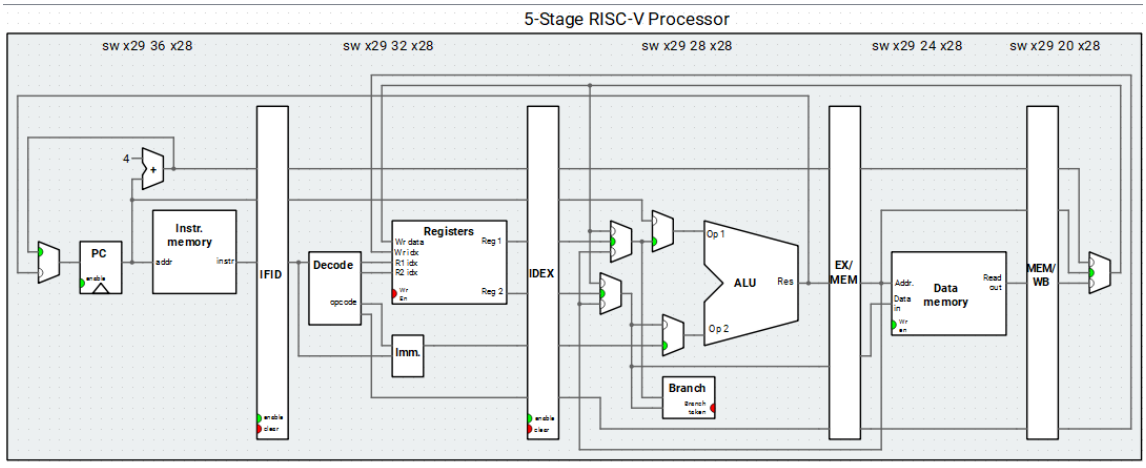
Cycle 54

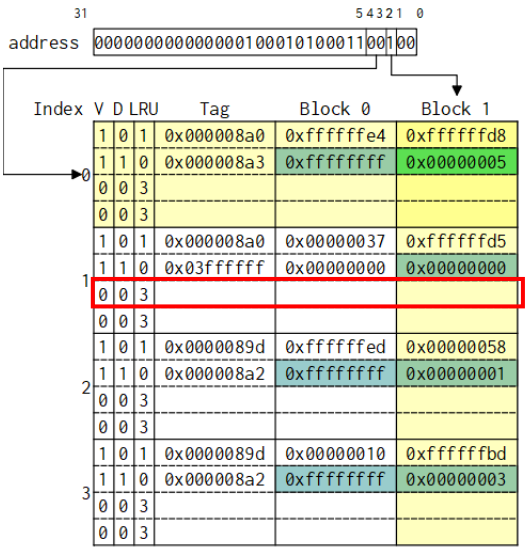
The replacement of block occurs at cycle 54 when the 4 way of the 2nd set (set 1) are already occupied, but new tag 0x000008a5 occurs, so that there is block replacement where the 1st way (way 0) (whose LRU bit was 3) of the 2nd set (set 1) is replaced and the LRU becomes 0, indicating that the 1st way (way 0) is the most recently used, the LRU bit of other 3 way then are all incremented by 1.

3. Write Back

The write of the block is after the sw x29 24 x28 instruction in EX stage pass through to MEM stage.





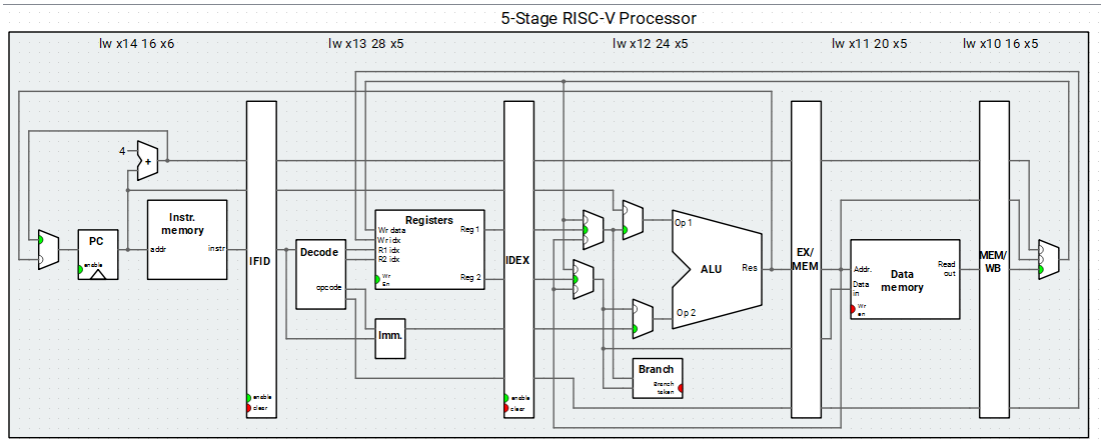


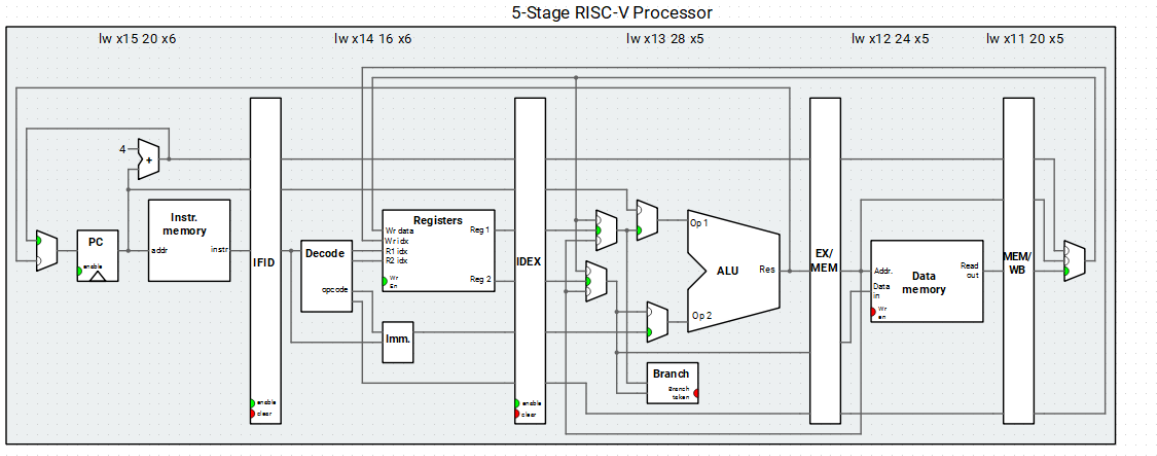
cycle37

cycle38

I can see that the 3rd way (way 2) of the 2nd set (set 1) is inserted data by a store instruction at cycle 38, thus the dirty bit becomes 1. And the LRU becomes 0 indicating that it is the most recent used way.

Then after the lw x12 24 x5 instruction goes to the MEM stage from EX stage





ccess address 00000000000000010001001111000100

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	0	0x0000089e	0x00000007	0x00000007
	1	1	3	0x000008a3	0xffffffff	0x00000005
	1	1	2	0x000008a4	0xffffffff	0x00000000
	1	1	1	0x000008a5	0xffffffff	0x00000000
1	1	1	1	0x000008a5	0xffffffff	0x00000000
	1	1	0	0x03ffffff	0x00000000	0x000100a4
	1	1	3	0x000008a3	0xffffffff	0x00000007
	1	1	2	0x000008a4	0xffffffff	0x00000000
2	1	0	0	0x000008a5	0x0000000c	0x00202820
	1	1	3	0x000008a2	0xffffffff	0x00000001
	1	1	2	0x000008a3	0xffffffff	0x00000000
	1	1	1	0x000008a4	0xffffffff	0x00000000
3	1	0	3	0x0000089d	0x00000010	0xfffffffbd
	1	1	2	0x000008a2	0xffffffff	0x00000003
	1	1	1	0x000008a3	0xffffffff	0x00000000
	1	1	0	0x000008a4	0xffffffff	0x00000000

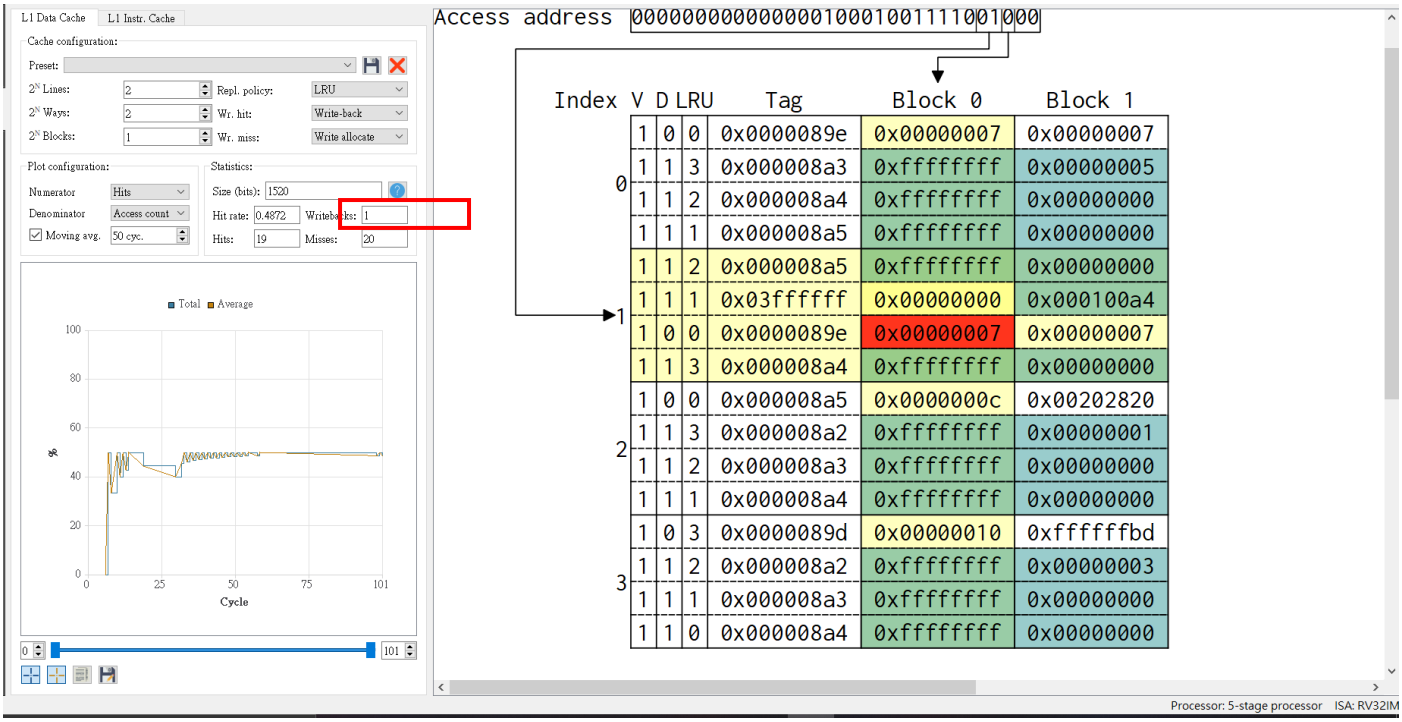
cycle100

Access address 00000000000000010001001111001000

Index	V	D	LRU	Tag	Block 0	Block 1
0	1	0	0	0x0000089e	0x00000007	0x00000007
	1	1	3	0x000008a3	0xffffffff	0x00000005
	1	1	2	0x000008a4	0xffffffff	0x00000000
	1	1	1	0x000008a5	0xffffffff	0x00202820
1	1	1	2	0x000008a5	0xffffffff	0x00202c20
	1	1	1	0x03ffffff	0x00000000	0x000100a4
	1	0	0	0x0000089e	0x00000007	0x00000007
	1	1	3	0x000008a4	0xffffffff	0x00000000
2	1	0	3	0x0000089d	0xffffffed	0x00000058
	1	1	2	0x000008a2	0xffffffff	0x00000001
	1	1	1	0x000008a3	0xffffffff	0x00000000
	1	1	0	0x000008a4	0xffffffff	0x00000000
3	1	0	0	0x000008a5	0x69746172	0x00203a6f
	1	1	3	0x000008a2	0xffffffff	0x00000003
	1	1	2	0x000008a3	0xffffffff	0x00000000
	1	1	1	0x000008a4	0xffffffff	0x00000000

cycle 101

After the load instruction goes to the MEM stage at cycle 101, the instruction makes the 3rd way (way 2) of the 2nd set (set 1) be replaced and then the previous data in the cache with dirty bit on was written back and we can observe that the dirty bit becomes 0 again since the load instruction doesn't need write back. And the LRU bit of the 3rd way (way 2) becomes 0 indicating that it is the most recent used way.



Simulation result

In previous homework, only one trial of finding centroid is performed, this time I performed 5 times and include some unrelated function to observe the block replace and writeback, such as storing value to array after every centroid is found.