Advanced Computer Architecture Mini Project 1

- Implement Pipelined RISC-V integer processor (partially) such that it supports three different category of instructions as mentioned below:
    1. ALU Instructions (R-Type instructions) also called as computational instructions
    2. Memory Instructions (load and Store)
    3. Control Transfer Instructions (should include conditional and unconditional branch instructions)
- The processor should support at least 12 instructions under the above specified categories.
- This processor should support forwarding and stalling to avoid data hazards.
- This processor should also support branch prediction and flushing to avoid control Hazards.
- The processor should be tested using a simple application based program e.g. Sorting, Searching, GCD computation etc.

(Refer to the RISC V Manual available at https://content.riscv.org/wp-content/uploads/2019/06/riscv-spec.pdf)
