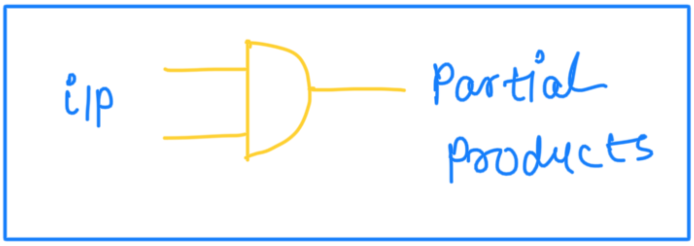
# Binary Multiplication

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | A2 | A1 | A0 | Multiplicand |
| × | | | B2 | B1 | B0 | Multiplier |
| | | | A2B0 | A1B0 | A0B0 | |
| + | | A2B1 | A1B1 | A0B1 | × | |
| + | A1B2 | A1B2 | A0B2 | × | × | |

- Combinational circuit Multiplier

**Array Multiplier :** cause it consists of the array of the adders as well as the AND gates.



Then we will use the adders circuit to get final output.

## N-bit Multiplication :

We need : $N^2$ - AND gates

$N$ - Half adders

$N(N-2)$ - Full adders

→ For N-bit multiplier, if we consider :

TA = Tc = TS = 1 unit delay
(AND gate) (carry) (sum)

then to get the valid product output,

required delay ~ $\boxed{\text{2N unit delay}}$

→ As N increases,

$$\left.\begin{array}{l}\text{Required Hardware resources}\\ \text{Hence power consumption}\end{array}\right\}\text{increase}$$

⇒ Array Multipliers are not preferable for large value of N.

## Signed binary Multiplication :

2's complement Form

$$\boxed{\begin{array}{r}\text{n bits}\\ \times\ \text{n bits}\\ \hline \text{2n bits}\end{array}}$$

Ex. 1

$$\left.\begin{array}{rl}-5 & \longrightarrow 1011\\ \times\ 7 & \longrightarrow 0111\\ \hline -35 & \end{array}\right\}\text{2's complement}$$

7 → $\boxed{\text{Positive}}$

So now,

$$\begin{array}{ccccccccc}
 & & & & 1 & 0 & 1 & 1 & \\
\times & & & & 0 & 1 & 1 & 1 & \\
\hline
1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & \\
1 & 1 & 1 & 1 & 0 & 1 & 1 & \times & + \\
1 & 1 & 1 & 0 & 1 & 1 & \times & \times & + \\
0 & 0 & 0 & 0 & 0 & \times & \times & \times & + \\
\hline
1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & \longrightarrow \boxed{-35}
\end{array}$$

Ignore the extra MSBs in the answer.

Ex. 2

$$-5 \longrightarrow 1011 \ \}\ \text{2's complement}$$

× (− +) → 1001

35

Negative

When multiplier is negative, we have to take 2's complement of last row to get the correct answer.

So now,

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | 1 | 0 | 1 | 1 | |
| × | | | | | 1 | 0 | 0 | 1 | |
| | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | f |
| | 0 | 0 | 0 | 0 | 0 | 0 | X | X | + |
| | 1 | 1 | 0 | 1 | 1 | X | X | X | − |
| | 0 | 0 | 1 | 0 | 1 | X | X | X | + |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |

important for −ve Multiplier

take 2's complement & add to the answer

ignore this bit

35

Note : now, since this is signed multiplication, if we apply this rule to the positive multiplier also, it won't change anything.

→ cause, signed +ve multiplier

⇒ M.S.B. "0" ⇒ Partial products "0.... 0" All zeroes

taking 2's complement won't affect anything

cause we are ignoring

cause we are ignoring
the extra bits.