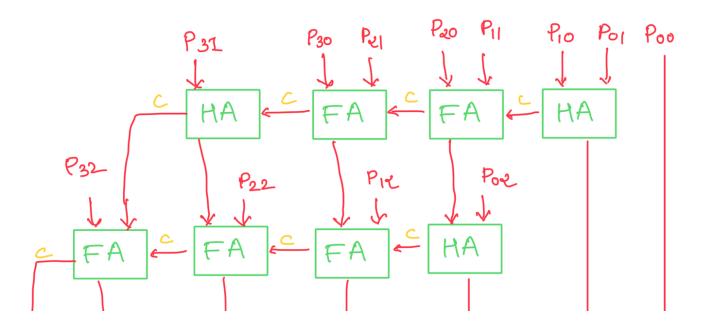
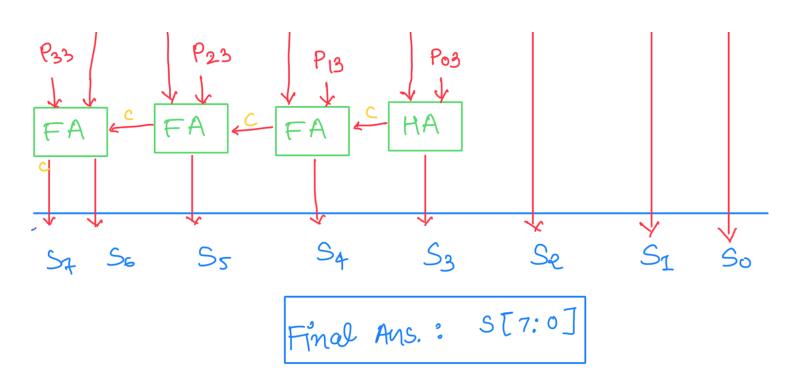
Multiplication of Binary numbers

4-01+ 11P

Let's call the partial product for bit Ai F
Bi, Pij. Now for addition we have to
use Full adders (FAs) or half adders (HAs)
according to the needs.





Now if we want to add the signed bit for multiplication purpose, we can provide an additional signed bit for both imputs, which then propagate through logic as the sign of the output.

Let's Assume, 0 bit -> "-"ve humber

I bit -> "+"ve number

Truth teste:

| A | В | si gn_ |
|---|---|--------|
| 0 | 0 | 1 |
| O | 1 | O |
| 1 | 0 | O |
| 1 | 1 | 1 |

n. er voe rese 2'- complement as input

number, it is very important to do sign extention upto M.S.B. too each term of murtiplication.

At the end of the multiplication, We ignore the extra bits to the left corner and treat left bit M.S.B. as a sign of the answer.

Note: But for this method, whem multiplier be the negative number, it won't give the correct answer.

To get the consect answer, we have to texter 2's complement of the last multiplicative fector and then we can get correct result by adding it to the answer. (Or to say subtract the last fector insted of adding it.)

Logic: So we will take 2's complement for both the cases cause it won't effect the answer for positive multiplier.

Optimization to avoid additional Hardware Problem?

Here, if we can make the extended signed bit "o" by adding on subtracting somer thing, it may lead us to optimize the hardware use.

But How! : Let's say the M.S.B. is A. $A \oplus 1 = \overline{A}$

A _____ A

So by adding "I" to the MSB, we can modify all the sign extentation to "o" and hence no need to add it

→ we need to add (1) to all the signed extention bits. And adding "I" means taking complement.

Because we are adding the numbers, we also have to substract or say add 2's complement at the and.

Result: so, the final result will look
like this:

⇒ By only addition of 2 adders, we are alone to make signed multiplier for

4-bit x 4-bit binary multiplication.