A REPORT ON

DIGITAL INTEGRATED CIRCUIT DESIGN ASSIGNMENT

ANALOG AND DIGITAL VLSI DESIGN

SUBMITTED BY

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Problem Statement No. 26

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INTRODUCTION

Logic function to be implemented:

$$Z = [(A * B * F + (C + (D * F) + E * C + H))]'$$

After simplification, the form of the above expression that leads to usage of minimal gates is:

$$Z = [(A * B + D) * F + C + H)]'$$

Note:

(i) Due to limitations of Microwind, LVS and PEX could not be implemented. Microwind does not give output unless DRC checks are passed. Our layout passed the DRC check and hence we were able to obtain outputs as shown below in the subsequent sections

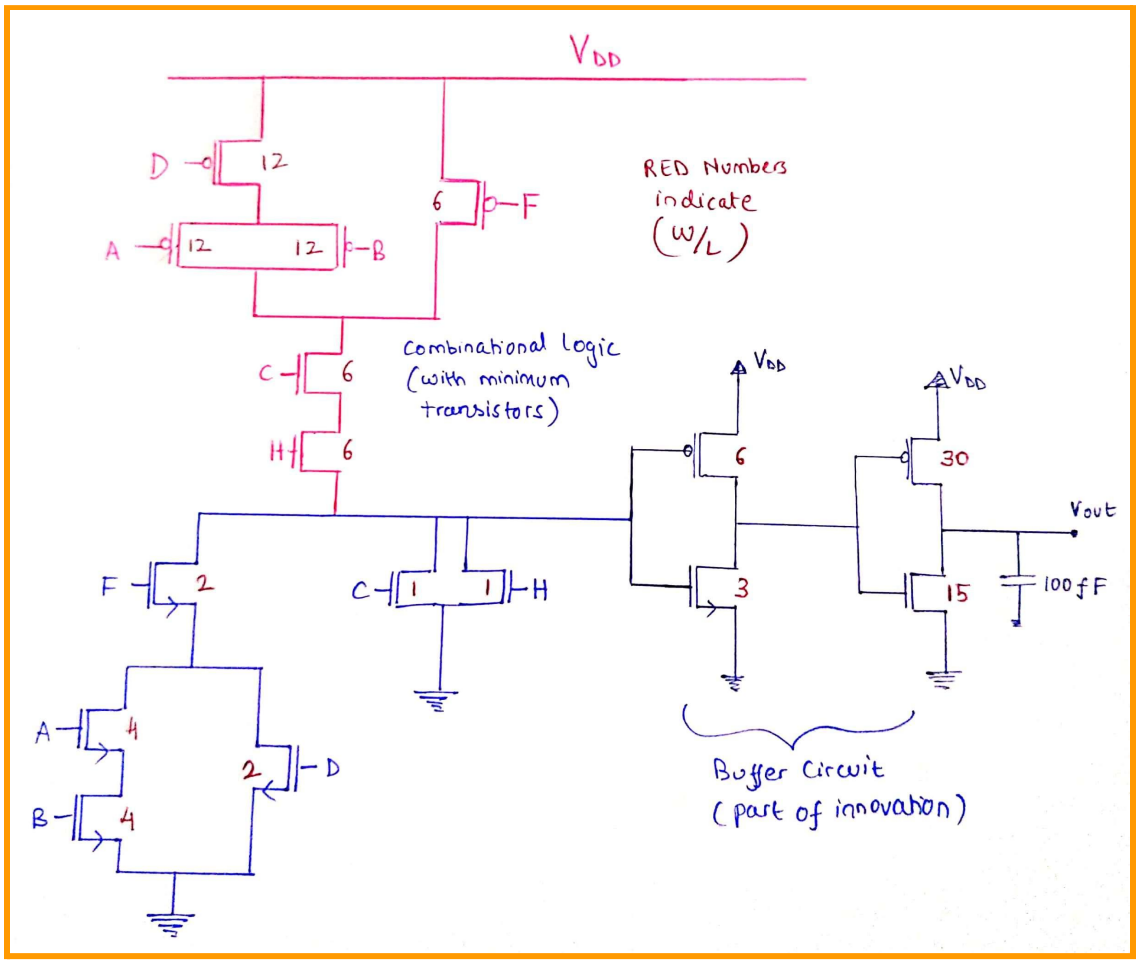
(ii) Microwind has a minimum resolution of 100 nm, hence we could not achieve Lmin = 180 nm, and had to settle for 200 nm. However, functionality of circuit has remained unchanged.

DESIGN SPECIFICATIONS

Parameter	Value
Supply Voltage	1.8 Volt
Load Capacitance	100 fF
Minimum Length	180 nm

MOSFET SIZING DIAGRAM

All aspect ratios in the *Combinational Circuit* were fixed by making the whole circuit an equivalent of a unit CMOS inverter. Aspect ratios of the *Output Buffer Circuit* were fixed using the concept of logical effort in a chain of inverters driving a load capacitance.



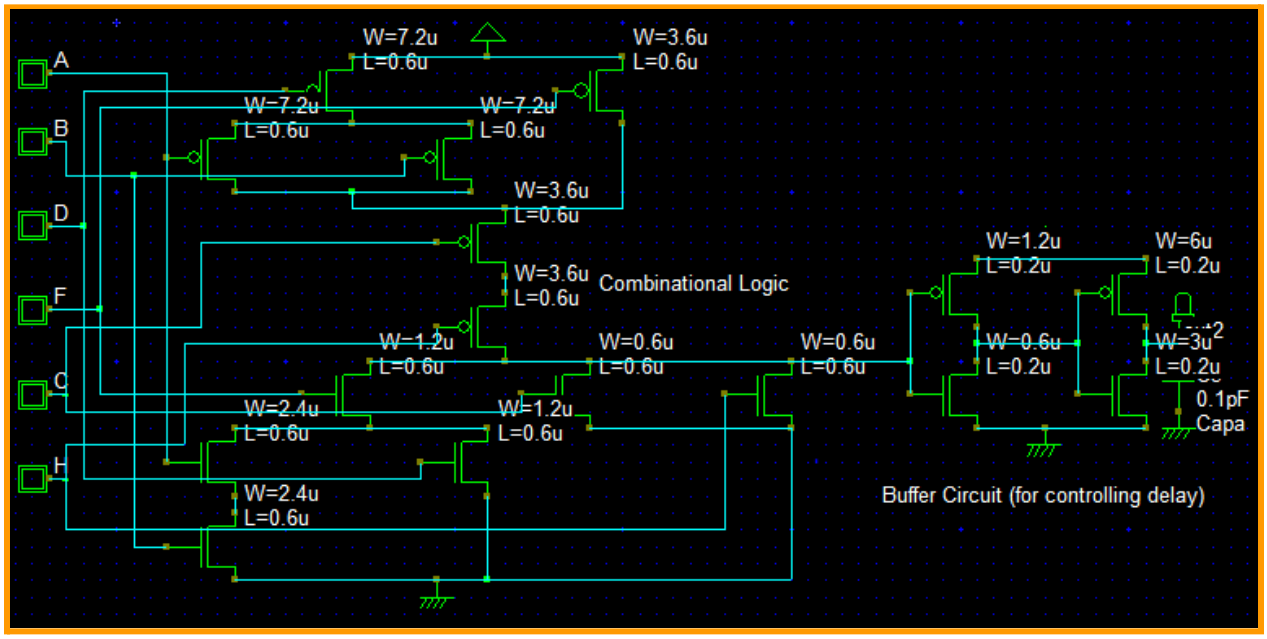


Fig. 1) Schematic of circuit (implemented in DSCH)

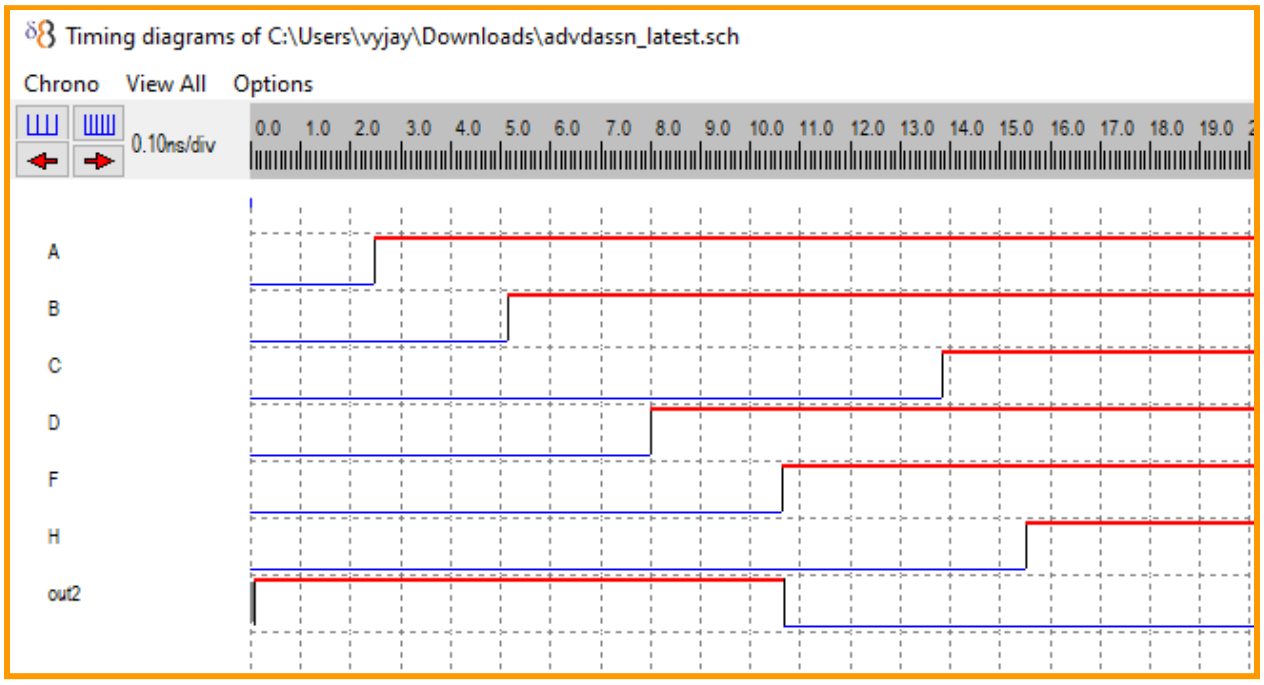


Fig. 2) Timing Diagram of DSCH schematic

LAYOUT

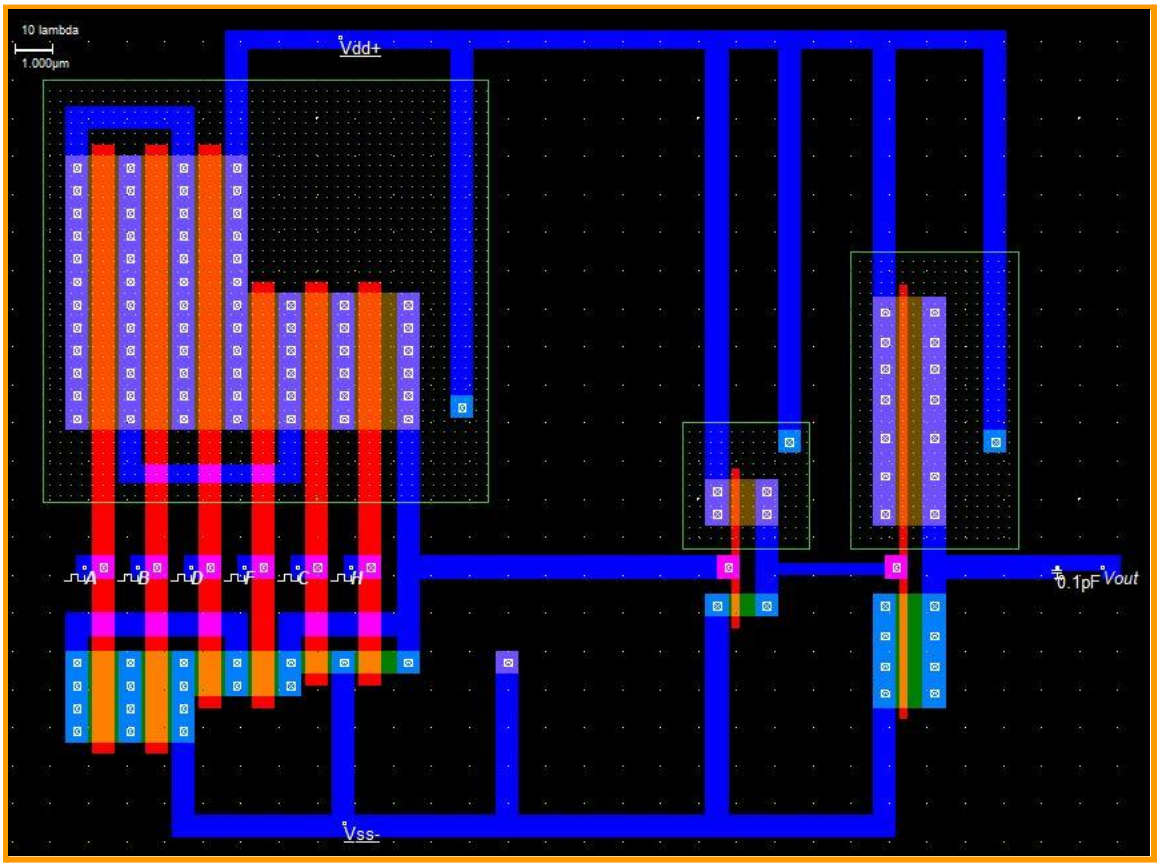


Fig.3) Layout in Microwind 3.1

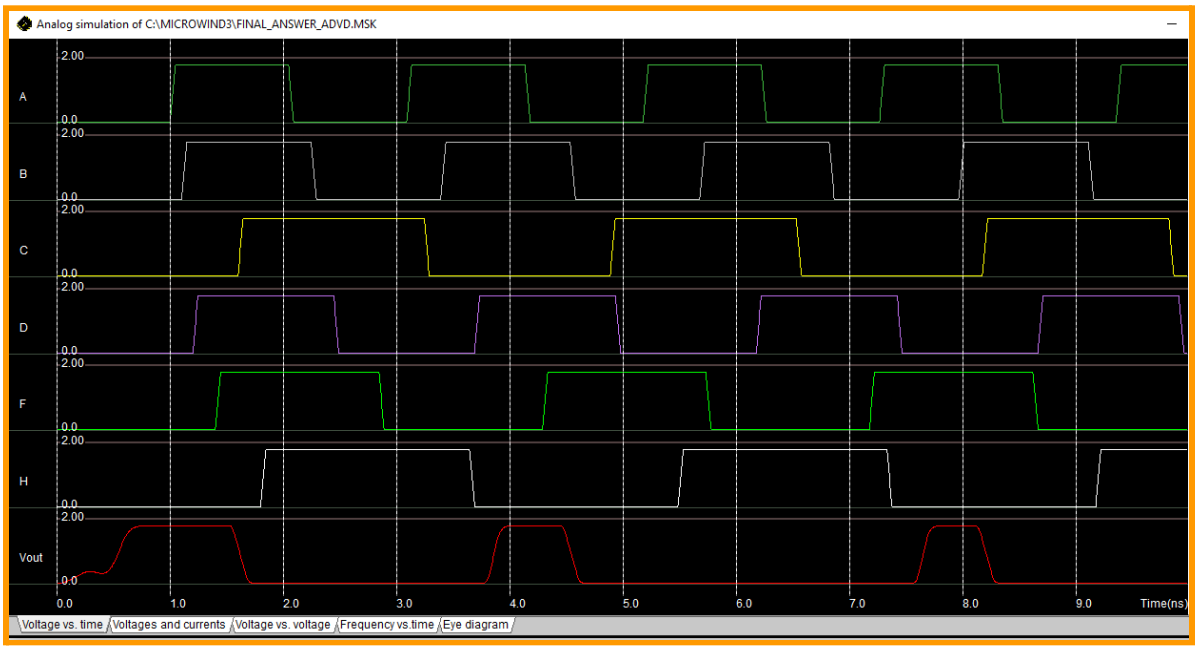


Fig. 4) Timing Diagram of Layout (generated in Microwind 3.1)

Power Consumption = 0.161 mW

Area = 648.7 um^2

$$T_{PLH} = 194\,ps$$

$$T_{PHL} = 140\,ps$$

$$T_{AVG} = \frac{T_{PLH} + T_{PHL}}{2} = 167\,ps$$

INNOVATION

We initially observed that the 0.1 pF load capacitor was smoothing the output of our circuit (*just the combinational part without the buffer*), which resulted in a somewhat distorted waveform devoid of sharp edges. We concluded that the Tplh and Tphl need to be minimised in order to tackle this issue. Hence somehow, the time constant of the net load capacitance was needed to be reduced.

A chain of inverters is a powerful tool used to drive large load capacitances. It acts as a buffer and reduces output resistance, thus decreasing the time constant of the capacitance at the load. Hence we sought to design a chain of inverters (even number) which could be attached to the output of the combinational circuit.

We first started with a minimum sized CMOS inverter connected to the output of the combinational circuit. We obtained the parasitic capacitance at the input node of the inverter

Cin = 4.165 fF

C_load = 100fF approx (*neglecting output parasitics*)

Hence **F = 100/4.165 = 24.01** (*electrical fanout*)

Therefore **N = log(24.01) to the base 3.6 = 2.48 => 2** (*optimal number of inverters in chain*)

f = $F^{\frac{1}{N}}$ = **4.9 (approximately 5)** *(sizing factor)*

Hence widths of the second inverter would be 5 times larger than the first inverter of the buffer

RESULTS OF THIS CHANGE

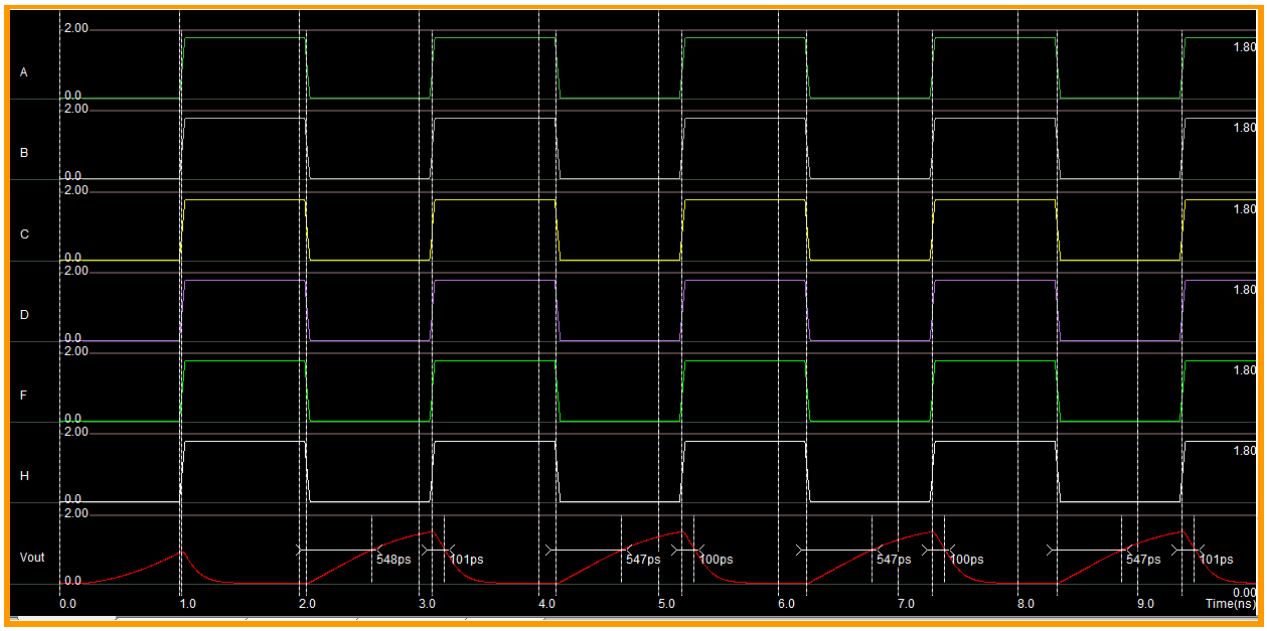


Fig. 5) Output waveform without inverter chain (shown in red at the bottom)

T_avg = 323.5 ps

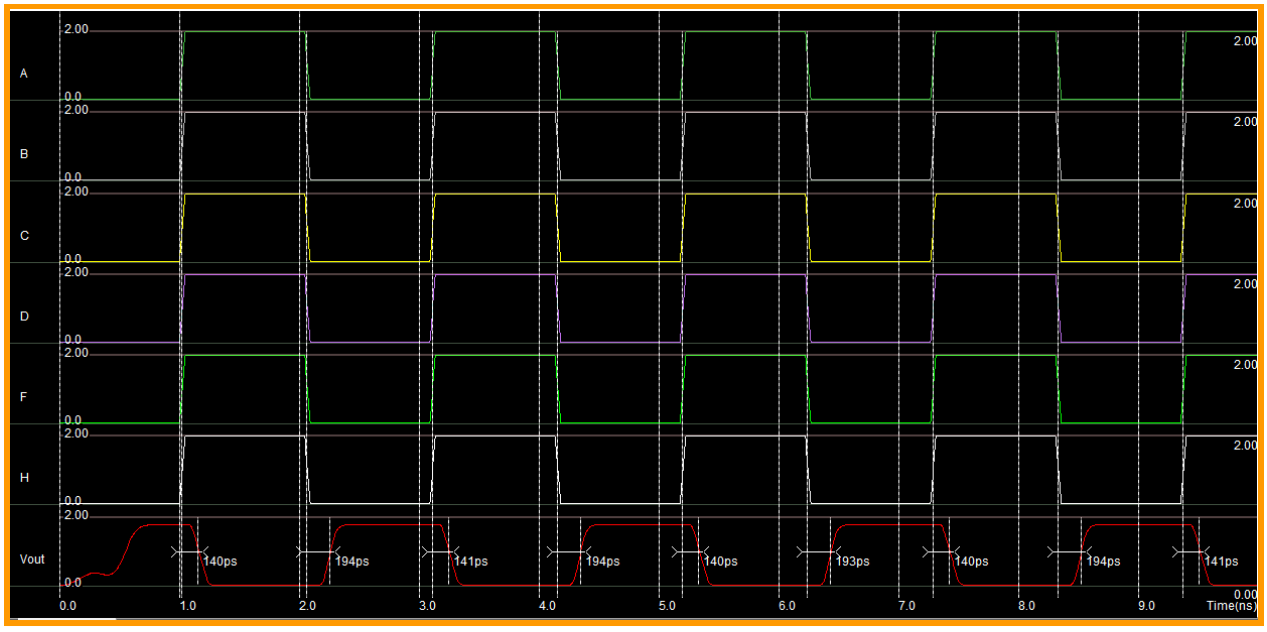


Fig. 6) Output waveform after attaching buffer chain (shown in red at the bottom)

T_avg = 167 ps **Improvement of 48.377 %**