Birla Institute of Technology and Science Pilani, Pilani Campus (Raj.)
Department of Electrical and Electronics Engineering
EEE/INSTR F244 Microelectronic Circuits
Second Semester 2019-20

Weightage: 10 marks **SPICE Assignment-II** **Date: 05/04/2020**

Instructions for submission

1. Students should use LTSPICE simulator for solving the problems.
2. Final report submission process shall be uploaded a few days before the submission dead line.
3. Your assignments shall be collected on *19th April 2020*.
4. A penalty of FIVE marks per day shall be imposed for late submissions.
5. Neatly sketch and label all the plots. Proper units have to be mentioned for all the quantities.

Problem-1 (Differential Amplifier Design): Design a differential amplifier using suitable topology to meet the specifications prescribed for you. V_{DD} is 3.3V.

1. Output swing has to be at-least 80% of V_{DD} .
2. Power supply rails available are V_{DD} and ground only.
3. Only one current source can be used in the design I_{REF} = 50µA.
4. Every bias voltage needed has to be generated by designing proper circuits.
5. Use of Resistors is not allowed in the design.
6. Use a load capacitance of 1pF on both the output terminals.
7. ICMR should be $0.2V_{DD}$ to $0.8V_{DD}$
8. Phase margin has to be at-least 45°.

Analysis Required:

1. DC operating point of each MOSFET in the circuit as obtained from SPICE.
2. Bode Plot for differential mode gain and CMRR.
3. Obtain the Gain margin and phase margin.
4. ICMR and output swing calculation from SPICE.
5. Plot the variation of differential mode gain when V_{DD} varies by ±10%.

In your submission:

List your specification as per the rules formulated in Table-II.
Draw the circuit showing the W/L values of each MOSFET.
Include hand calculations.
At the last present a table comparing the hand calculation Vs actually used W/L values.

Table I Specifications

	Col.-1	Col.-2	Col.-3
	A_{DM}(dB)	CMRR (dB)	Power dissipation (mW)
Row-1	85 ± 5%	110± 5%	2.5± 5%
Row-2	90± 5%	120± 5%	3.5± 5%
Row-3	75± 5%	90± 5%	2.0± 5%
Row-4	80± 5%	100± 5%	3.0± 5%

Your Design Specifications:

Table II Rules for choosing the specification

A_{DM}	Row-1 (if sum of last two digits of id no. %4 == 0)
	Row-2 (if sum of last two digits of id no. %4 == 1)
	Row-3 (if sum of last two digits of id no. %4 == 2)
	Row-4 (if sum of last two digits of id no. %4 == 3)
CMRR	Row-1 (if sum of last four digits of id no. %4 == 0)
	Row-2 (if sum of last four digits of id no. %4 == 1)
	Row-3 (if sum of last four digits of id no. %4 == 2)
	Row-4 (if sum of last four digits of id no. %4 == 3)
P_D	Row-1 (if (tut. Sec no. * last 2 digits of year of admission) %4 == 0)
	Row-2 (if (tut. Sec no. * last 2 digits of year of admission) %4 == 1)
	Row-3 (if (tut. Sec no. * last 2 digits of year of admission) %4 == 2)
	Row-4 (if (tut. Sec no. * last 2 digits of year of admission) %4 == 3)

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