

A REPORT ON

ANALOG CIRCUIT DESIGN ASSIGNMENT

ANALOG AND DIGITAL VLSI DESIGN

SUBMITTED BY

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EEE/INSTR F313 - Analog and Digital VLSI Design



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Problem Statement No. 48

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INTRODUCTION

Problem Statement:

Ques 48. Design a Two stage single-ended output CMOS OPAMP with a -3dB bandwidth of 5MHz.

- (a) Analog schematic for OPAMP (choose appropriate OPAMP).
- (b) Analysis of all equations for OPAMP, with a systematic derivation of all transistors W/L ratios. (Do not use hit-an-trial method)
- (c) What is the settling time for your OPAMP?
- (d) What is the closed loop gain and phase margin for your OPAMP using STB analysis?
- (e) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, CMRR plot, ICMR plot, PSRR plot, slew rate, settling time, output voltage swing (dc + Transient), power consumption, and input and output offset voltage.

DESIGN SPECIFICATIONS

Technology	TSMC 180nm technology*
V_{DD}	2.5V
C_L	≤ 1 pF
Current mirror ratios	≤ 20
Reference Current	Single ideal current source of arbitrary value, with the positive node tied to V_{DD} or negative node tied to ground
Power Dissipation	≤ 3 mW unless stated

MOSFET SIZING

Channel length used = 350 nm for all MOSFETS

MOSFET	W/L
M1, M7, M8, M9	60.649
M4, M5, M6	127.45
M3	122.87
M2, M13	121.298
M11, M14	30.47
M10, M12	60.94

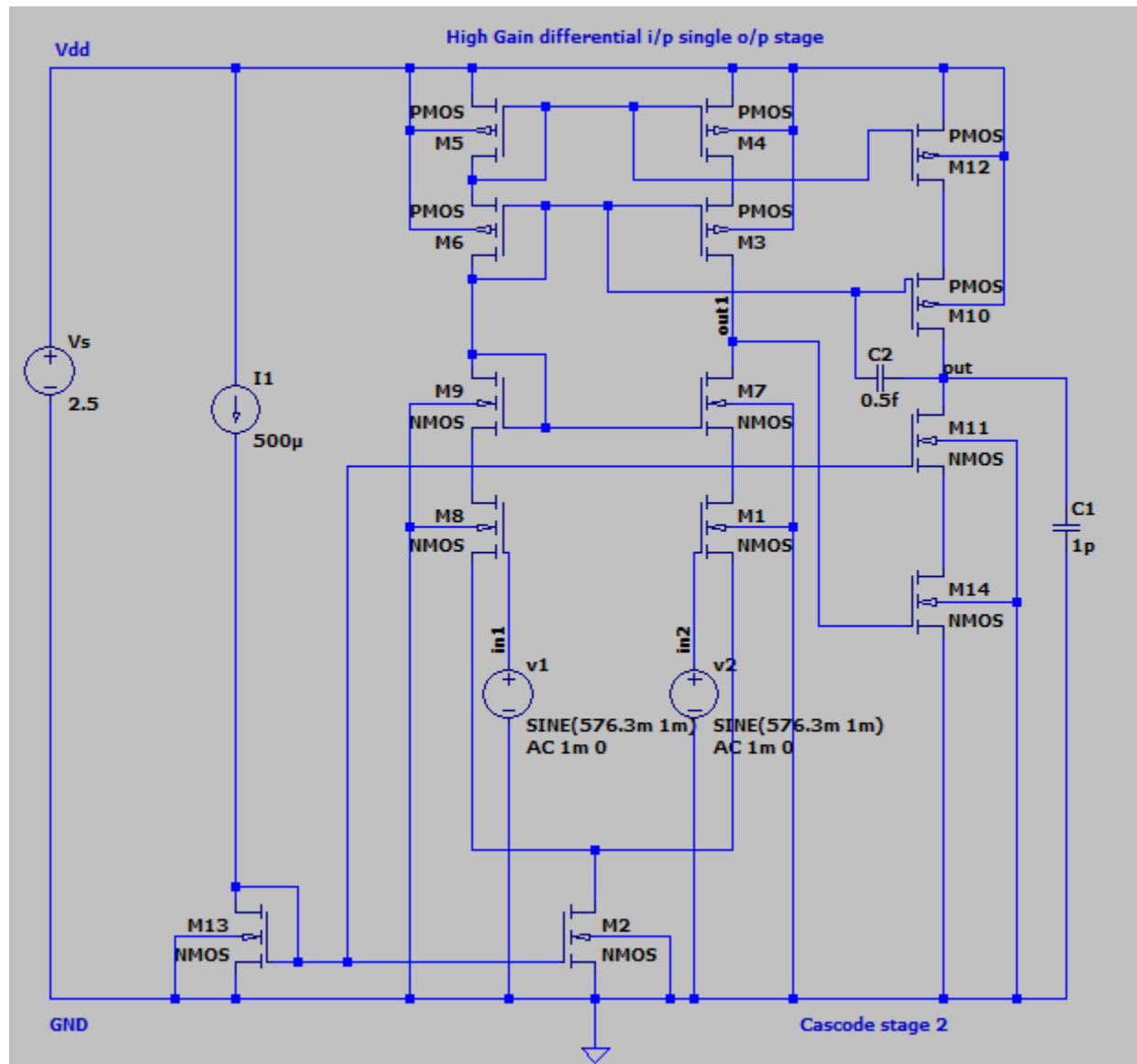
Stage 1 was used as differential amplifier with single ended output to obtain a single ended output with some gain

Stage 2 was used as a cascode amplifier in order to boost gain and obtain 3dB frequency by matching Rout

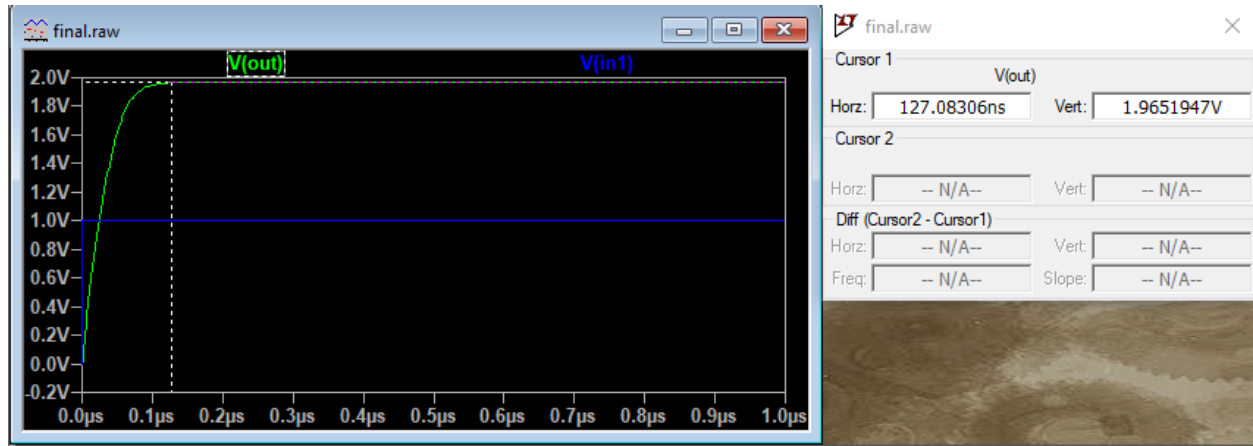
Design Equations Used

Quantity	Formula
g_m	$\frac{2I_D}{V_{OV}}$
r	$\frac{1}{\lambda I_D}$
I_D	$\frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$
CMRR	$20 \log_{10} \left(\frac{A_D}{A_{CM}} \right)$
PSRR	$20 \log_{10} \left(\frac{A_D \Delta V_{supply}}{\Delta V_{out}} \right)$

Schematic Diagram



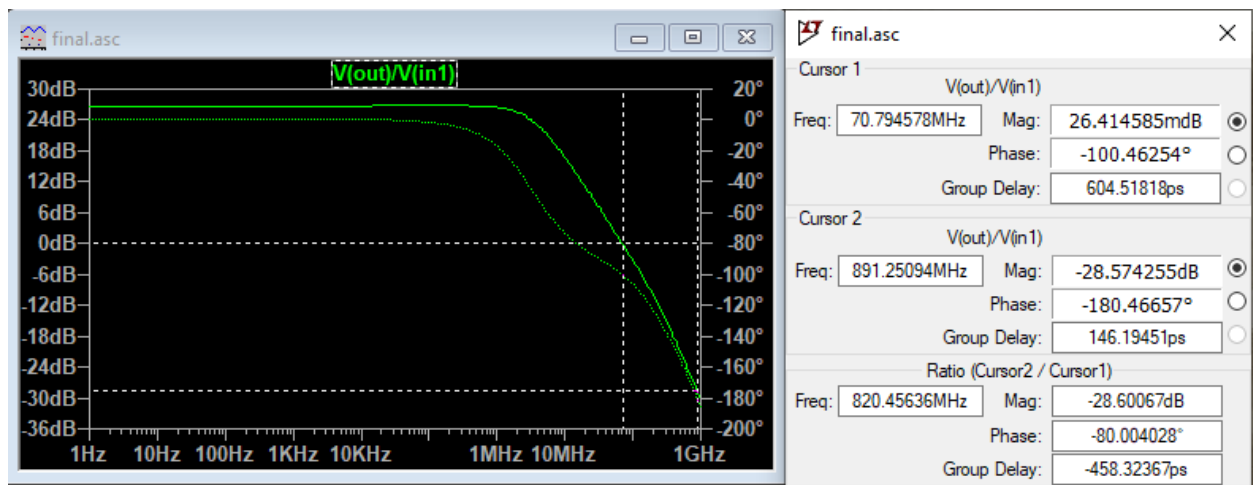
SETTLING TIME ANALYSIS



Settling time = 0.127 μs (non-inverting feedback configuration)

Slew Rate = 2960 V/μs

CLOSED LOOP GAIN AND PHASE MARGIN



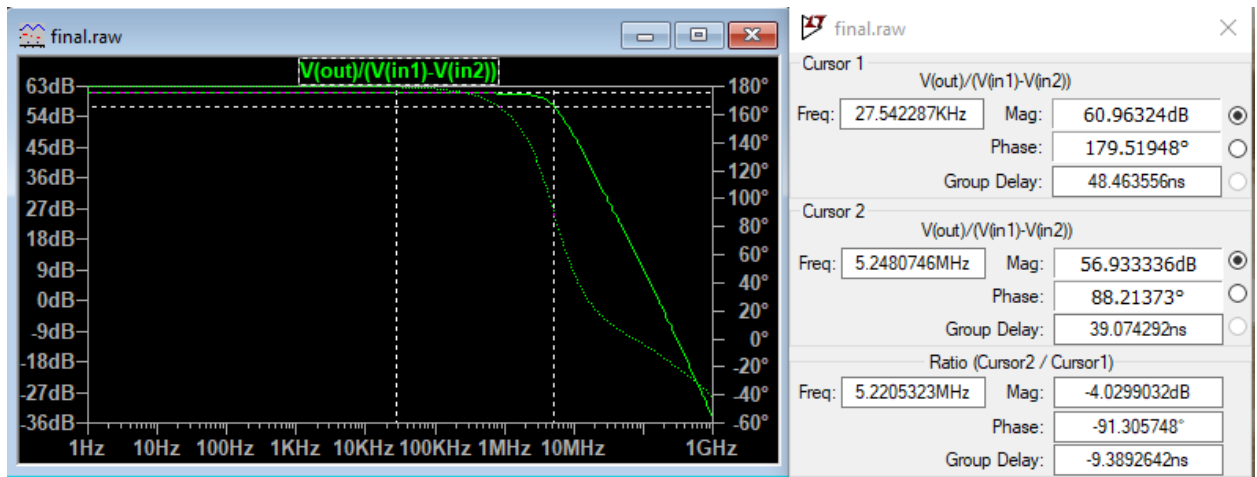
We connect the op-amp in a closed loop fashion and use miller compensation capacitor of 0.5f to adjust for Gain and Phase margin

Phase Margin = 79.537 degrees

Gain Margin = 28.60067 dB

OTHER PARAMETERS

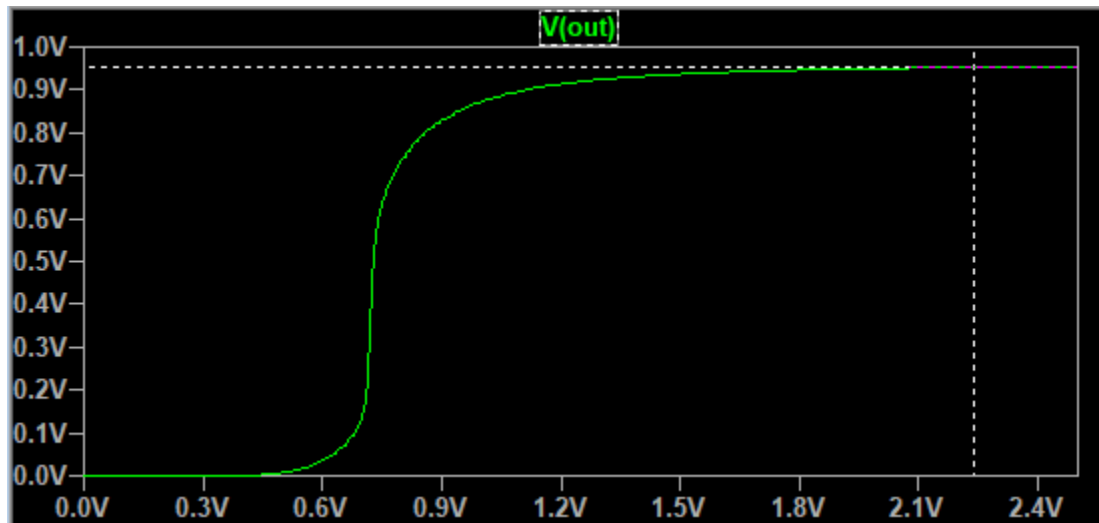
1) AC Gain and Phase



Max Gain = 60.9 dB

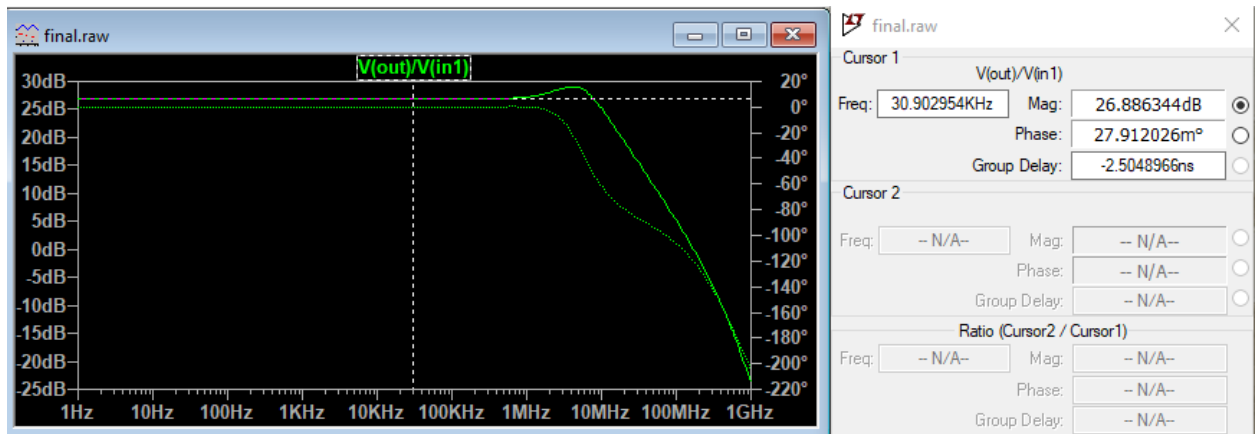
3 dB frequency = 5.248 MHz (target was 5 MHz)

2) ICMR plot



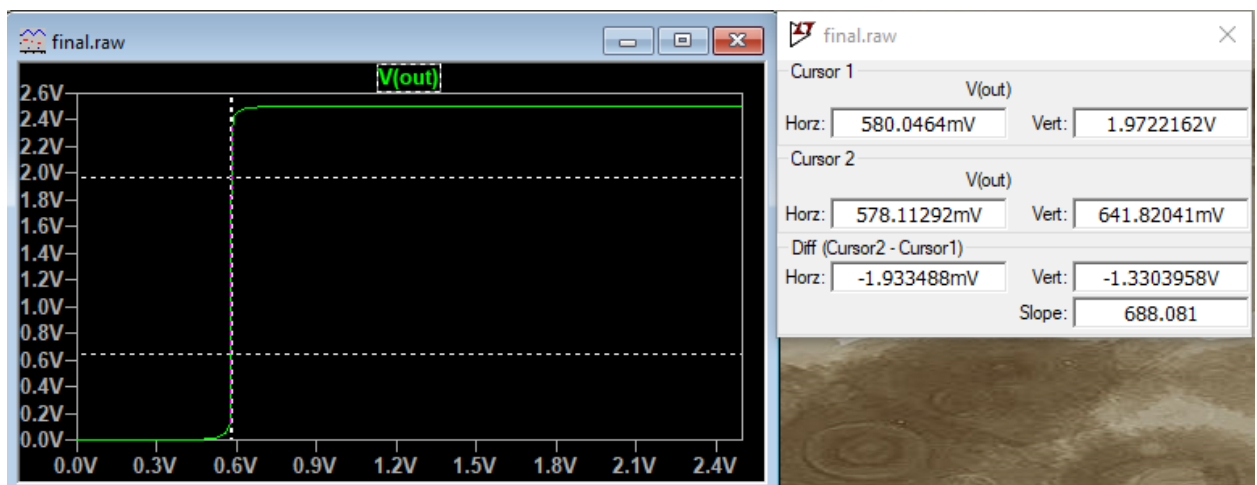
ICMR = 0.952 volt

3) CMRR Plot



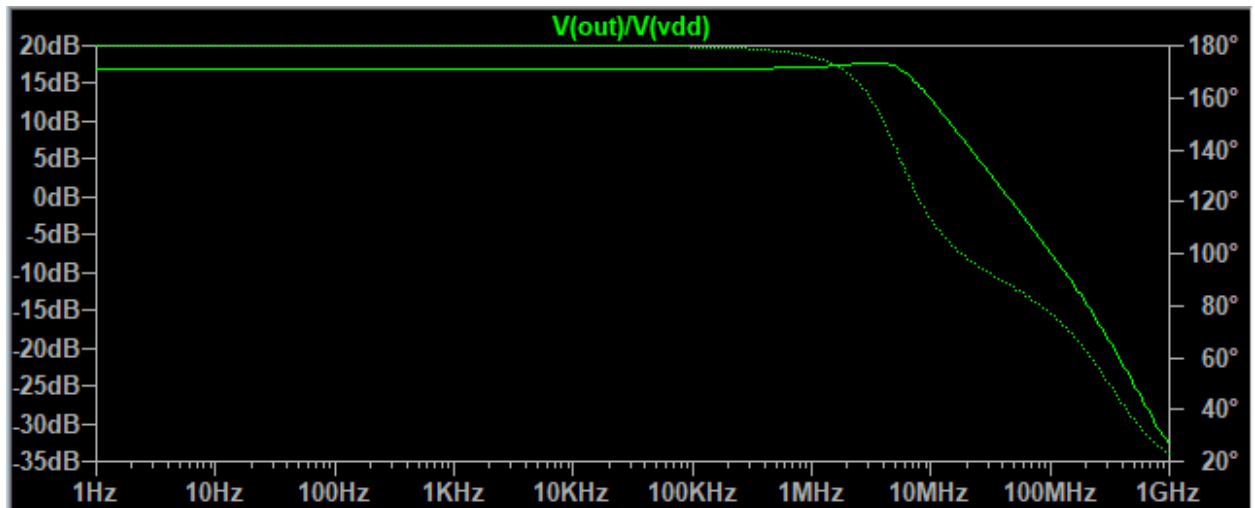
CMRR = 26.88 dB

4) DC Gain



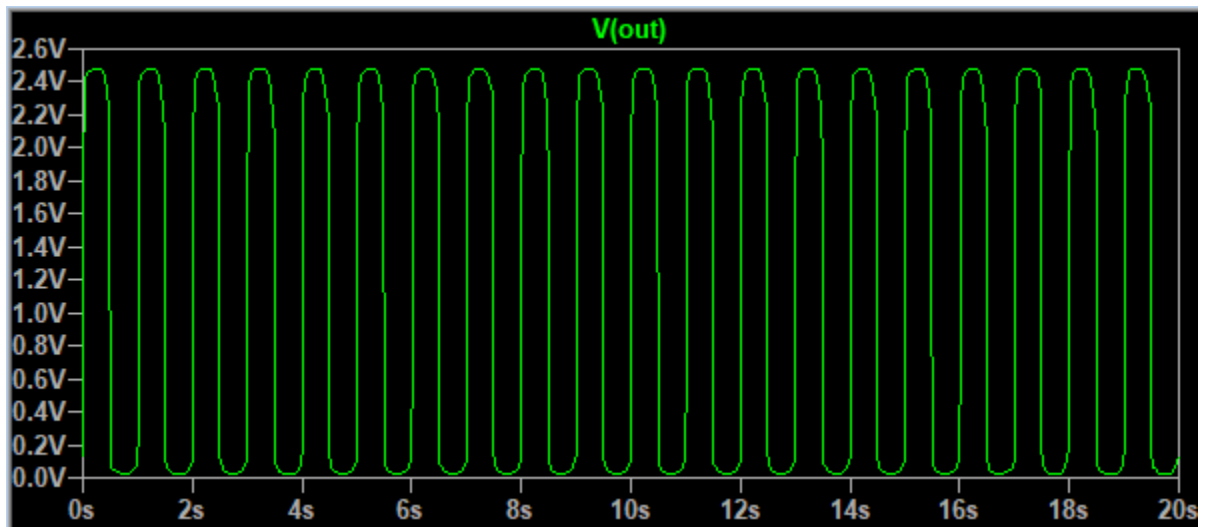
DC Gain = 688.081 (slope of VTC)

5) PSRR



PSRR = 17dB

6) Output Voltage Swing



AC

DC Swing can be seen from VTC (0 to 2.5 volts)

7) Power Consumption

Is(M5): 4.78678e-05 device_current
Is(M4): 4.8014e-05 device_current
Is(M12): 2.3021e-05 device_current
I(bias): 50e-5

Power = 1.547 mW (within the 3mW budget)

8) Input Offset Voltage = 0.5763 volt

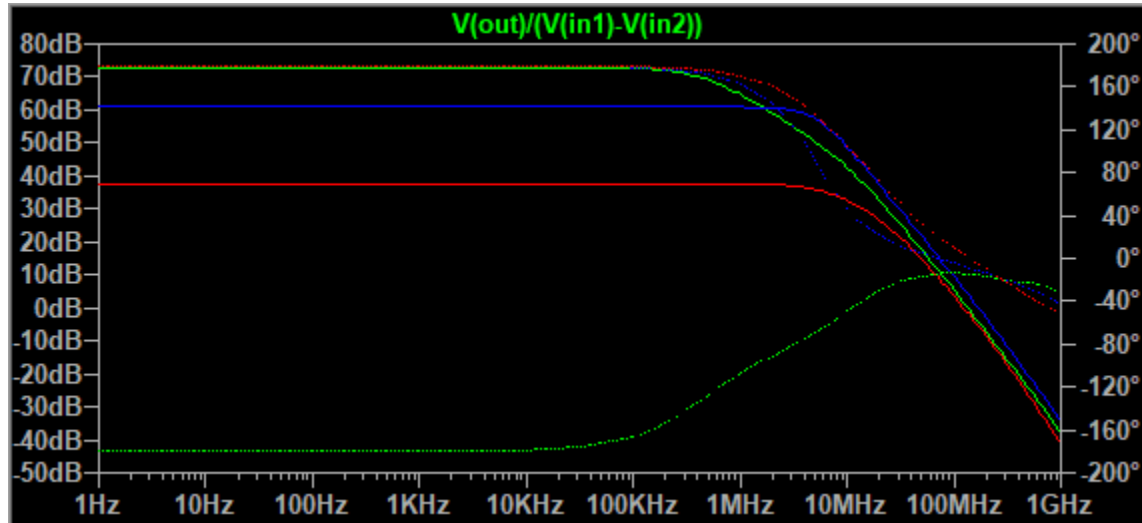
9) Output Offset Voltage = 0.131584 volt

Parameter	Target	Achieved
Open Loop Gain	-	60.9 dB
3dB Frequency	5 MHz	5.248 MHz
ICMR	-	0.952 volt
Power Consumption	<= 3mW	1.547 mW
CMRR	-	26.88 dB
PSRR	-	17 dB
Gain Margin	-	28.60067 dB
Phase Margin	50-60 degrees	79.537 degrees
DC Gain	-	688.081

INNOVATION

- 1) We added a compensation capacitor (Miller Compensation) to obtain such a high 3dB frequency.
- 2) Normally people use Common Drain stage for Output Impedance matching, but we used a Cascode for the same, so that we get both gain as well as output impedance, which helped in setting the 3dB frequency, as cascode offers high Rout.

TEMPERATURE EFFECTS ON Adm



100 degrees

27 degrees

0 degrees