TRIBECA 32-BIT INSTRUCTION SET ARCHITECTURE V1.0

DEC	BIN	HEX
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

	OPCODE					COND	LITERAL	SIGN EXT	TGT REG				OPERAND A				OPERAND B (LITERAL/REG)															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG REG OP	R-R OP					C	0		REG_D				REG_A				0												REG_B			
							1	S									LITERAL															
LOAD	LDR					C	0										0												REG_B			
							1	S									LITERAL															
STORE	STR					C	0										0												REG_B			
							1	S									LITERAL															
SCF	SCF					C	1	0	CSR				CSR				CONDITION CODE															
SWI	SWI					C	1	S	0								LITERAL (ISTP BYTE OFFSET)															
CALL	CALL					C	1	S	0								LITERAL (PC BYTE OFFSET)															
RETURN	RTN					C	0	0	0																							
BRANCH	ADD					C	0		PC				PC				0												REG_B			
							1	S									LITERAL															

REGISTER	USE
0	GP
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	SP
12	ISTP
13	LR
14	CSR
15	PC

OPERATION	OPCODE	DESCRIPTION
MOV	00	MOVE ALL 32 BITS OF OPERAND B TO TGT
MOVH	01	MOVE LOW 16 BITS OF OPERAND B TO HIGH 16 BITS OF TGT
OR	02	BITWIZE LOGICAL INFIX OPERATION
XOR	03	
AND	04	
ADD	05	SIGNED INFIX ARITHMETIC
SUB	06	
LSL	0D	TGT = LOGICAL SHIFT LEFT/RIGHT OF OPERAND A BY OPERAND B BITS
LSR	0E	
ASR	0F	TGT = ARITHMETIC SHIFT RIGHT OF OPERAND A BY OPERAND B BITS
ROR	10	TGT = RIGHT ROTATE OF OPERAND A BY OPERAND B BITS
CMP	11	SETS COMPARISON FLAGS IN CSR
STR	12	STORE Rd TO [Ra+OPERAND B]
LDR	13	LOAD [Ra+OPERAND B] TO Rd
CALL	18	BRANCH TO TARGET AND STORE RETURN ADDRESS IN LR
RTN	19	BRANCH TO ADDRESS IN LR
SWI	1A	CALL ISTP+OFFSET
SCF	1B	SET THE CONDITION FLAG IN THE CSR

REGISTER NUMBER	DESCRIPTION	MODE
14	Control and Status Register (CSR)	R/W*

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CF	WC	C	GT	LT	GT	LT	WF									M3	M2	M1	M0	IR3	IR2	IR1	IR0			AS	E2	E1	E0	RMWM	
	-		-	SGN		USGN		-					0				INTRPT MSK				INTRPT							ENBL			-	
			CFLGS														HARDWARE INTERRUPT CONTROL														RMWM	
READ VALUE	#	1	#					1	0								#														0	0

BIT	DESCRIPTION
1..0	READ MODIFY WRITE MODE FOR BITS 8..0
2	INTERRUPT ENABLE 0
3	INTERRUPT ENABLE 1
4	INTERRUPT ENABLE 2
5	AUTO SWITCH
6	
7	
8	INTERRUPT ON PIN 0
9	INTERRUPT ON PIN 1
10	INTERRUPT ON PIN 2
11	INTERRUPT ON PIN 3
12	INTERRUPT MASK [0]
13	INTERRUPT MASK [1]
14	INTERRUPT MASK [2]
15	INTERRUPT MASK [3]

24	WRITE ENABLE FOR BITS 29..25
25	UNSIGNED LESS THAN
26	UNSIGNED GREATER THAN
27	SIGNED LESS THAN
28	SIGNED GREATER THAN
29	CARRY ON ADD
30	WRITE ENABLE FOR BIT 31
31	CONDITION FLAG

RMWM	VALUE
PRESERVE	00
SET	01
CLEAR	10
WRITE	11
COND SELECT	**VALUE**
EQ	0
NE	1
SLT	2
SLE	3
SGT	4
SGE	5
ULT	6
ULE	7
UGT	8
UGE	9
CARRY	A
NO CARRY	B