EE 287 S'25
Project
V 1.0

This semester, you are designing a FIR filter to be used in an A/D converter. The converter is a delta sigma type. The filter has 512 taps, and is designed for a system with 256X oversampling. The filter is defined by a set of coefficients. The filter is even. There are two samples with the same filter values.

The file fircoefs.v contains the filter coefficients, and a few comments to help you use the coefficients.

The modulator provides 256 1 bit (1/0) samples for each clock period. The filter has a memory holding 512 samples/bits. They are filtered when a signal FILTER is a 1. The FILTER signal may only be high for one clock cycle every 256 cycles, or could be high for longer. It takes 256 clocks to perform the filtering. The filter has 512 taps/coefficients. The design is limited to 4 (four) adders. The coefficient data is 4.24 format signed binary. The additions should be performed to 13.24 (36 bits), and the bits [23:8] (rounded) extracted as the answer. Double buffering of the input will need to be implemented. Bits arrive continuously from the modulator. You will need to keep the old data around while performing calculations.

Interface:

Name	Bits	Dir	Description
Clock	1	In	Rising edge clock
Reset	1	In	Reset all functions, clear memories, and wait for FILTER signal
FILTER	1	In	Start filtering and create output
BitIn	1	In	Single bit from the 256x analog modulator
Dout	16	Out	16 bit ADC output
Push	1	Out	Data is present on output

Pass Simulation, and Synthesize the design for operation at 512 MHz.

Limited to 4 adders (>24 bits) total.