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High aspect ratio micromachining (HARM) technologies for microinertial devices

M. McNie, D. King, C. Vizard, A. Holmes, K. W. Lee

Abstract In this paper, we review work on novel, high aspect processes for microinertial components at the Defence Evaluation and Research Agency (DERA). High aspect components may lead to significant cost-performance improvements in both accelerometers and gyroscopes. We have evaluated 3 low temperature process technologies – silicon on insulator (SOI) HARM, UV electroforming and bulk HARM. Prototype microinertial devices fabricated in these technologies are also presented. The potential of the processes for integration with on-chip CMOS electronics is assessed which may be either as part of a fully integrated MEMS process or as "value-added" post-processing on commercial CMOS wafers.

Bonded SOI (BSOI) materials has been specially designed for micromachining applications to give a low stress material that is optimised for a sacrificial release process. Trench isolation is achieved by deep dry etching to the buried dielectric. These trenches may be refilled to allow metallisation to reach isolated components. Structures with aspect ratios of up to 50:1 have been realised using a combination of photolithography, deposition and deep dry etching. CMOS compatibility has been demonstrated. The process is an attractive manufacturing technology. Electroforming of nickel in resist moulds formed using conventional UV photolithography has also been investigated. Some of the early limitations with this technology have been overcome by using a new resist technology, SU8. The process needs to mature further, but remains a promising candidate. Bulk HARM uses deep dry etching of a bulk silicon membrane which is defined using wet etching. Device isolation is difficult and process control complex making this the least attractive of the technologies.

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1 Introduction

There is currently much interest world-wide in developing microinertial components [1], primarily for a broad range of relatively low performance applications, such as vehicle dynamic control systems. To date, standard IC fabrication technology has been the primary enabling technology for the development of micromechanical systems. Typically, polysilicon sacrificial surface micromachining (SSM) or traditional bulk micromachining (TBM) have been used to fabricate microinertial devices.

Many advantages result from using high aspect ratio micromachining (HARM) technologies that offer added flexibility in 3 dimensions. In HARM, mechanical structures and trenches are fabricated which have large depths when compared with their widths. SSM and TBM are typically limited by practical considerations to features with a maximum aspect ratio of about 5–10. Here we demonstrate aspect ratios of between 10 and 50. This high aspect reduces unwanted cross-axis coupling, may increase capacitance in electrostatic devices, maintains high packing density as in SSM and allows thick, high mass elements to be formed for good sensitivity as in TBM – all key drivers for microinertial components in terms of performance.

For microinertial device performance to increase with the same size of device and to miniaturise the microsystem, it may be desirable to move from a hybrid solution to a fully integrated monolithic device. For this reason, we have restricted the HARM technologies discussed to CMOS compatible or potentially CMOS compatible processes with silicon as a substrate material.

2 Fabrication processes

2.1 SOI HARM

A simple, single mask process flow for SOI HARM is shown in Fig. 1. The start material is BSOI wafer. A variety of low stress, anti-stiction SOI layers and dielectric structures have been designed for micromachining applications at DERA (patent pending) and bonded by BCO Technologies. This gives a uniform 25–100 μm thick, single crystal

bonded silicon layer with a buried dielectric on a silicon handle. The thickness range was chosen as a compromise between performance, ease of processing and throughput whilst still behaving as if a bulk substrate from the point of view of CMOS circuitry.

The wafers were patterned using either a photoresist or an oxide mask and etched in a Surface Technology Systems advanced silicon etch (ASE) system [2]. This system uses the Bosch process chemistry [3] in a high density, low pressure inductively coupled plasma to etch silicon at rate of up to 2.5 μm/min with anisotropic profiles. A timed chemical etch was employed to yield suspended micromachined structures at the same time as leaving large footprint structures anchored to the substrate.

More advanced process flows include etching to preformed voids, implanting for piezoresistive pick-off, metallisation and electrically linking mechanically isolated parts. In order to make electrical contact to parts which may be mechanically isolated by deep trenches, it is necessary to provide a path for the interconnect – the quality of the refill is not critical and some voids may be tolerated without significantly degrading device performance. Rather than use a high temperature refill process, such as LPCVD nitride or polysilicon, that would degrade transistor characteristics and could not be used to post-process on commodity metallised CMOS wafers [4], we have developed a low temperature (<450 °C) process based on PECVD dielectric refill at the top of trench. Metal tracks may be deposited over this bridge and patterned as interconnect – again at low temperatures. Contact is made to the desired structures by etching contact windows in the insulating dielectric layer.

2.2 UV electroforming

A potentially cheaper alternative to LIGA and SOI HARM is UV electroforming. As shown in Fig. 2, a mould is formed on a seed layer (typically copper or titanium) on wafer using conventional UV lithography. The wafer is then placed in an electroforming bath and the mould filled to the desired depth with metal (in this case, nickel). The resist is removed to leave micromechanical nickel structures. In order to produce freely suspended structures, the surface of the wafer may be patterned with a polymer sacrificial layer under the seed layer and removed at the same time as the mould.

In conjunction with Imperial College, we have investigated the use of this technology to produce electroformed nickel microinertial structures. CMOS compatibility does not necessarily result from the low temperature process as contamination and applied electric field remain issues. It should be possible to overcome this by incorporating suitable protection layers over the electronics.

2.3 Bulk HARM

TBM cannot achieve vertical sidewalls in a standard [100] silicon substrate. This leads to a reduced the packing density when compared with other HARM technologies. Special passivation layers are also needed to protect the CMOS circuitry during the wet etch. A typical bulk HARM process flow to overcome the vertical sidewall limitation is shown in Fig. 3. A membrane is defined from the back of the wafer using an anisotropic wet silicon etchant (in this case, TMAH for CMOS compatibility). Deep dry etching

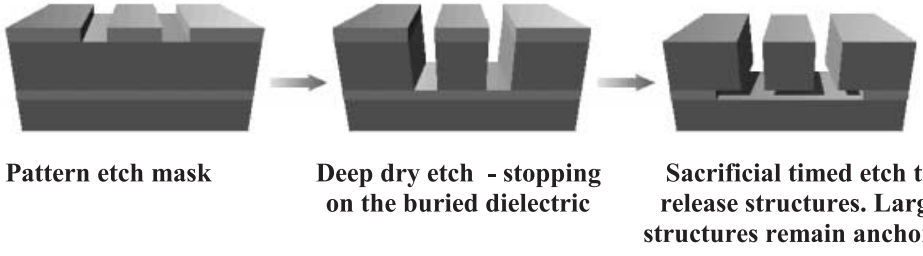

Fig. 1. Schematic of simple SOI HARM process

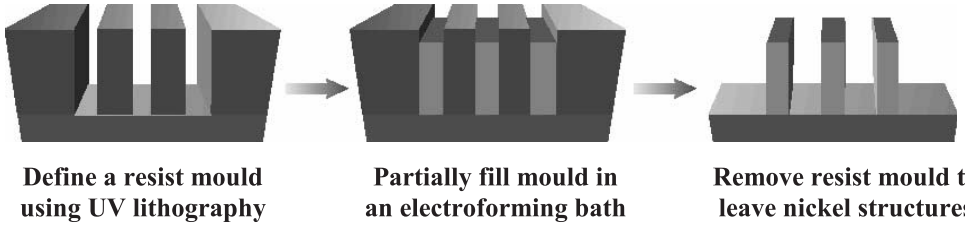

Fig. 2. Simplified schematic of a UV electroforming process

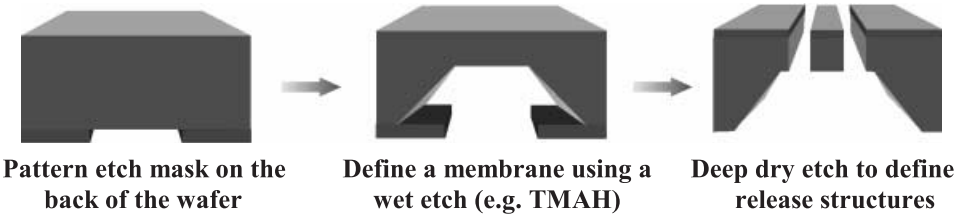

Fig. 3. Simplified schematic of a bulk HARM process

may form high aspect features form the front of the wafer when etching to define and release structures in the membrane. An equally viable, potentially more manufacturable process flow would be to deep dry etch first to define the structures and then to form the membrane and release structures using the wet etch.

3
Results

3.1
SOI HARM

We found that it was important that the device design, etch process and mask were optimised for good uniformity in order to reduce or eliminate the effect of notching at the base of a trench (Fig. 4). This was attributed to charging and to an increase in the fluorine concentration at the dielectric interface. These combine to break down the sidewall passivation. A multi-step etch process with extra passivation in the breakthrough phase has also been used to further reduce this effect. Surface Technology Systems have recently announced an upgrade to their ASE etch system (under assessment at DERA) which should drastically reduce charging effects and hence any potential notching.

A ring gyroscope structure fabricated in this process [6] is shown in Fig. 5. A resonant accelerometer has also been developed in conjunction with Druck in 100 μm thick BSOI with a noise equivalent floor of 0.5 mg and a frequency shift of 50 Hz/g. Figure 6 shows SOI HARM devices with integrated CMOS electronics on the same substrate. As we have previously reported [5], this low temperature process is fully CMOS compatible. A bridged trench with metallisation is shown in Fig. 7. We are investigating using dual frequency PECVD deposition to improve penetration of the species into the trench. The impact of these dielectrical/metal bridges on reliability has yet to be assessed.

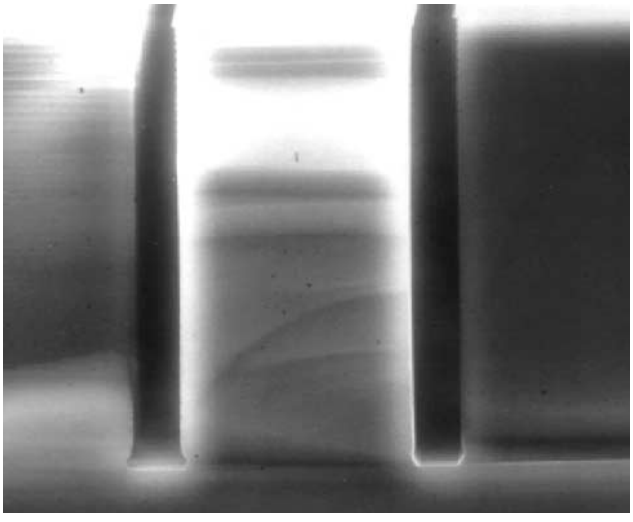

Fig. 4. Notching at the dielectric interface in an unoptimised process – trenches are notched (left) whilst slightly underetched (right)

3.2
UV electroforming

Devices have been successfully fabricated with depths of up to 20 μm and aspect ratios of up to 10 (Fig. 8). In our original process, the sidewall profiles were not ideal and tapered slightly inwards with depth. The effect of these trapezoidal profiles on device performance has been assessed [6]. Notably, it will lead to a sizable out-of-plane component of the motion when using electrostatic actuation. We believe that this problem may be largely overcome by moving to alternative thick resist technologies, such as Epon SU8. We are currently evaluating SU8 as a mould for electroforming. SU8 offers much thicker layers (20 μm to >100 μm) in a single spin with almost vertical side walls and aspect ratios up to 20 (Fig. 9). We are seeking to improve the SU8 mould removal process. Current results indicate a slight variability in the resist process over time and between batches of resist, requiring

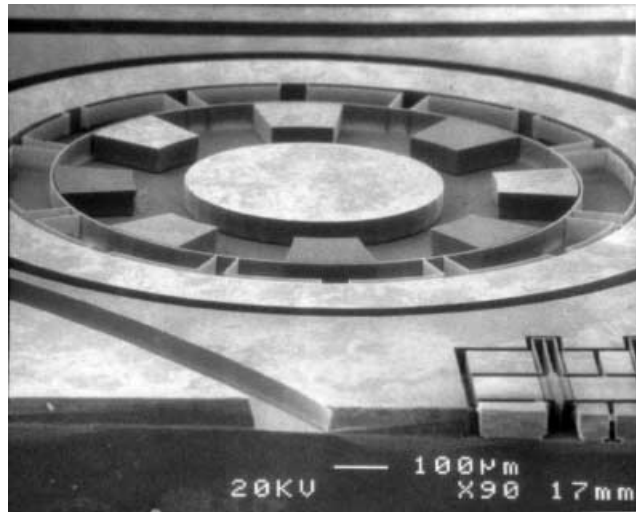

Fig. 5. 100 μm deep, 1 mm diameter BSOI gyroscope

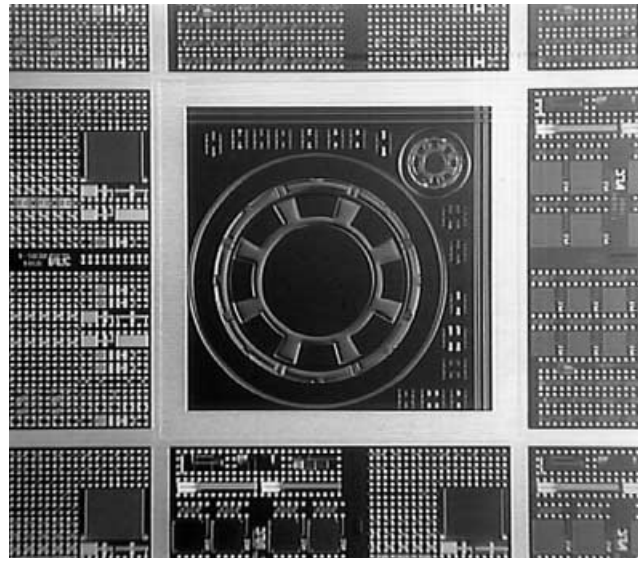

Fig. 6. SOI HARM structures post-processed on a substrate 2 μm CMOS

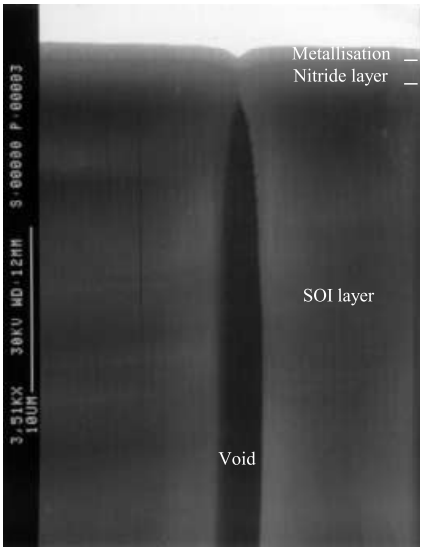

Fig. 7. 100 μm deep trench bridged by low stress silicon nitride and surface metal

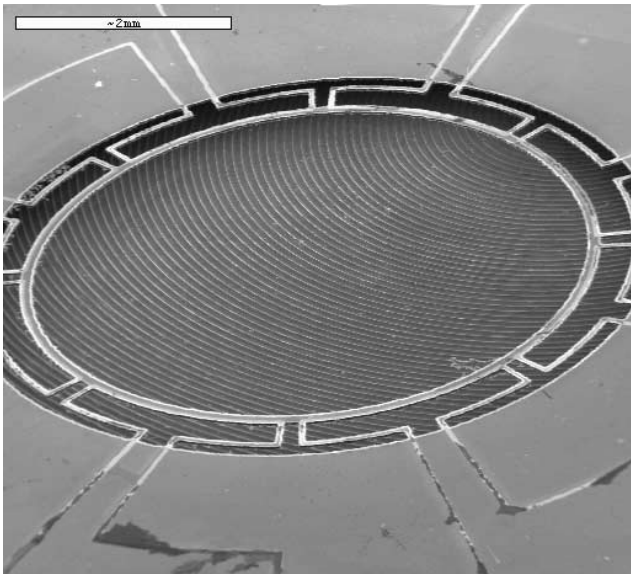

Fig. 10. Electromagnetic bulk ring gyroscope

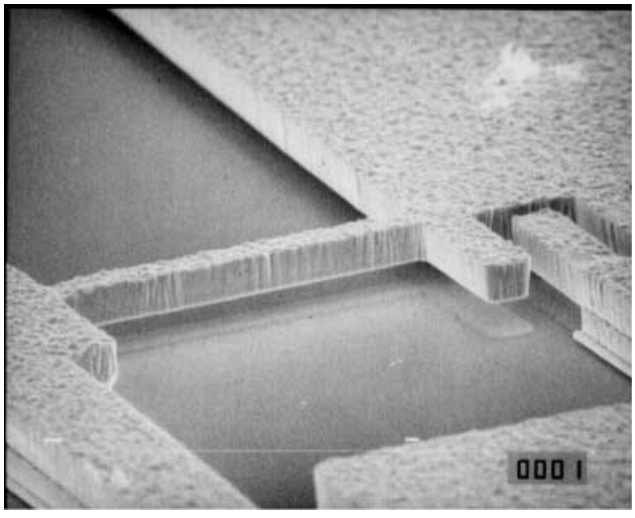

Fig. 8. 20 μm deep electroformed nickel structures

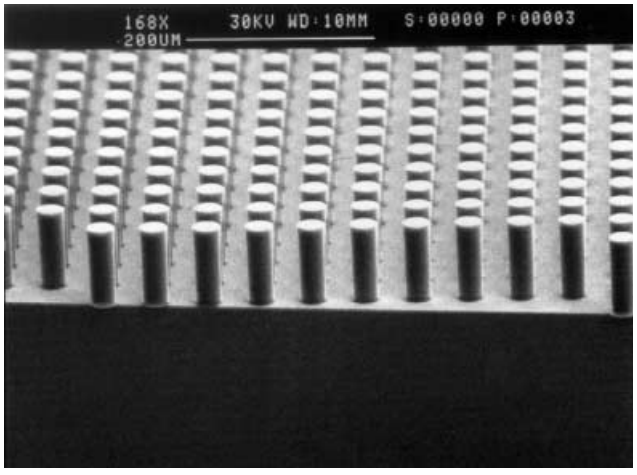

Fig. 9. 25 μm deep columns fabricated in SU8 resist

optimisation of exposure times on each run. This is a potential issue if the technology is to be commercialised in a production environment, but is likely to be addressed in the near term by the manufacturer.

The nickel layers formed need further optimisation to reduce the internal stress and hence make the large devices required for microinertial components. Slight modifications to the bath chemistry and conditions should alleviate the problem. Despite these limitations, the savings from using standard microelectronics industry tools for patterning and the use of batch processing in electroforming baths mean that this technology may develop into a significant challenger as a commercial manufacturing process.

3.3 Bulk HARM

Figure 10 shows a ring gyroscope fabricated in a 30 μm deep membrane in [100] bulk silicon with electromagnetic actuation as part of joint DERA-University of Newcastle activity [8]. Precisely controlling the thickness of the membrane was found to be difficult using a timed etch. Etch stop mechanisms, such a boron implant etch stop may not be CMOS compatible and tend to induce unwanted stress. Moreover, TMAH does not have as good a selectivity to the etch stop as other common etchants, such KOH and EDP.

Machining in the bulk of the substrate places constraints on devices. Isolation is difficult – diode isolation may be utilised, but to reduce leakage high resistivity substrates are used – in conflict with standard CMOS. The sense and actuation mechanisms available are also limited. For example, electromagnetic mechanisms require extra thin film metal and isolation layers on the released structures. This results in a non-homogeneous mechanical layer that may induce unwanted stress and adversely impact reliability. Similarly, piezoresistive pick off requires non-standard implants.

4
Conclusions

SOI HARM is a simple, high yielding process with a well controlled, highly reliable crystalline silicon layer and looks a very promising candidate for mass production of microinertial components with an improved performance-cost ratio. The ability to make fully integrated components has already been demonstrated.

UV electroforming with an improved resist technology and the simple electroforming batch process also looks to be a promising candidate. However, it is less mature than SOI HARM. Stress, fatigue and reliability remain unresolved issues in electroformed structures. In resonant components, quality factors are likely to be lower than in silicon.

Bulk HARM has several disadvantages when compared with the aforementioned processes in terms of process complexity, process control, packing density and device isolation for realising high aspect microinertial components. However, it is a fairly mature technology and the drawbacks are alleviated somewhat if a hybrid approach is adopted and CMOS compatibility is not required.

All the processes investigated were low temperature and could potentially be used to post-process MEMS devices on commodity metallised CMOS or BiCMOS wafers. This has the fourfold advantage of risk reduction, providing "value-added" functionality to standard state-of-the art microelectronics, reducing the overall size of the integrated microsystem and potentially improving performance.

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