Microsystem Technologies 3 (1996) 20–27

Etching processes for High Aspect Ratio Micro Systems Technology (HARMST)

R. Kassing, I. W. Rangelow

Abstract This paper reports on the development of a dry etching based HARMS-Technology which will offer the potential to manufacture micro-engines, micro-turbines, micro-sensors, micro-actuators, and electronic circuits onto a single silicon IC chip. This technology is based on the highly anisotropic and selective dry etching of Si-monocrystals. The suitability of reactive ion etching for the fabrication of micro electro mechanical systems (MEMS) has been evaluated by characterising the change of lateral dimensions vs. depth in etching deep structures in silicon. Fluorine, chlorine and bromine containing gases have provided the basis for this investigation. A conventional planar RIE (Reactive Ion Etching) reactor has been used, in some cases with magnetic field enhancement or ICP (Inductive Coupled Plasma) Source and low substrate temperature. For reactive ion etching based on Cl_2 or Cl_2/HBr plasma a slightly "positive" (top wider than bottom) slope is achieved when etching structures with a depth of several 10 μm, whereas a "negative" slope is obtained when etching with an SF_6/CCl_2F_2 based plasma. Pattern transfer with vertical walls is obtained for reactive ion etching based on SF_6 (with O_2 added) when maintaining the substrate at low temperature (in range $\approx -100\,^{\circ}C$). Further optimisation of plasma chemistries and reactive ion etching procedures should result in runouts in the order or 0.1 μm/100 μm depth in Si as well as in organic materials. Etching processes for HARMST is demonstrated in the realisation in Si microturbine. Axes or stators (nonmoving parts) are etched into the initial Si-wafer. The movable parts (rotors, beams, etc.) are prepared from electro-chemically etched Si-membranes with defined thicknesses that, all movable parts are created lithographically on the SiN_xO_y surface. This is followed by dry etching the monocrystalline Si-membrane down to the SiN_xO_y sacrificial layer on the back side of the membrane by an RIE-process. The wafer with the movable parts is flipped onto the wafer with the already etched axis and then positioned and centred. The SiN_xO_y-sacrificial layer is then dissolved by a chemical wet or vapour etch process. Subsequent bonding with a Pyrex glass wafer seals the parts.

Received: *30 October 1995/Accepted*: *20 May 1996*

R. Kassing, I. W. Rangelow
Institute of Technical Physics, University of Kassel,
Heinrich-Plett-Strasse 40,
D-34109 Kassel, Germany

Correspondence to: R. Kassing and I. W. Rangelow

We wish to thank P. Hudek (Academy of Science, Bratislava), Z. Borkowicz (Tech. Univ. of Wroclaw), and Dr. M. J. Cooke (Oxford Instruments, Yaton) for their contribution to this work. We like to thank Dr. K.-N. Leung from Lawrence Berkeley Laboratory for helpful discussions. Special thanks to J. W. Coburn for his encouragement.

1 Introduction

In recent years the development of micro-robot technology has been hampered by the absence of a method to integrate micro-motors, -turbines, -sensors, -actuators and electronics onto a single micro-chip. Very often several technological processes are used to manufacture the individual parts, which are subsequently mounted to form a hybrid micro-system. The manufacture of micro-structures demands etching processes of extremely high selectivity and anisotropy without which the production of structures of very large aspect-ratio would not be possible. An additional demand of such etching processes is the protection of vertical walls and residue-free surface during etching at extreme depth. With the aid of various technologies, electrostatically or magnetic field-driven micro-motors and -actuators have been manufactured successfully.

For the high volume fabrication of Micro Electro Mechanical Systems (MEMS) "high aspect ratio micro structure technology" must be developed for a large variety of materials. Using synchrotron based X-ray lithography, a lateral run-out of only 0.1 μm for 100 μm depth has been demonstrated when using PMMA organic resist materials [1]. As is well-known, the commerically used LIGA (German acronym for Lithographie, Galvano-formung, Abformung) process, which uses synchrotron X-ray lithography, electroforming, and plastic moulding as the major process steps, is highly successful in fabricating microstructures. These microstructures have extremely high structural heights (several hundred micrometers) and lateral dimensions down to 1 μm [1]. The structures consist of different materials such as plastics, metals, ceramics or combinations of any of them.

A lower-cost alternative to the LIGA process is based on the structuring of photosensitive polyamide [2]. However, this process has lower manufacturing costs than the LIGA process, but cannot match the aspect ratio performance of the LIGA process. The realisation of this "low cost" technology does not demand any nonconventional equipment (i.e., it can be set up in any conventional clean-room).

Refs. 3 and 4 demonstrate processes for serial mounting of micro-mechanical devices produced with the aid of dry etching, anodic bonding, and wet etching. This technology

permits the production of micro-electro mechanical systems consisting of electro-static micro-motors, toothed wheels, and axes. The movable micro-elements were produced by lithography and dry etching (5–10 μm deep) in a highly boron-doped layer and subsequently freed in EDP-solution. The dry etching process was carried out in a SF_6/CCl_2F_2-plasma. This results in a 10% under-etching and relatively smooth, almost completely vertical walls of the micro-structure. Prior to etching the parts in EDP (Ethylene-Diamine Pyrocatechol), anodic bonding on a glass plate takes place. In this way integration with integrated circuit (IC) manufacture is impossible. The SCREAM-II called technology is far more refined [5]; this develops capacitive, two-dimensional actuators from mono-crystalline GaAs. The lateral dimensions are in the sub-micron range with an aspect of 25. The technology process is based on CAIBE (Chemically Assisted Ion Beam Etching), RIE and PECVD. The exceptionally high selectivity of the CAIBE-process is a decisive contribution towards the realisation of this technology. The advantage of this technology is its compatibility with technologies used for opto-electronic parts and circuits. However, neither of the above-mentioned processes can manufacture structures of comparable quality directly in silicon.

In order to realise more compact and low cost MEMS fabrication techniques the combination of lithography and reactive ion etching (LIRIE) techniques has been proposed [6, 7]. The use of scanning electron beam lithography is of advantage for prototyping and low volume fabrication. Optical and masked ion beam proximity printing may be implemented for high volume production, however, masked ion beam lithography (MIBL) providing superior exposure latitudes and huge depth of focus capabilities.

The use of reactive ion etching has the advantage of high silicon to mask selectivity for a large variety of organic [7] and inorganic mask materials. Si [6], and SiO_2 [8] may be patterned, thus – and in combination with electroplating [9] – meeting quite diverse MEMS requirements.

In this paper, we will propose an even lower cost process for silicon structure transfer that can achieve much of this, and with lateral dimensions well under 1 μm. This offers the possibility of the formation of a Mircrosystems consisting of many different microstructures, including movable ones, all onto a single silicon micro-chip. The manufacturing concepts presented here is based on the extending of already existing IC technology for conventional microelectronic devices, manufactured by already existing tools.

2 Dry etching

This paper presents experimental results of investigations of mechanisms which determine the anisotropic character of deep silicon etching using plasma-assisted etching. The profile and lateral undercut of the trenches were observed and evaluated by scanning electron microscopes. Important theoretical considerations and computer simulations contribute towards profile development, selectivity, etch rates, as well as prediction of on-going side effects [14–26]. Selecting the correct dry etching technology is the decisive step towards realising dry etching, and this was discussed and demonstrated in previous publications [6, 22]. Generally, the ratio of ion flux and radical flux is the deciding factor to produce anisotropy. High anisotropic etching is driven by ion assisted reactions on the bottom surface, but anisotropy is limited by radical side-wall reactions which cause undercutting. Because the reaction probabilities of chlorine or bromine radicals (energy of 0.05 eV) are very small, such plasmas can be used for providing high anisotropic processes. The ion bombardment induced chemistry on the bottom is driven by ions with energies down to even as low as 25 eV, but the sidewalls are beneficially "protected" against reaction with radicals by absorbed atoms of non-fluorine halogens.

Today the requirements for pattern transfer applications in the VLSI fabrication are becoming ever more stringent. Etching of deep trenches in mono-crystalline Si was established while developing the storage-trench-capacitor [17]. Cl- or Br-containing plasmas were chosen and not an F-containing plasma, in order to avoid undercutting due to F spontaneous etching. Employment of F-containing plasma requires special techniques (Side-Wall Passivation – SWP) to reduce the undercutting. Deep-trench etching technology was applied successfully in the manufacture of 15 μm thick Si-hole-masks for electron- and ion-projection lithography as well as the etching membranes for pressure sensors [18]. The requirements of the etching process for micro-mechanical applications are: High-aspect/ratio structures $>1{:}30$, high etching selectivity >100, controlled side-wall slope and an IC-technology-compatible masking technique.

In order to obtain high aspect ratio structures with reactive ion etching, the ratio of ion flux and radical flux is of decisive influence: Highly anisotropic etching is driven by ion assisted reactions at the bottom surface, but is hindered by undercutting caused by reactive radical induced side-wall reactions. When aiming for high aspect ratio structures, miscellaneous phenomena occur which are not commonly observed when etching low aspect ratio ($<3{:}1$) features. The most significant of these are aspect ratio dependent effects such as RIE-lag, bowing (barrelling), facetting, micro-trenching and profile shape dependence (Fig. 1). These effects are caused by several mechanisms:

– angular dispersion of ions and (etchant) neutrals due to collisions within the plasma sheath [10, 11, 20],
– ion and etchant transport within the feature onto the sidewalls [12, 26],

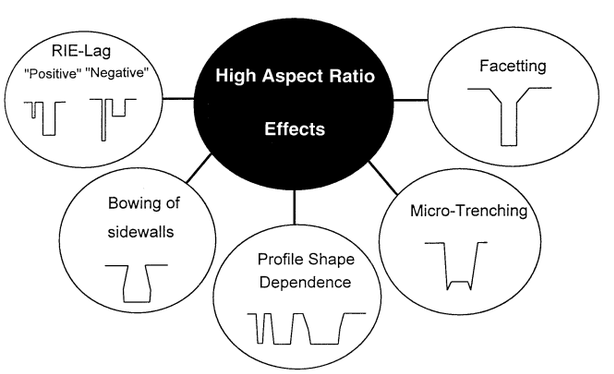


Fig. 1. Schematics of etching profiles influenced by different high aspect ratio RIE effects

– depletion of the reactant (microscopic loading) under conditions of high probability at the surface [10],
– charging of feature sidewalls, as local charging of substrate surface or micro structure sidewalls can deflect ions and thus may prevent them from reaching the bottom surface to be etched [13],
– etching yield dependencies upon the angle of incidence [14, 19]
– deposition of material produced in the discharge within the feature [16],
– redeposition of material released by ion-induced etching (reaction of the neutrals on the sidewalls to form passivation layers [17, 26].

The choice of gas phase chemistry, pressure conditions (ion bowing in the sheath), reactant transport to the surface, and product transport away from the surface have been identified as the key factors for controlling the microscopic etch uniformity in the high aspect ratio etching. In order to reduce the above listed detrimental effects, we have concentrated our efforts on two main etching strategies: (i) controlled formation of sidewall-inhibitor films, and (ii) reactive ion etching at low substrate temperatures.

2.1
Reactive ion etching with Cl and Br containing plasma chemistry

Reactive ion etching based on Cl and Br plasma chemistries may achieve highly anisotropic structures due to the low reaction probabilities of chlorine or bromine radicals with Si at room temperature. The etching is driven by ion bombardment induced chemistry at the bottom surface, where an ion energy as low as 25 eV is sufficient. The sidewalls are covered and thus protected by radicals of absorbed atoms/molecules of non-fluorine halogens.

Plasmas such as BCl_3/Cl_2, BCl_3/Cl_2/HBr, CF_3Br/Br_2, and Ar/HBr/Br_2 proved to be most suitable. In the case of etching Si in Cl_2/BCl_3 plasma, etch products like SiCl, $SiCl_2$, $SiCl_3$, or $SiCl_xB_y$ have high reactivity, exhibiting a great tendency to redeposit onto the sidewalls (Fig. 2a). These unsaturated etch product radicals are highly reactive and thus react with oxygen available from the gas environment and due to sputtering of an SiO_2 masking layer. At the initiation of the etching process the gas phase concentration of these radicals is low but rises during further etching. The resulting high gas phase concentration leads to high density of $SiCl_x$ related radicals on the planar Si surface. Oxygen will more readily assault these unsaturated etch products than the halogenated Si surface which is essentially passivated. Therefore, oxidised etch products deposited onto the wafer surface lead to "black silicon" development [17]. To avoid the "black silicon" formation a two-step etching processes is necessary. The first step is etch initialisation, which practically means surface scavenging. The surface of the silicon should be clear of native oxides, water, and other contaminants. This is realised by using BCl_3 plasma, which is the best scavenger for these types of contaminants, before the main etch step is started with bromine or chlorine. During the main etch step it is necessary to prevent surface contamination, which originates in the sputtering of the mask or chamber walls. When the concentration of BCl_3 is too high, then the selectivity is reduced. The difficulty in this process

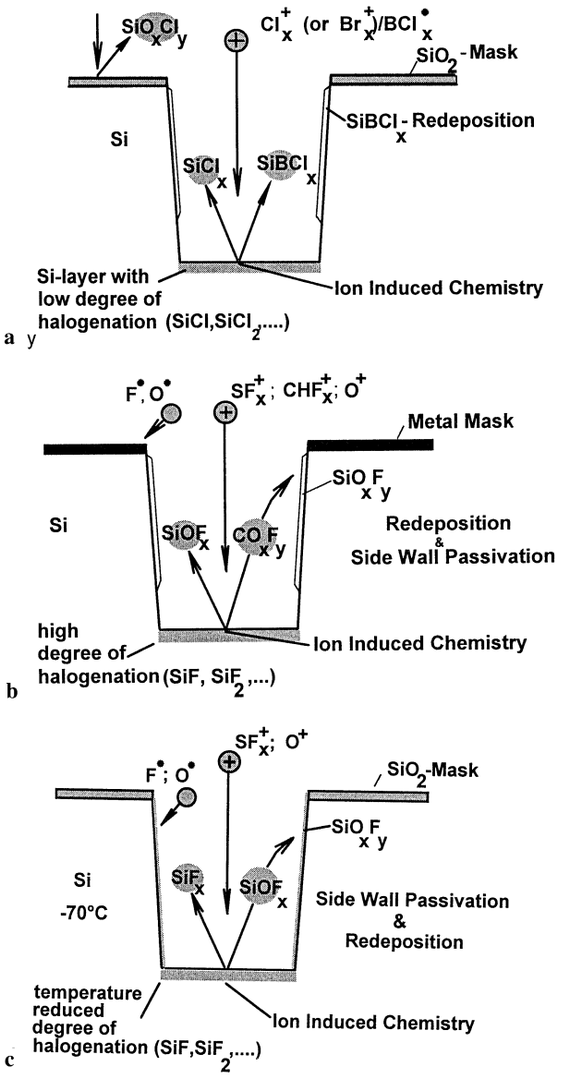


Fig. 2a–c. Etching chemistry schematics of **a** RIE etching of Si with Cl_2 (or Br_2)/BCl_3; **b** RIE etching of Si with $SF_6/O_2/CHF_3$; and **c** Low temperature RIE etching of Si with SF_6/O_2

is to keep the concentration of BCl_3 optimal without at the same time reducing the selectivity, and to prevent the developing of microscopic silicon pillars or "black silicon" by micromasking. In some cases the micro-masking can lead to the formation of micro pin-holes [22].

These plasmas permit an etch selectivity of Si to the SiO_2-mask layer in excess of 100, for ion energies in the range of 30 to 80 eV. The etch rate for Si is in the range of 100–300 nm/min. Practical micro-mechanical application requires that an etching produce nearly vertical walls. To obtain this, an over-etching of 50–150% is employed. For BCl_3/Cl_2, plasma, walls with an 88.6°-angle have been attained. However, over-etching can cause the development of "facets" at the upper structure-edge, and/or "trenching" at the bottom edge. As with most highly selective etching processes, the occurrence of "black silicon" is a frequent effect. In addition to

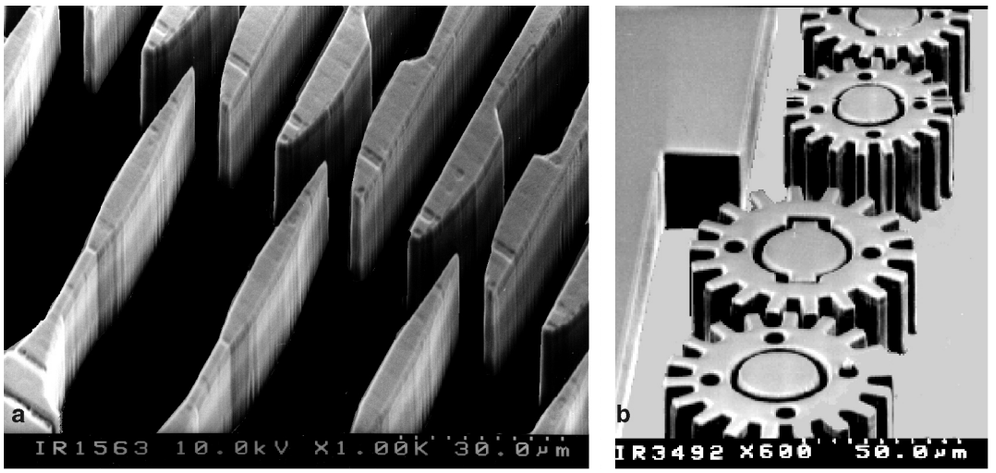


Fig. 3a, b. High aspect ratio structures etched into Si with $Cl_2/HBr/BCl_3$ plasma chemistry at 20 °C using a TEOS-oxide masking layer. **a** array of Si-micro-plugs etched in 16 µm thick Si-membrane. Si etch rate was 280 nm/min, selectivity 25:1 (1,3 µm thick TEOS); **b** etching depth is 38 µm. Si etch rate was 310 nm/min, selectivity 25:1, (2.5 µm thick TEOS)

the choice of gas phase chemistry, ion scattering (bowling) in the sheath, enhanced reactant transport to the surface, and product transport away from the surface have been considered to be the key for controlling the microscopic etch uniformity.

The scavenging step is also enhanced by increasing the power (DC-bias). During the main etching step in Cl_2/BCl_3 plasma it is necessary to prevent surface contamination due to sputtering of the masking layer or due to material originating from the chamber walls. The SiO_2/Si etching selectivity is degraded when using substantial BCl_3 concentration, thus the concentration of BCl_3 has to be optimised (∼15%) to achieve sufficient selectivity and at the same time suppress "black silicon" formation. Using ion energies in the range of 30 eV to 80 eV a SiO_2/Si etch selectivity of >100 could be achieved when using RIE with magnetic field enhancement. The etch rate for Si was between 100 nm/min and 300 nm/min. Figure 3 shows structures etched in Si with $Cl_2/HBr/BCl_3$ based plasma chemistry.

By chopping the BCl_3 gas flow in periods of 200 sec the formation of oxidised unsaturated halogenated film onto the bottom surfaces may be prevented [21]. During the main etching step with gas chopping, an etch rate of 180–230 nm/min could be achieved; whereas in the case of permanently adding BCl_3 to Cl_2 the etch rate was 270–320 nm/min. The most important improvement is a reduction of RIE-lag effects was shown in (Fig. 4) [21]. This is due to the removal of oxidised unsaturated products during the periods where the BCl_3 flow is switched on.

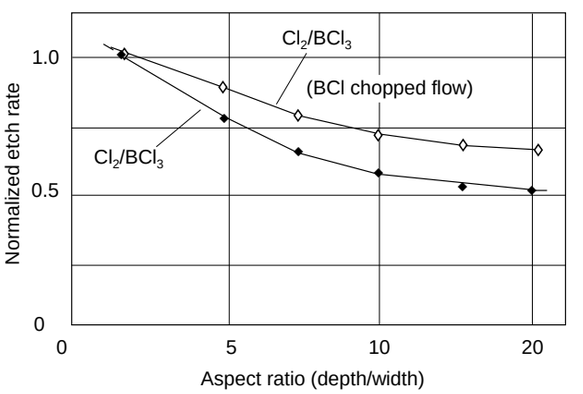


Fig. 4. Aspect ratio vs. normalized (vertical/transverse) etch rate for RIE etching of Si with Cl_2/BCl_3 with permanent and chopped (200 s) BCl_3 flow demonstrating a reduction of RIE-lag effects

2.2
Reactive ion etching with F-containing plasma chemistry

Following the same basic principles also in fluorine containing plasmas very high aspect ratio microstructures may be produced (Fig. 2b). Using an SF_6 plasma, Si etch rates of 1 µm/min may be achieved even at low rf power densities of 0.05 W/cm^2. This is due to the high reaction probability of fluorine with silicon which is much higher than the probability of a reaction between Si and any of the other halogens (Cl, Br, I) [20, 22]. Subsequent to a scavenger step the anisotropic main etching process is based on a SiO_xF_y films which is sputtered from the bottom surface and redeposited onto the side walls. This process is possible by adding oxygen to SF_6 based plasmas. To prevent the formation of black silicon due to oxidation of the slightly halogenated bottom silicon surfaces [17, 21], scavenger gases such as CHF_3 are added to the plasma. It is mandatory to maintain defined substrate temperatures in order to achieve process reproducibility. In this process, "hard" masking layer materials (Cr, Ni, Al, or SiO_2) can be used, the proper material selected to be compatible with an IC-fabrication process. Using such materials mask-to-Si etch selectivitys of 300:1–1000:1 have been achieved. Figure 5 shows high aspect ratio (>25) structures with a depth of 7.5 µm etched into Si with $SF_6/O_2/CHF_3/Ar$ using a 0.1 µm thick Cr film mask.

Reactive ion etching processes with a "soft" masking layer have also been established. Deep trenches in single crystal

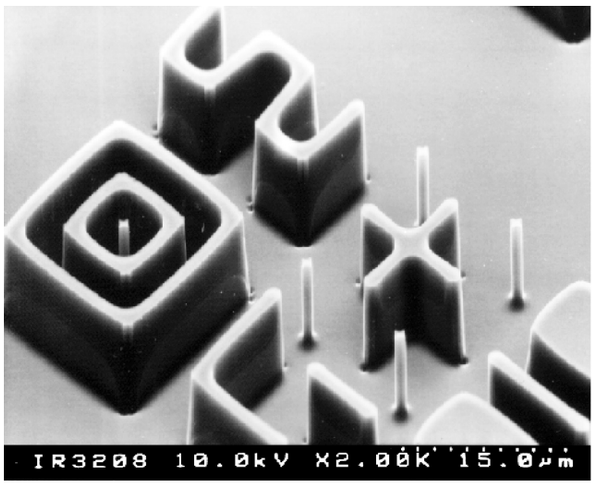


Fig. 5. High aspect ratio (≈ 25) structures etched into Si with $SF_6/O_2/CHF_3$/Ar plasma chemistry at 20 °C using a 0.1 µm thick Cr film masking layer. Etching depth is ≈ 7.5 µm. Si etch rate was 340 nm/min

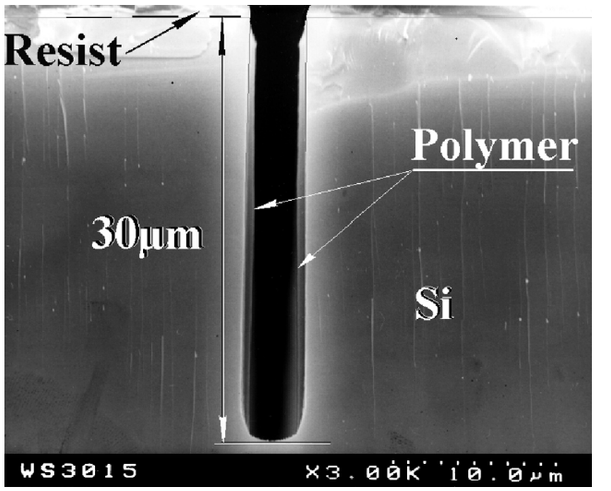


Fig. 6. Etched Si trench obtained with side wall polymer using a 2.5 µm thick AZ4562 resist mask. RIE etching based on (65% SF_6 + 30% CCl_2F_2 + 5% Ar) plasma chemistry. Si etch rate was 450 nm/min, selectivity 30:1

silicon have been realised with AZ photoresist masks and RIE based on $SF_6/C_2Cl_3F_3$ [26], SF_6/CCl_2F_2/Ar [22] or $SF_6/C_2F_8/O_2$ [21] plasma chemistries have been produced with high etch rates of $\geqslant 1$ µm/min and resist to Si selectivities of 20:1 to 50:1 [21, 22, 26]. Here the formation of the protectic side-wall layer is governed by quite different mechanisms: Polymers are generated on the photoresist surface in the presence of active species from the plasma and are redeposited to the side walls by ion sputtering. The polymer passivation film is visible in the SEM micrograph of Fig. 6. This example was obtained with a 2.5 µm thick photoresist mask (AZ4562). The operating pressure of the gas mixture (65% SF_6, 30 CCl_2F_2, 5% Ar) was in the range of 20–100 mTorr. The rf power was kept at 0.3 W/cm^2. The detailed mechanisms of polymer composition and transport to the sidewalls are not yet understood.

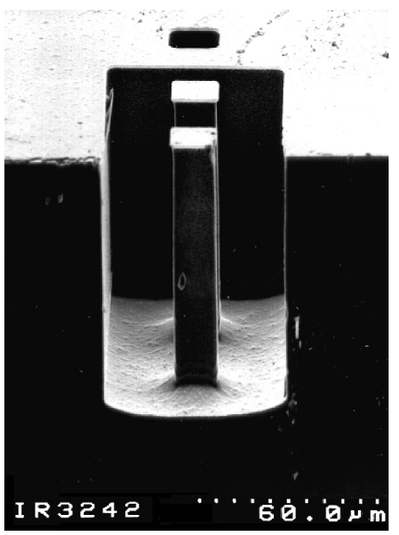


Fig. 7. Cryo-etching example: 85 µm deep structures etched into Si with SF_6/O_2 plasma chemistry using a 2.5 µm thick SiO_2 masking layer and keeping the substrate at −70 °C. Si etch rate was 1200 nm/min, selectivity 65:1

2.3
Reactive ion etching at low substrate temperatures

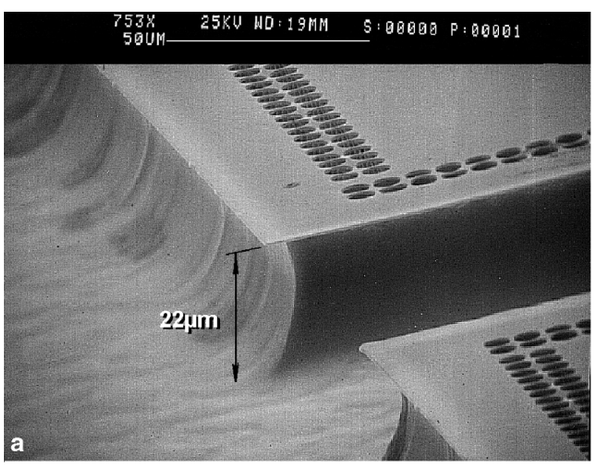
Reactive ion etching of Si at low substrate temperatures offers decisive advantages for MEMS fabrication [6, 21, 22, 27]. High aspect ratio etching is possible without formation of protective halogen-carbon polymers at the side walls. In the experiments reported here reactive ion etching was performed with an electrostatically shielded ICP source (Inductive Coupled Plasma from Oxford Plasma Technology). Liquid nitrogen was used as cooling source for the cryo-table. This source supplies a uniform cooling across a wide temperature range, realised due to controlled liquid nitrogen flow and integral electrical heater design. This construction allows a rapid change of the temperature up to +200 °C. In this processing, the substrate temperature was typically set in the range of −50 to −100 °C. With SF_6 plasma chemistry etch rates between 2 µm/min and 5 µm/min have been achieved, where etching was done with an ion energy of about 90 eV. With controlled addition of oxygen, vertical structures of more than 85 µm in depth have been achieved with excellent reproducibility. Figure 7 demonstrates smooth bottom and side walls achieved with a 3% addition of O_2 to SF_6. The proper amount of oxygen flow is dependent upon the plasma conditions, the loading, and the desired etching depth.

When keeping the substrate at low temperature, fluorine is much less penertrating into Si lattice, than in room temperature, reducing spontaneous reactions which form volatile products. Halogenated products are formed readily reacting with oxygen on the Si bottom surface. Ion induced redeposition causes a silicon-fluorine-oxide passivation layer to be condensed onto the side walls (Fig. 2c). Sufficient (10%) oxygen

has to be added to form an effective sidewall passivation. If the etching is done with the identical RIE parameters, but with the substrate kept at room temperature large undercutting is visible in Fig. 8a. When the temperature is increased to room temperature after etching, the SiF_xO_y passivation layer becomes volatile and leads to a "post-cryo-erosion" effect and is visible in a parallel etching of the vertical walls (Fig. 8b). This effect is not understood at present.

3
Lateral runout vs. etching depth

Figure 9 summarises measurements of lateral runouts for high aspect ratio microstructures as obtained in Silicon wafer substrates with reactive ion etching using different plasma chemistries. The feature size width was between 5 μm and 10 μm and the depth up to 50 μm as indicated. "Positive" runouts (top larger than bottom) were obtained for RIE with Cl_2 and Cl_2/HBr plasma chemistries, whereas "negative" runouts were obtained for SF_6/CCl_2F_2. Vertical slopes were



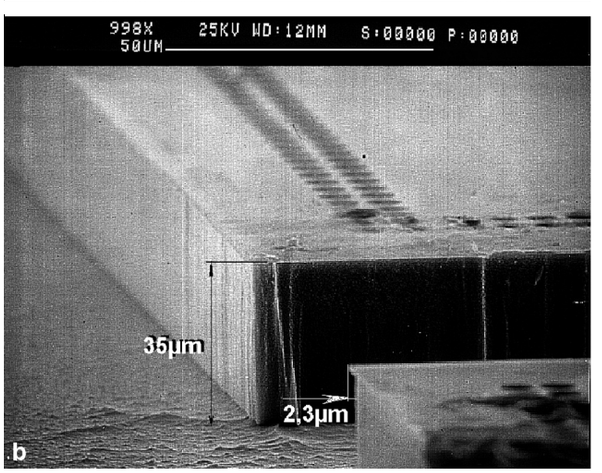


Fig. 8a, b. Temperature effect in etching of Si with SF_6/O_2 plasma chemistry, where **a** the substrate is at room temperature, **b** the substrate is kept at −80 °C during etching. In case **b** the parallel shift of the vertical Si edge of about 2.3 μm beneath the masking layer is due to "post-cryo etching", i.e. etching of Si by fluorine containing sidewall passivation when warming up the substrate to room temperature

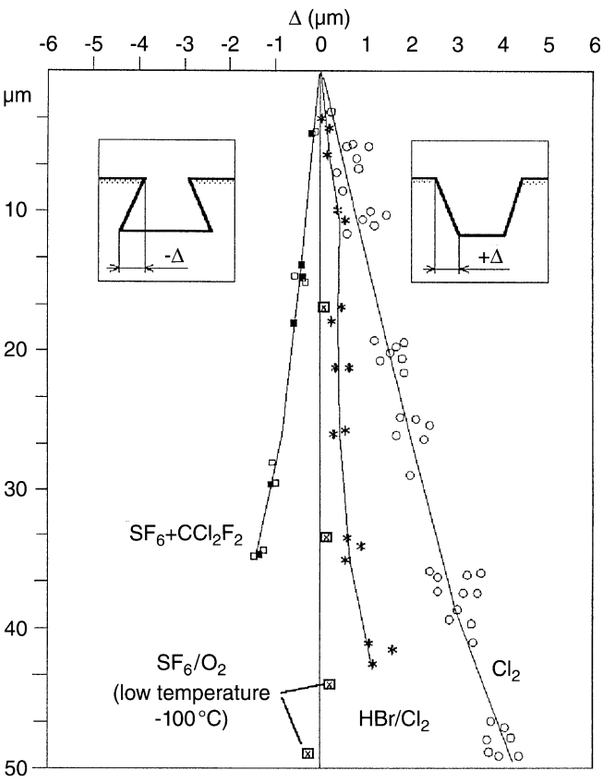


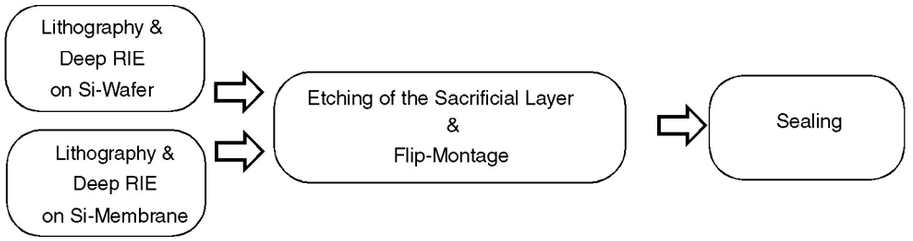
Fig. 9. Lateral runout (as defined in the figure) vs. etching depth for RIE etching of Si with the different plasma chemistries as indicated. The feature width was 5 μm and 10 μm

achieved for low substrate temperature etching with SF_6/O_2. Further optimisation of plasma chemistries as well as reactive ion etching procedures should result in runouts in the order of 0.1 μm/100 μm depth in Silicon as well as in organic materials.

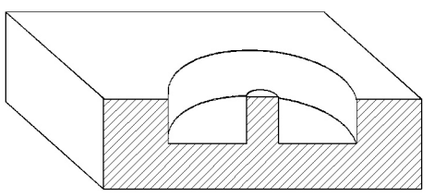
4
LIRIE technology

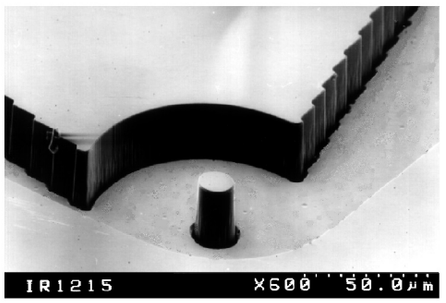
The technology presented here is based on deep dry etching as well as electro-chemically stopped wet etching and on the use of sacrificial layers, which is IC-technology compatible. The technology makes use of highly anisotropic and selective dry etching of silicon monocrystals. Figure 9 shows the sequence of the LIRIE (Lithography and Reactive Ion Etching) [6] manufacturing process. Figure 10a is a flow chart diagram depicting the LIRIE manufacturing steps which are then photographically and schematically illustrated in Fig. 10b–d. In the first step, the initially (nonmovable) axes or stators are etched into a monolithic Si-wafer (Fig. 10b). The movable parts are prepared from electro-chemically etched Si-membranes (Fig. 10c). The thickness of the membranes is defined by stopping the electro-chemical etch process at the desired p-n junctions. In this way we can vary the thickness of the membrane by varying the depth of the p-n junction.

As basis material for the membrane fabrication, we used ⟨100⟩ silicon doped with Boron. With the aid of wet, thermal oxidation at 1150 °C, the Si-wafers are covered with a 1.5 μm

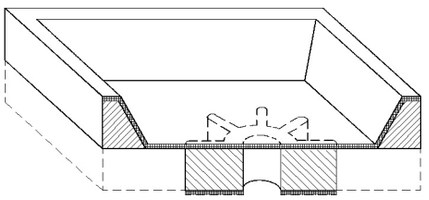


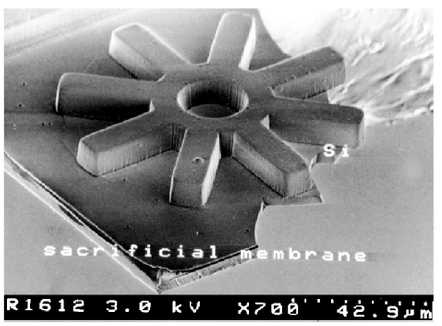
a



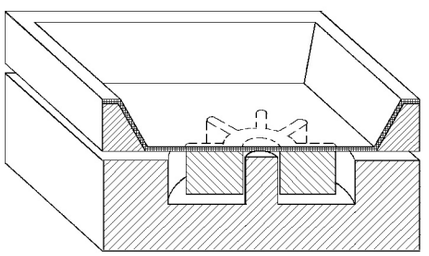


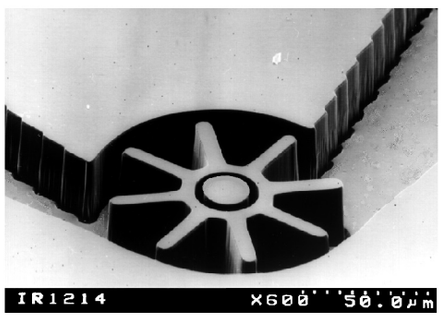
b





c





d

Fig. 10a–d. Example of a Si MEMS batch fabrication process

thick layer of SiN_xO_y. Subsequently, the windows for the diffusion of phosphorus or arsenic are etched into the SiO_2-layer. Thus we obtain a p-n-junction, which serves as electro-chemical etching stop for the membrane area. The depth of the p-n junction can be controlled in the range of 3 to 30 µm. This is sufficient to assure an etching stop for a desired membrane thickness. The above selected process parameters will result in a stress value smaller than 70 MP, and in turn this will assure the necessary mechanical elasticity for mounting the system.

The 1.5 µm thick SiN_xO_y-layer is deposited by a PECVD-process on both sides (front and back) of the membrane. Subsequently, all movable parts are defined lithographically into the photoresist film which covers the SiN_xO_y which was

deposited onto the front membrane surface in the previous step. By using RIE in $CHF_3 + Ar$ plasma, the lithographically created pattern in the photo-resistive film is transferred into SiN_xO_y film. Thereupon the mono-crystalline Si-membrane is etched down to the SiN_xO_y sacrificial layer on the back side of the membrane by an RIE process. That fixes the movable parts to this SiN_xO_y-layer. The wafer with the membrane and the movable parts is flipped onto the second wafer with the already etched axis and then positioned, centred, and aligned (Fig. 10d). The SiN_xO_y-sacrificial layer is then dissolved by a chemical wet or vapour process. Subsequent bonding with a Pyrex glass wafer seals the parts.

5 Summary

We have demonstrated the feasibility of producing micro-mechanical structures from mono-crystalline Si by using lithography and the RIE technology. The etching processes presented allows us to attain high selectivity at high anisotropy. Etching rates of 50 to 2000 nm/min have been attained. We have proven that the adjusting and mounting of micro-mechanical parts can be done by using the sacrificial SiN_xO_y-layer. A LIRIE technique is thus presented here which makes it possible to produce many micro-mechanical parts from single-crystal silicon. We suggest that when the movable and unmovable parts are loaded onto the areas (e.g., 4×4 chips) on the wafers, flipping is easier because the slopes of the sidewalls that we achieve after dry etching are only almost, but not exactly perpendicular. This makes it much easier to flip the moving parts onto the nonmoving parts and for them to be better aligned so as to better meet the tribological requirements. Also, the methods presented here can be regarded as complementary to the LIGA process, actually adding to its capabilities but at the same time being much cheaper. Other important advantages of this process are full compatibility with IC manufacturing processes and the capability of mounting microsystems containing many types of microdevices onto a single silicon microchip. In the near future, it will be possible to demonstrate the integration of IC with MEMS technology by the LIRIE method. The results of our study can contribute towards the development of MEMS engineering.

References

1. **Mohr J; Ehrfeld W; Münchmeyer D:** (1988) Requirements on resist layer in deep-etch synchrotron radiation lithography. J Vac Sci Technol B6: 2264–2267
2. **Frazier AB; Allen MG:** (1992) High aspect ratio electroplated microstructures using a photosensitive polyimide process MEMS'92, IEEE Cat. Nr. 92CH3093-2, pp. 87–92
3. **Gianchandani Y; Najafi K:** (1992) Batch fabrication and assemly of micromotor-driven mechanisms with multi-level linkages. In: Ibid, pp. 141–146
4. **Ginachandani Y; Najafi K:** (1992) Micron-sized, high aspect ratio bulk silicon micromechanical devices. In: Ibid pp. 208–213
5. **Zhang ZL; Porklab GyA; MacDonald NC:** (1992) Submicron, movable galium arsenide mechanical structures and actuators. In: Ibid, pp. 72–77
6. **Rangelow IW; Hudek P:** (1995) MEMS-Fabrication by Lithography and Reactive Ion Etching (LIRIE). Microelectr Eng 27: 471–474
7. **Furuya A; Shimokawa F; Matsuura T; Sawada R:** (1993) Micrograig fabrication of fluorinated polyimide by using magnetically controlled reactive ion etching. Proc. IEEE MEMS'93, IEEE Cat. Nr. 93CH3265-6, pp. 59–64
8. **Dahm G; Rangelow IW; Hudek P; Koops HW:** (195) Quartz etching for phase shifting masks. Microelectr Eng 27: 263–266
9. **Löchel B; Maciossek A; König M; Huber H-L:** (1994) Galvanoplated 3D structures for micro systems, Microelectr Eng 23: 455–459
10. **Gottscho RA; Jurgensen CW:** (1992) Microscopic uniformity in plasma etching. J Vac Sci Technol B10: 2133–2147
11. **Ulacia JL; McVitte JP:** (1989) A two-dimensional computer simulation for dry etching using Monte Carlo techniques. J Appl Phys 65: 1484–1491
12. **Coburn JW; Winters HF:** (1989) Conductance considerations in the reactive ion etching of high aspect ratio features. Appl Phys Lett 55: 2730–2732
13. **Ingram SG:** (1990) The influence of substrate topography on ion bombardment in plasma etching. J Appl Phys 68: 500–504
14. **Rangelow IW:** (1983) Computer simulation of line edge profiles undergoing ion bombardment. J Vac Sci and Technology, Vol. A1 410–414
15. **Wechsler K; Rangelow IW; Borkowicz Z; Durst F; Kadinski L; Schäfer M:** (1993) Experimental and numerical study of the effects of neutral transport and chemical kinetics on the plasma etching system CF_4/Si. Proceedings of the 11th International Symposium on Plasma Chemistry, Loughborough, UK, 22–27 August, 1993, pp. 909–914
16. **Rangelow IW; Kassing R:** (1988) Inhibitor films as microetching tools in pattern transfer technology. Plasma Surface Engineering 1: 473–478
17. **Rangelow IW; Thoren P; Maßeli K; Kassing R; Engelhardt M; Schwarzl S:** (1986) Secondary effects of single crystalline silicon deep-trench-etching in a chlorine-containing plasma for 3-dimensional capacitor cells. Microelectr Eng 5: 387–394
18. **Olschimke J; Rangelow IW; Tschudi T; Kassing R:** (1987) Fabrication of 15 um thick Si-hole masks for demagnifying projection systems for ion- or electron-beams. Microelectr Eng 5: 547–552
19. **Rangelow IW; Thoren P; Kassing R:** (1985) Computer simulation of pattern profiles through physical etching with shadow, trenching, and redeposition. Microelectr Eng 3: 631–638
20. **Fichelscher A; Rangelow IW; Kassing R:** (1990) Simulation of RIE-processes considering sheath dynamics. Proc. of Second International Conf. on Plasma Surface Engineering in Garmisch-Partenkirchen, FRG, Sept. 10–14, 1990, published in: Materials Science and Engineering, A 139: 412–417
21. **Rangelow IW; Löschner H:** (1995) Reactive ion etching for MEMS fabrication. J Vac Sci Technol 2394–2399
22. **Rangelow IW; Hudek P; Shi F:** (1995) Bulk micromachining of Si by lithography and reactive ion etching (LIRIE). Vacuum 46: 1361–1369
23. **Rangelow IW; Hudek P; Shi F; Kostio I; Kassing R; Löschner; Chalupka A; Hammel E; Stengl G; Vonach H:** (1995) Stencil maasken für die ionen projektions lithographie und für die maskierte ionenstrahl lithographie. VDI-Bericht von VDI Fachtagung "Maskentechnik für Mikroelektronik-/Mikrotechnik-Bausteine" 25/26 Oct. 1995, München, pp. 13–118
24. **Hudek P; Rangelow IW; Kostic I; Münzel N; Daraktchiev I:** (1996) Evaluation of chemically amplified deep UV resist for micromachining using E-beam lithography and dry etching. Microelectronic Eng 30: 309–312
25. **Rangelow IW; Shi F; Hudek P; Kostic I; Hammel E; Löschner H; Stengl G; Traher C:** (1996) Silicon stencil masks for masked ion beam lithography proximity printing. Microelectronic Eng 30: 257–260
26. **Yunkin VA; Rangelow IW; Schaefer JA; Fischer Dr; Voges E; Sloboshanin S:** (1994) Experimental study of anisotropy mechanisms during reactive ion etching of silicon in $SF_6 + C_2Cl_3F_3$ Plasma. Microelectr Eng 23: 361–364
27. **Tachi S; Tsujimoto K; Arai S; Kure T:** (1991) Low temperature dry etching. J Vac Sci Technol A9(3): 796–803