COL-216 Lab-report-2.5

2020CS10356

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1 Introduction

This lab assignment is VHDL description of processor.

There is a make file available in the submission directory which can compile all the files in one attempt.

Follow the commands to run make file in linux system (if available)

1.make (compiles all the files)

2.make plot (gtkwave of processor)

3.make clean (cleans the vcd files)

An additional component is added shifter.

I want to utilise my extra day for submitting assignment 2.2 in time.

2 Shifter

Shifter is made according to lecture notes and as per lab report flags are set correspondingly

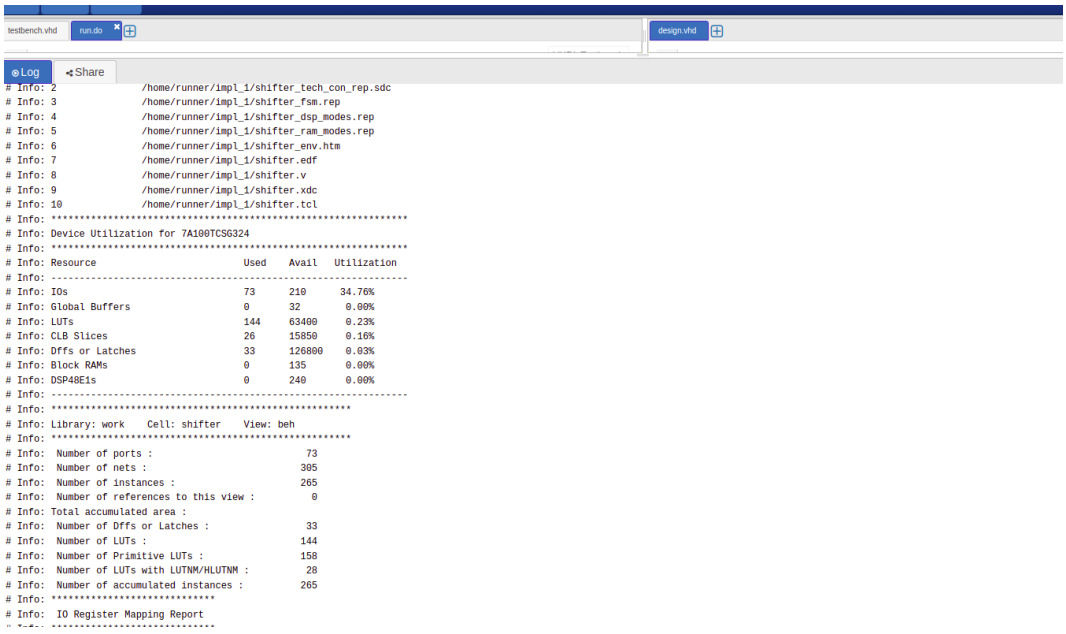

Figure 1: Device Utilisation for shifter

shifter is added with suitable glueing in the processor between regester files and ALU extra clock cycle is added for this.

3 Testcases

Test Case 1

X"E3A00028",X"E3A01023",X"E1A00A40",X"E1A01CA1",X"E08145A2", X"E1A04463",X"E5803000",X"E5814000",X"E5935000",OTHERS-X"00000000"

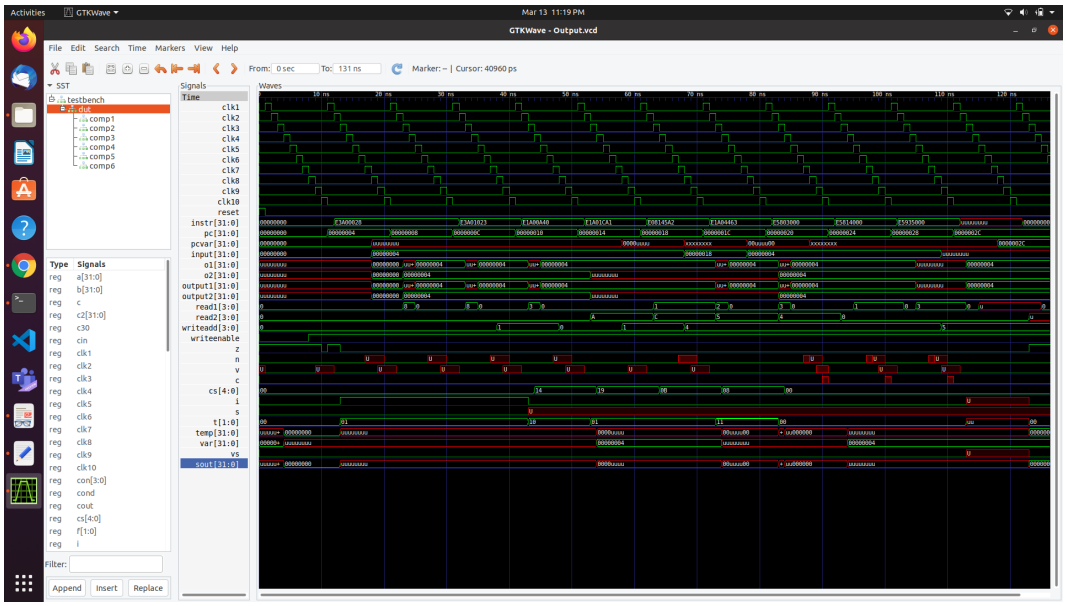

Figure 2: Example-1

Test Case-02
0=X"E3A00028",1=X"E3A01023",2=X"E1A00A40",3=X"E1A01C81",4=X"E08145A2",5=X"E04412E1"

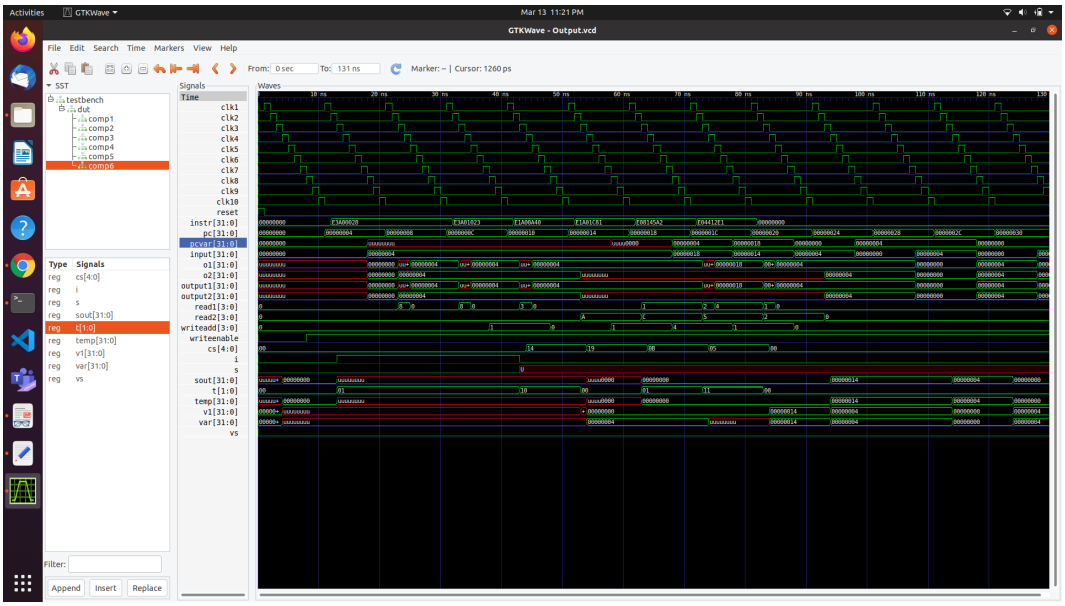

Figure 3: Example-2

Test Case-03
0=X"E3A00001",1=X"E3A01003",2=X"E1A00640",3=X"E08140A2",4=X"E0441261",5=X"E1500001",6=
8=X"E0401001",others=X"00000000"

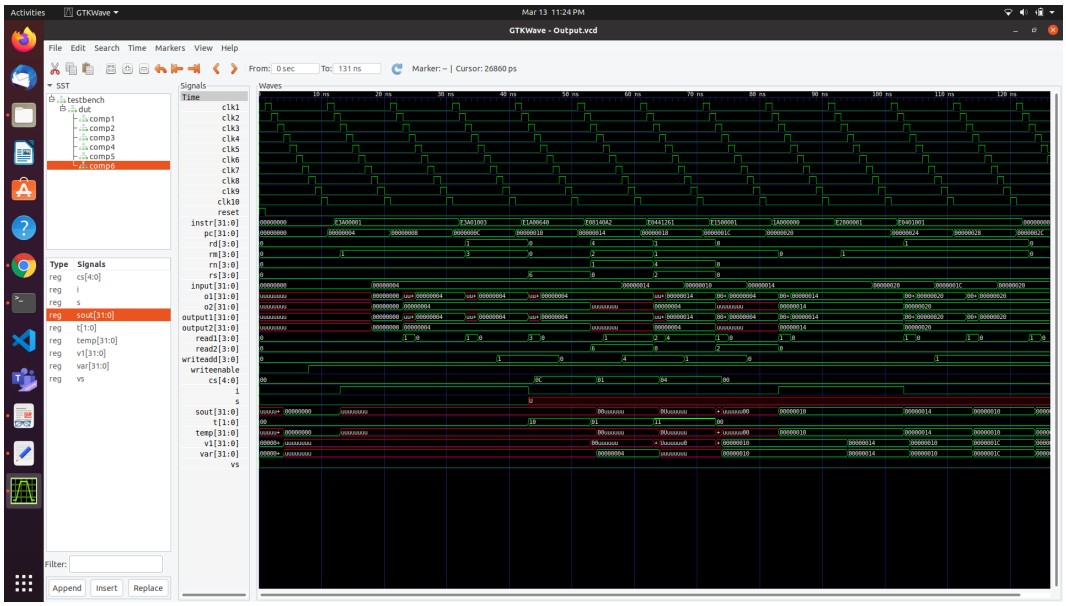

Figure 4: Example-3