COL-216 Lab-report-2.1

2020CS10356

February 2022

1 Introduction

This lab assignment is VHDL description of ALU , register file, Program memory and data memory.

There is a make file available in the submission directory which can compile all the files in one attempt

Follow the commands to run make file in linux system (if available)

1.make (compiles all the files)
2.make plotALU (gtkwave of ALU testbench)
3.make plotregfile (gtkwave of register file testbench)
4.make plotdatamem (gtkwave of datamemory testbench)
5.make clean (clears all vcd files)

vcd files Output1, Output2,Output3 will be created in the directory along with workfile

2 ALU_32 design

performs all the 16 operations based on the 4-bit operation code

and	0000
eor	0001
sub	0010
rsb	0011
add	0100
adc	0101
sbc	0110
rsc	0111
tst	1000
teq	1001
cmp	1010
orr	1011
mov	1101
bic	1110
mvn	1111

The design of ALU_32 contains sub entities and it uses components which are in submission directory
it uses :

1. MUL_2.vhdl (2-1 Multiplxer)
2. MUL_4.vhdl (4-1 Multiplexer)
3. Full_Adder.vhdl (1-bit full Adder)
4. ALU.vhdl (1-bit ALU (takes 2 input bits a and b and opcode to perfor 1 bit operation)
5. ALU_32.vhdl (32 1-bit ALU extension)
6. testbench_ALU.vhdl (testbench)

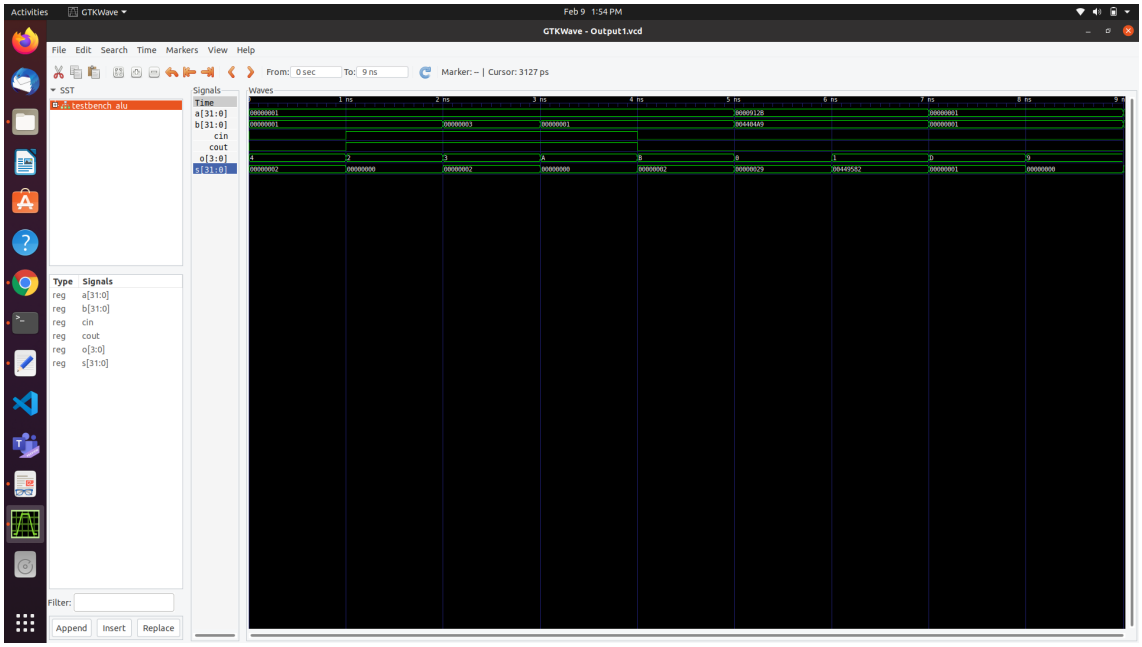

Figure 1: GTKWave of ALU_32

3 Register-File 16×32

It contains array of 16 std_logic_vector(31 downto 0).

VHDL files used by this register-files are:

1.register_file.vhdl

2.testbench_rf.vhdl

It contains two read ports two read addresses can be given and the output is always shown

But it contains only one write port which writes into specific address and is clock sensitive.

It loads the adress at clock edge after activating the command.

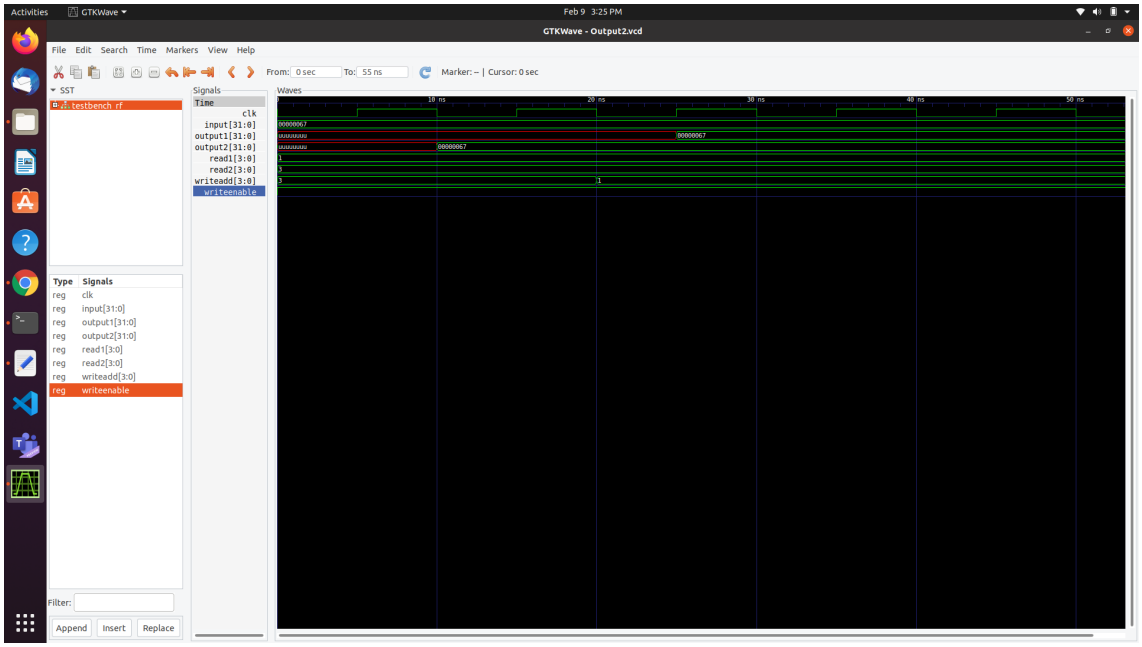

Figure 2: GTKWave of register_file

4 Data Memory 64×32

Data Memory is an array of 32 bit std_logic_vectors , the array contains 64 vectors.

It stores data memory it contains 1 read and 1 write port same as Register file its read port is
clock insensitive while its write port is clock sensitive. when write enable signal is 1 and at clock edge it writes the data to the corresponding 6 bit write address given and it outputs every time the value in read address.
VHDL files used by Data memory are :
1.data_memory.vhdl
2.testbench_dm.vhdl
It has one writeEn signal which writes complete word and it has 4 writeEn signals
writeEn1,writeEn2,writeEn3,writeEn4 which loads the corresponding byte value to write address

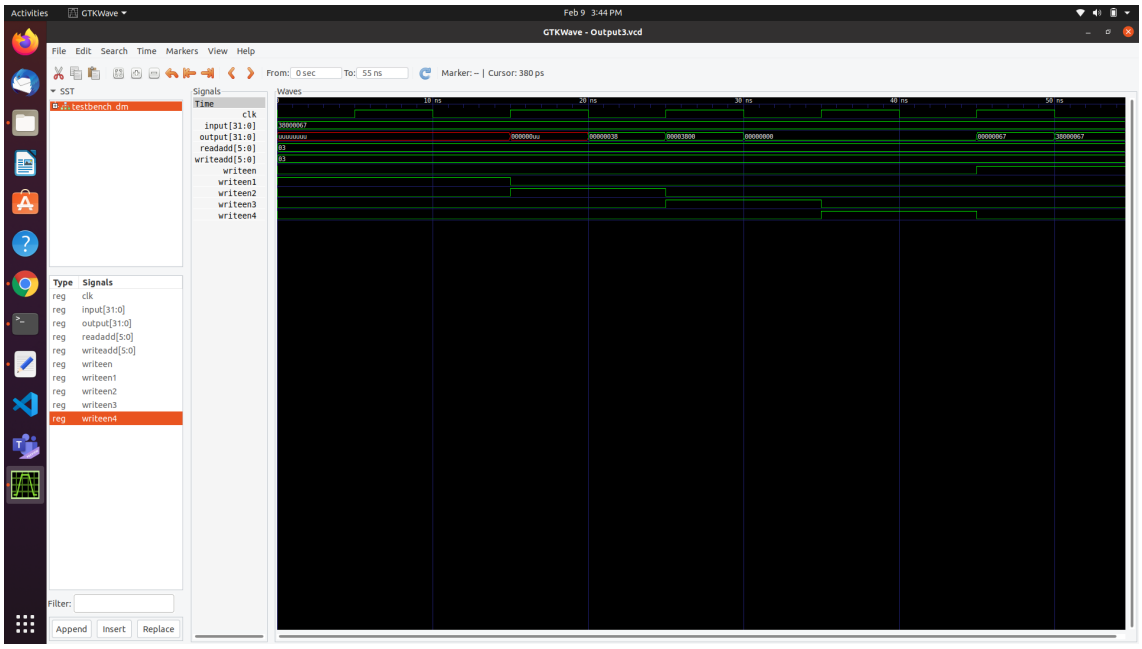

Figure 3: GTKWave of data_memory

5 Program Memory 64×32

Program Memory is an array of 32 bit std_logic_vectors ,the array contains 64 vectors.

It stores program memory and only has one read port which when given read address shows the output

of value stored in respective array element

VHDL files used by Data memory are :

1.program_memory.vhdl

2.testbench_pm.vhdl

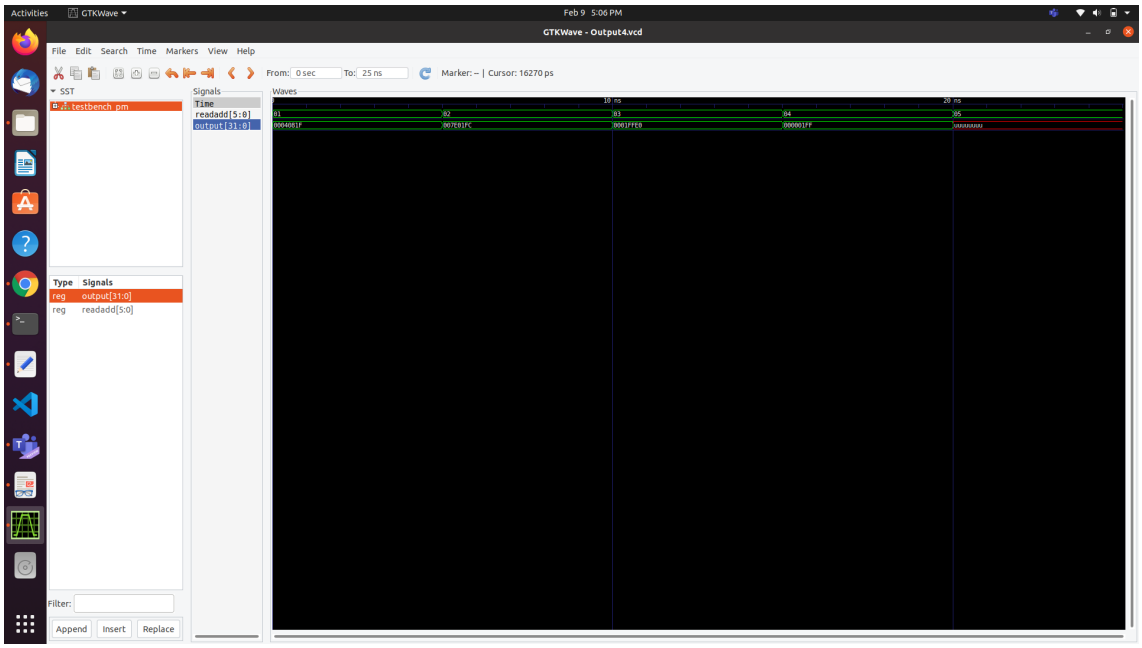

Figure 4: GTKWave of program_memory