COL-216 Lab-report-2.6

2020 CS 10356

March 2022

1 Introduction

This lab assignment is VHDL description of processor.

There is a make file available in the submission directory which can compile all the files in one attempt.

Follow the commands to run make file in linux system (if available)

1.make(compiles all the files)2.make plot(gtkwave of processor)3.make clean(cleans the vcd files)

An additional component is added shifter.

Made slight changes in shifter and Data Memory for adjustments in DT instructions

2 Shifter

Shifter is made according to lecture notes and as per lab report flags are set correspondingly

Shifter also shifts the corresponding operands in DT and DP instructions.

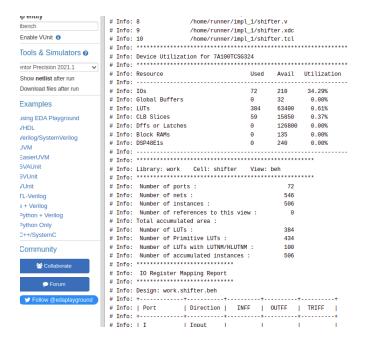


Figure 1: New Device Utilisation for shifter

shifter is added with suitable glueing in the processor between regester files and ALU extra clock cycle is added for this.

A test bench for shifter is also provuded in the directory to test shifter.

3 Data Memory

There are also slight changes made in data memory part WriteEn signal is made a 4 bit signal and removing other 3 write ports.

```
1111-will write a complete word
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1000-will write 1 byte

0100-will write 2 byte

0010-will write 3 byte

0001-will write 4 byte

1100-will write 1 half word

0011-will write 2 half word.

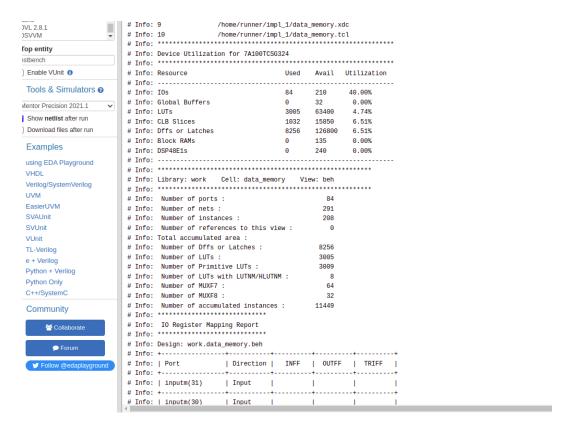


Figure 2: New Device Utilization for Data Memory

4 Testcases

Test Case 1

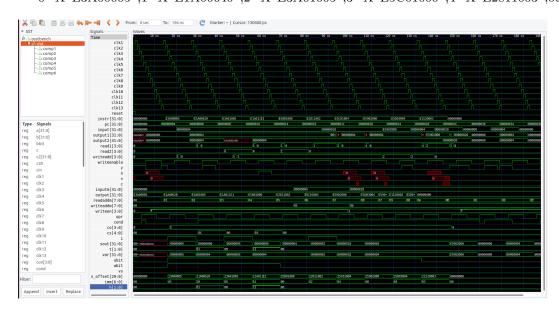


Figure 3: Example-1

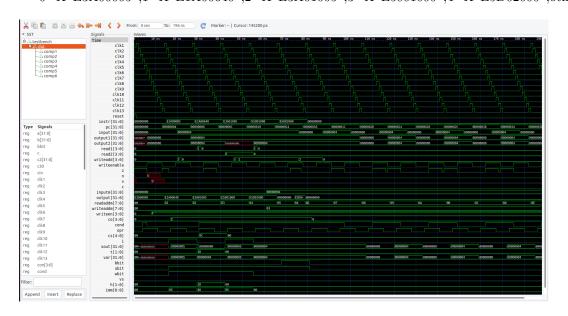


Figure 4: Example-2

 ${\it Test \ Case-02}$

.text

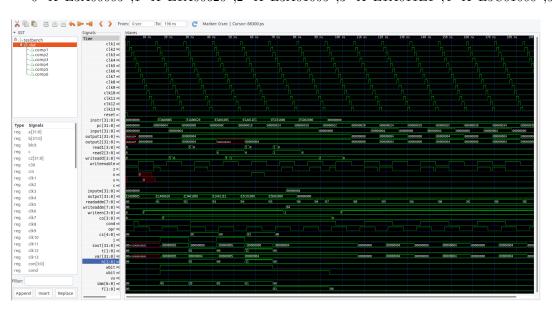


Figure 5: Example-3

 ${\it Test \ Case-03}$

```
Test Case-04 .text mov r0, 5 mov r0,r0,LSR 12 mov r1, 5 mov r1,r1,ROR 3 str r1, [r0] add r1,r1,2 strb r1,[r0,4] ldr r2, [r0] ldrb r3,[r0,4] cmp r2,r3 .end 0=X"E3A00005",1=X"E1A00620",2=X"E3A01005",3=X"E1A011E1",4=X"E5801000",5=X"E2811002",68=X"E5D03004",9=X"E1520003",others=X"000000000"
```

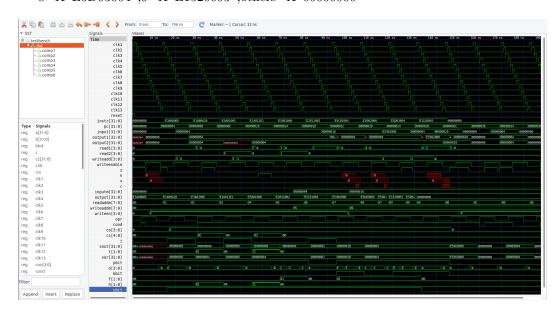


Figure 6: Example-4