COL-216 Lab-report-2.7

2020CS10356

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1 Introduction

This lab assignment is VHDL description of processor.

There is a make file available in the submission directory which can compile all the files in one attempt.

Follow the commands to run make file in linux system (if available)

1.make (compiles all the files)

2.make plot (gtkwave of processor)

3.make clean (cleans the vcd files)

There are no additional components but multiplication instructions are added.

A test bench for shifter is also provuded in the directory to test shifter.

All types of multiplication rules are added

mul

mla

umul

smul

umula

smula

are inplemented based on lecture slides and assignment description.

2 Testcases

Test Case 1

.text

mov r0, 5

mov r1,6

umull r3,r2,r0,r1

.end

0=X"E3A00005",1=X"E3A01006",2=X"E0823190",others=X"00000000"

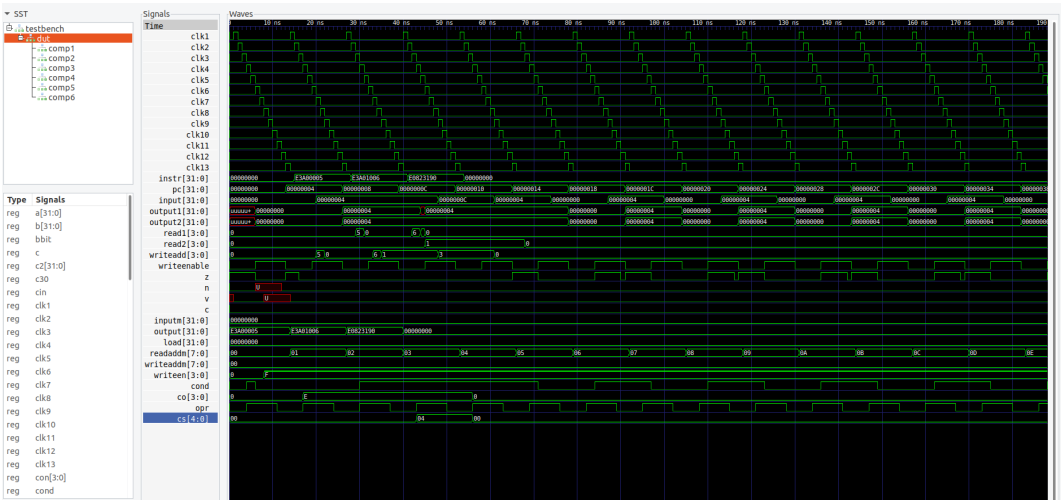

Figure 1: Example-1

Test Case-02
.text
mov r0, 5
mov r1,-6
smull r3,r2,r0,r1
.end
0=X"E3A00005",1=X"E3E01005",2=X"E0C23190",others=X"00000000"

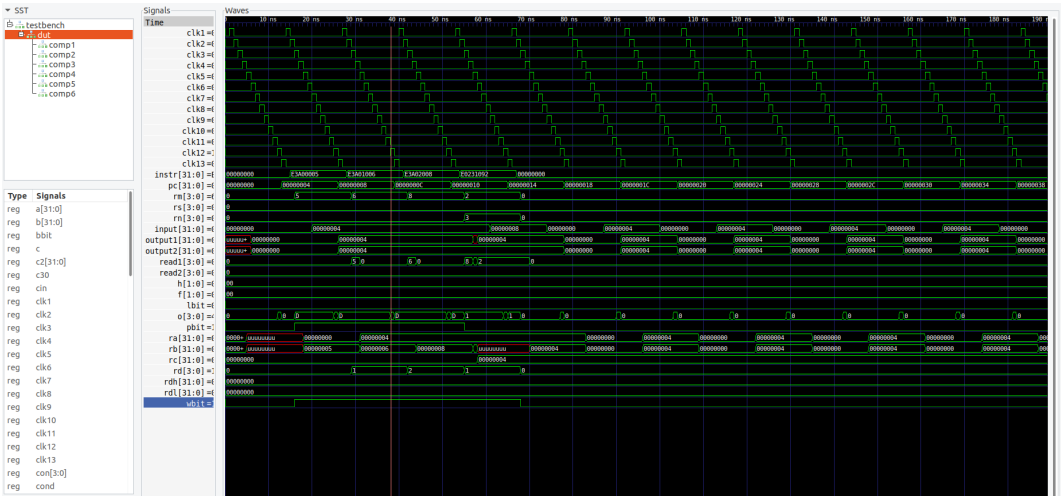

Figure 2: Example-2

Test Case-03
.text
mov r0, 5
mov r1,6
mov r2,8
mla r3,r2,r0,r1
.end
0=X"E3A00005",1=X"E3A01006",2=X"E3A02008",3=X"E0231092",others=X"00000000"

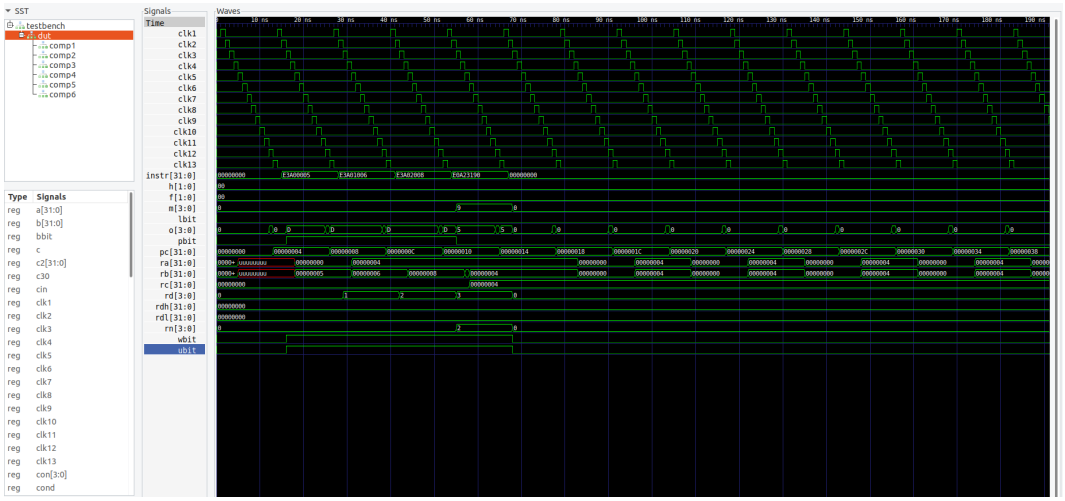

Figure 3: Example-3

Test Case-04
.text
mov r0, 5
mov r1,-6
mov r2,8
smlal r3,r2,r0,r1
.end
0=X"E3A00005",1=X"E3E01005",2=X"E3A02008",3=X"E0E23190",others=X"00000000"

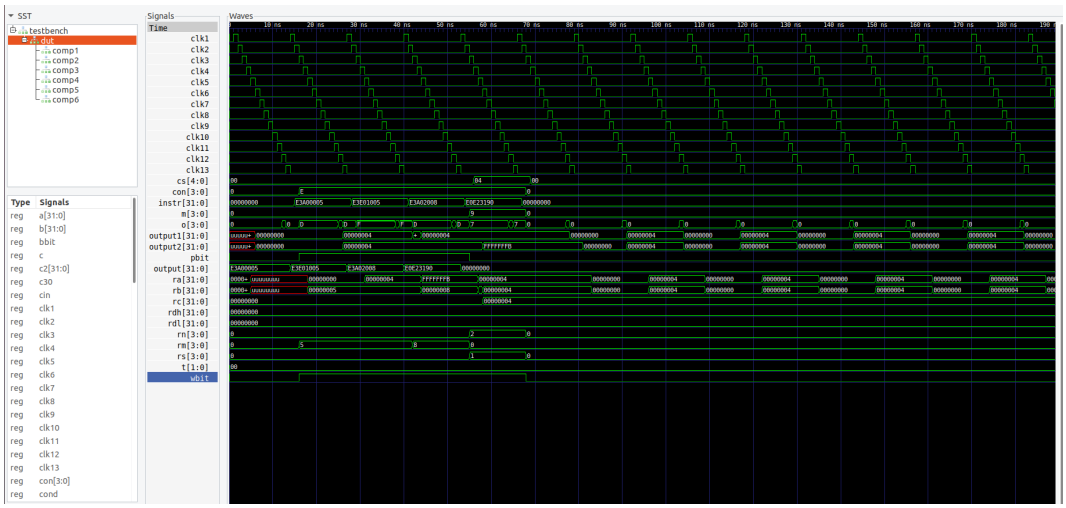

Figure 4: Example-4