COL-216 Lab-report-2.3

2020CS10356

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1 Introduction

This lab assignment is VHDL description of processor.

There is a make file available in the submission directory which can compile all the files in one attempt.

Follow the commands to run make file in linux system (if available)

1.make (compiles all the files)

2.make plot (gtkwave of processor)

NO additional components are created only registers are added and the processor is changed to multi-clock design

Changes in the design :

Made some changes to the ALU component used loops instead of all concurrent statements.

The new updated precision of ALU is :

```
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               102     210      48.57%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              244     63400     0.38%
# Info: CLB Slices                        48      15850     0.30%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ************************************************
# Info: Library: work    Cell: ALU_32    View: beh
# Info: ************************************************
# Info:  Number of ports :                          102
# Info:  Number of nets :                           594
# Info:  Number of instances :                      494
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           244
# Info:  Number of Primitive LUTs :                 262
# Info:  Number of LUTs with LUTNM/HLUTNM :          36
# Info:  Number of MUX CARRYs :                     125
# Info:  Number of accumulated instances :          589
# Info: ****************************
```

Figure 1: Device Utilisation for ALU

Made some changes to the flags component used loops instead of all concurrent statements.

```
# Info: ------------------------------------------------------------------
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               38      210      18.10%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              7       63400     0.01%
# Info: CLB Slices                        1       15850     0.01%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ****************************************************
# Info: Library: work    Cell: flags    View: beh
# Info: ****************************************************
# Info:  Number of ports :                           38
# Info:  Number of nets :                            80
# Info:  Number of instances :                       46
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of LUTs :                             7
# Info:  Number of Primitive LUTs :                   8
# Info:  Number of LUTs with LUTNM/HLUTNM :           2
# Info:  Number of accumulated instances :           46
# Info: ****************************
# Info:  IO Register Mapping Report
```

Figure 2: Device Utilisation for Flags

2 Multi Processor

The processor created in this assignment is based on multi clock cycles

at one clock cycle only one of the components are in process remaining are ideal.

after every clock period the values are stored in particular registers connected to the device.

when reset is 1 PC automatically converts to X0000000.

and signals are updated corresponding to the clock edge given in testbench.

Logic for addition and sign extension is no longer required. ALU will provide the next address that goes into PC.

Components contained in processor are :

1.) ALU_32

2.) Conditional_Checker

3.)data_memory

4.)flags

5.)register_file.

3 Sample test inputs given in Assignment -2.2

Test Case 1 :

The program memory is given in data memory along with the data as there is no requirement of two memory storing units in multi cycle design the PC and many corresponding additions are done in ALU wothout the extra requirement of Adderes. as there is only one component usage in one cycle.

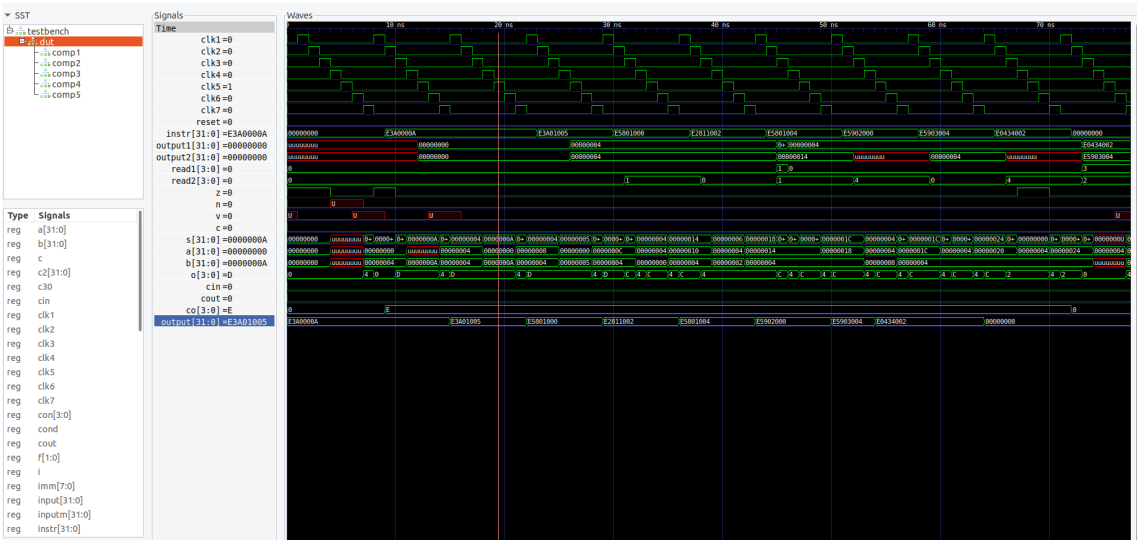

Figure 3: Example-1

This corresponding example has no branch instructions.
All the instructions are shown in Instr after clock cycles (7 clock cycles).
instructions one after the other are read and executed simulataneously.
The following example is a program which contains branch instructions and going back of instructions is clearly seen in the following images of the examples.

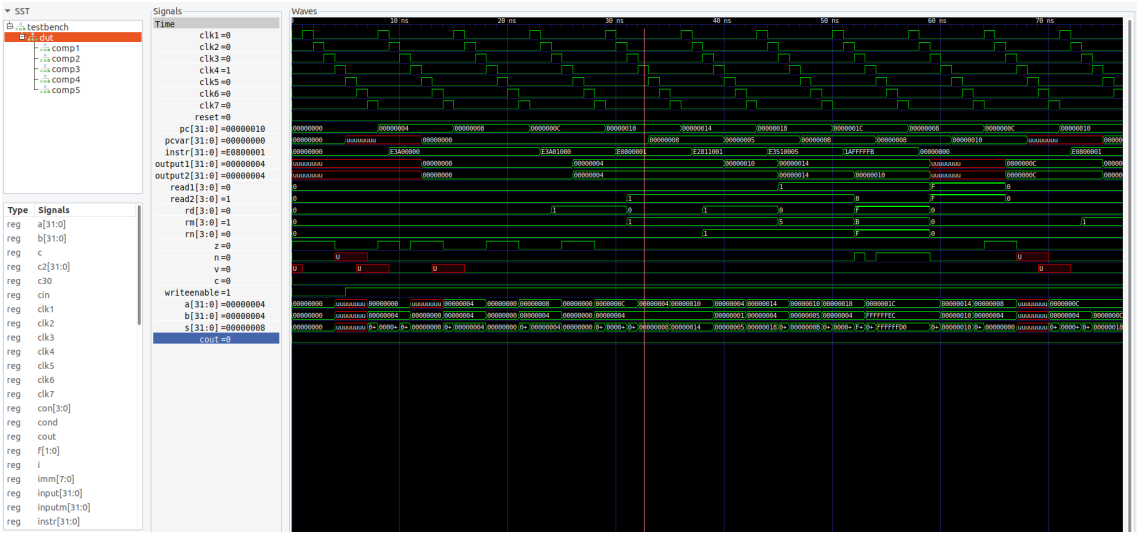

Figure 4: Example-2

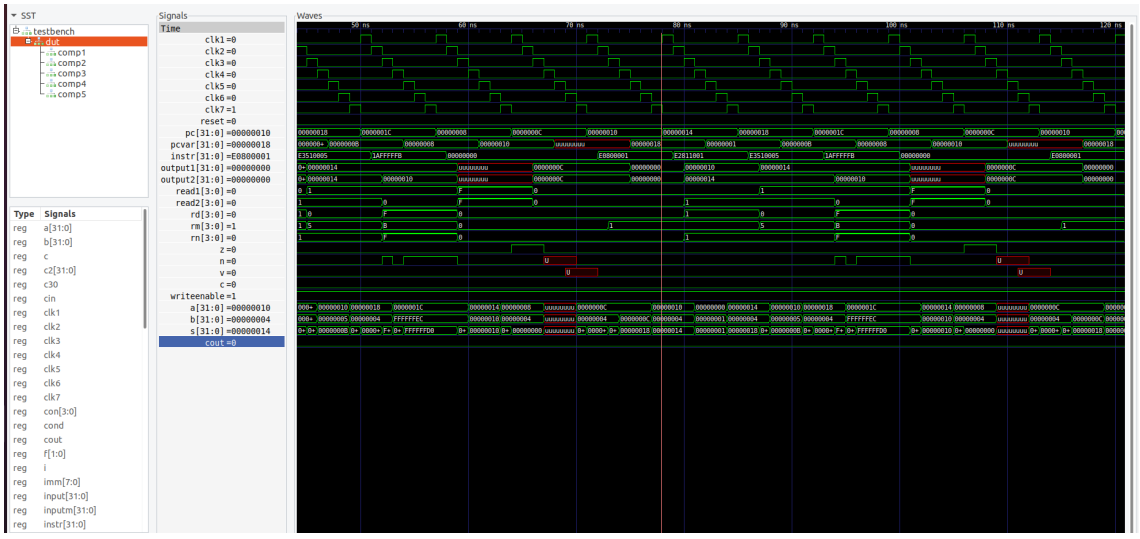

Figure 5: Example-2

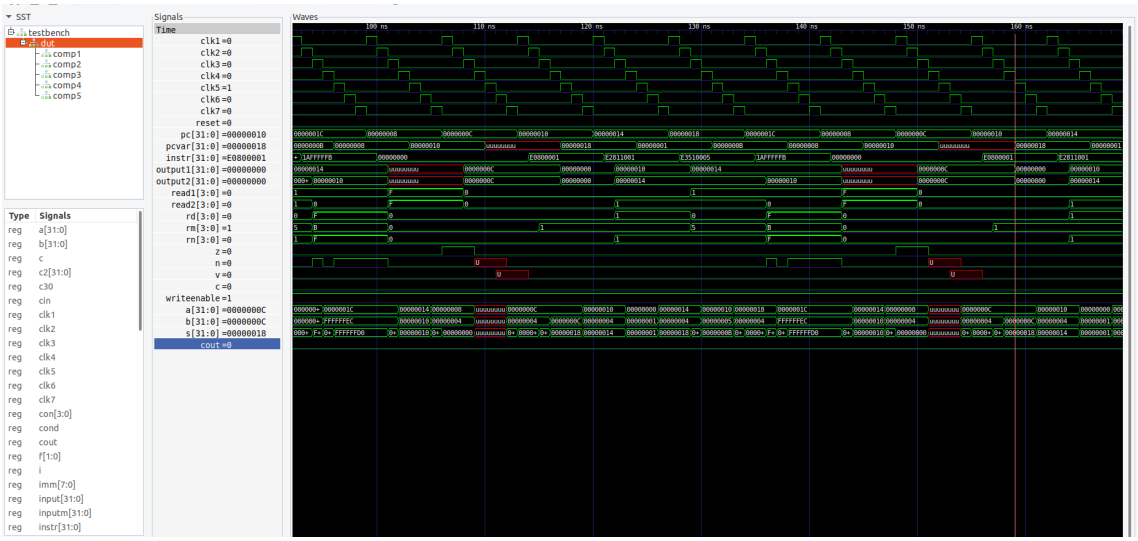

Figure 6: Example-2