COL-216 Lab-report-2.2

2020CS10356

February 2022

1 Introduction

This lab assignment is VHDL description of processor.

There is a make file available in the submission directory which can compile all the files in one attempt.

textbfFollow the commands to run make file in linux system (if available)

1.make (compiles all the files)

2.make plot (gtkwave of processor)

Coponents Additional to 2.1 Assignment Created are :

1. Flags

2. program_counter

3. condition_checker

2 Flags

Flags are created by inputs S and C31 and C30 from the ALU port and it sets the Z,V,N,C Flags.

outputs all the flags and every flag is updated at clock edge.

The value of the flags is set according to the lecture slides by S,C30,C31 from ALU.

3 program_counter

program_counter entity takes PC and Instruction and corresponding Flags as input

and if the instruction is branch instruction PCout(updated PC) is set with corresponding Offset available in branch instruction.

if the instruction is not a branch instruction PCout(updated PC) is set to PC+4 at clock edge

and the output is available as PCnew.

```
# Info: ------------------------------------------------------------
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               39      210      18.57%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              7       63400     0.01%
# Info: CLB Slices                        1       15850     0.01%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ************************************************
# Info: Library: work    Cell: flags    View: beh
# Info: ************************************************
# Info:  Number of ports :                          39
# Info:  Number of nets :                           86
# Info:  Number of instances :                      51
# Info:  Number of references to this view :         0
# Info: Total accumulated area :
# Info:  Number of LUTs :                            7
# Info:  Number of Primitive LUTs :                  8
# Info:  Number of LUTs with LUTNM/HLUTNM :          2
# Info:  Number of accumulated instances :          59
# Info: ****************************
```

Figure 1: Device Utilisation for Flags

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               98      210      46.67%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              61      63400     0.10%
# Info: CLB Slices                        16      15850     0.10%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: program_counter    View: beh
# Info: ************************************************************
# Info:  Number of ports :                          98
# Info:  Number of nets :                          280
# Info:  Number of instances :                     189
# Info:  Number of references to this view :         0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           61
# Info:  Number of Primitive LUTs :                 61
# Info:  Number of MUX CARRYs :                     57
# Info:  Number of accumulated instances :         274
# Info: ******************************
```

Figure 2: Device Utilisation for program_counter

4 Condition_Checker

Condition_Checker takes the flags and current Instruction as inputs and it gives the Cond as output at every clock edge it updates the Cond. the value of Cond is set according to the lecture slides.

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               38      210      18.10%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              5       63400     0.01%
# Info: CLB Slices                        1       15850     0.01%
# Info: Dffs or Latches                   8       126800    0.01%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: Condition_Checker    View: beh
# Info: ************************************************************
# Info:  Number of ports :                          38
# Info:  Number of nets :                           38
# Info:  Number of instances :                      29
# Info:  Number of references to this view :         0
# Info: Total accumulated area :
# Info:  Number of Dffs or Latches :                 8
# Info:  Number of LUTs :                            5
# Info:  Number of Primitive LUTs :                  7
# Info:  Number of LUTs with LUTNM/HLUTNM :          4
# Info:  Number of accumulated instances :          31
```

Figure 3: Device Utilisation for Condition_Checker

5 Processor

processor designed in this assignment is a single cycle design same as in lecture slides.

The processor contains ALU , register-file , data-memory , flags , program-counter,condition-checker as components in it.

The design includes the increment of PC change in Instructions ,signals, Flags etc.. by the clock time.

At every clock edge there is change in PC and correspondingly updating all the signals.

Processor contains two input ports clock and reset when reset is 1

PC automatically converts to X0000000.

and signals are updated corresponding to the clock edge given in testbench.

6 Sample Testing Inputs which are in Assignment

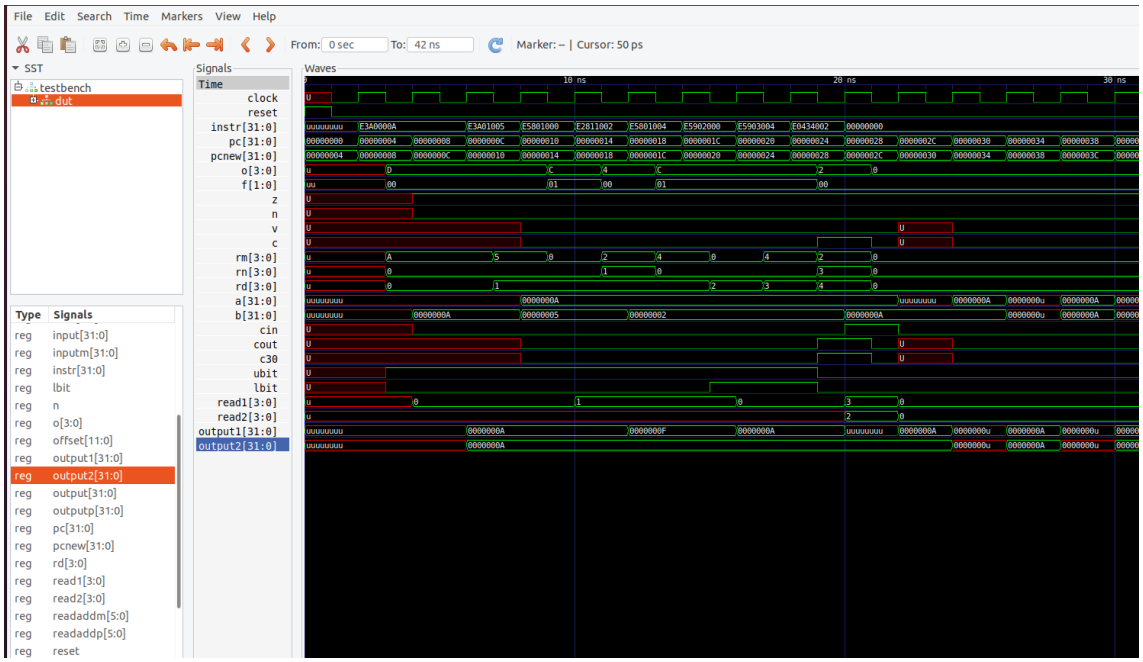

Figure 4: Example -1

Few major inputs are shown in respective components.
we can see the PC is incrementing by PC the following example has no branch instructions.
The load,str instructions and DP instructions are shown.
here,the Instr signal and the corresponding signals change by the clock edge
Rd,Rm,Rn values at each and every clock edge is shown.
The Flags Z,N,V,C are updated at respective clock cycles and clock edges.
The following is the example of branch instruction as we can see the branch loops again and again

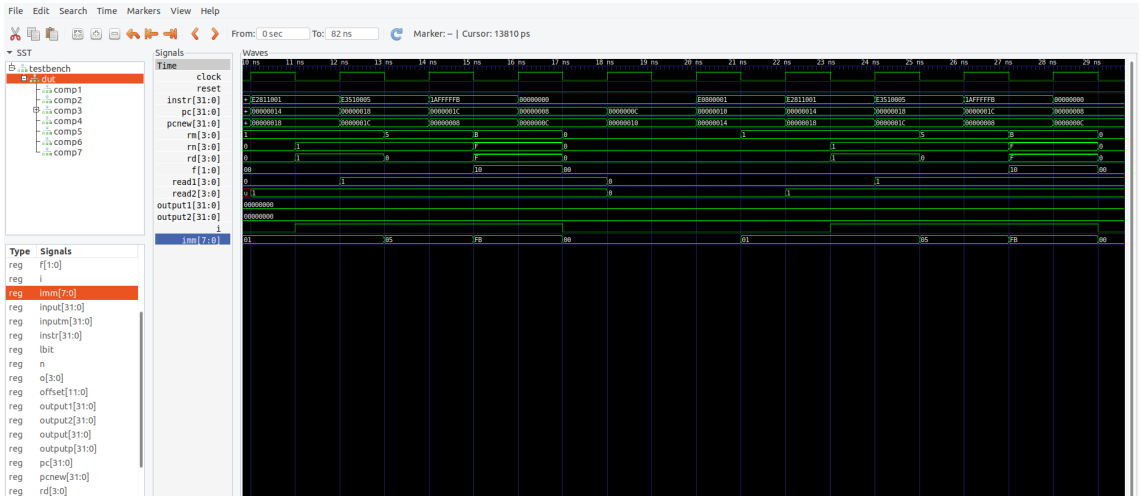

Figure 5: Example -2

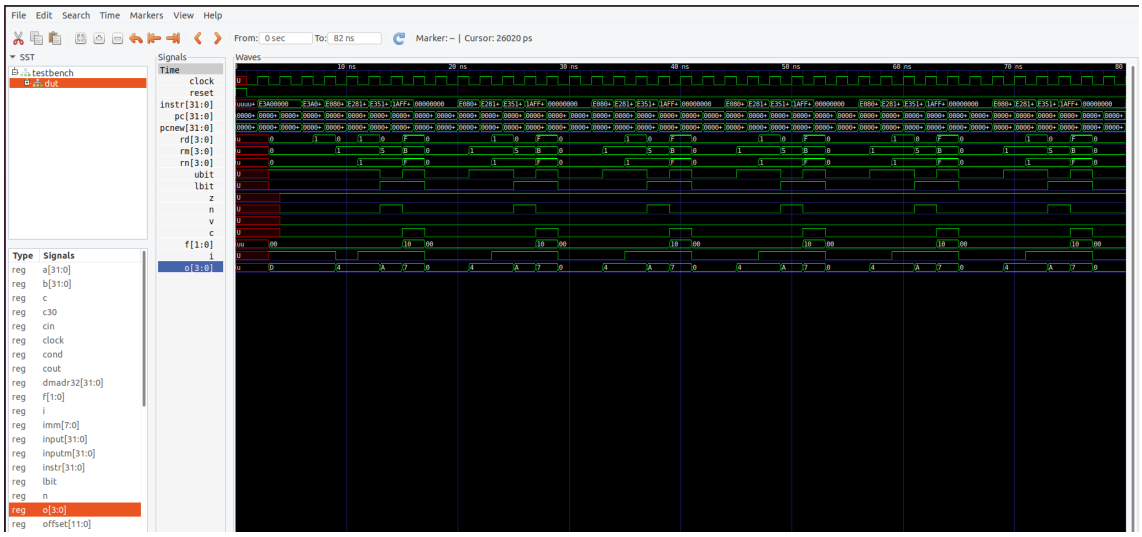

Figure 6: Example -2