Experiment - 5: Implementation of a 7-Segment Display to Show the Registration Number by Using Quartus Prime

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REG NO: 22BEC1205

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Aim:
Write a Verilog RTL code for designing and implementing a 7-segment Display. Also, perform the simulation of the Full Adder using Quartus Prime and Model Sim. Finally, implement the circuit on the FPGA kit, "5CSXFC6D6F31C6N"

Software Required: Quartus Prime**,** ModelSim

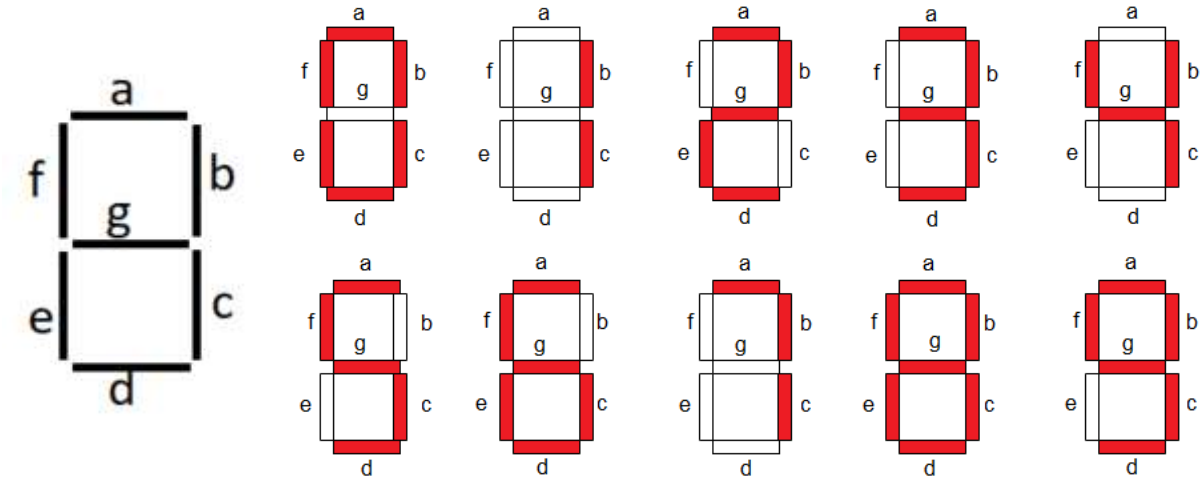
Haraware Required: Altera Cyclone V 5CSXFC6D6F31C6N

Procedure:

- Open Quartus Prime 21.1.
- Go to File -> New Project wizard -> select Source folder & type file name -> Next.
- Select Empty Project in Project type -> Next.
- Click on Next in Add Files dialog box.
- Select "Cyclone V SX Extended Features" in Device Family.
- In available devices, select the one ending with "31C6" -> Next.
- Select the tool name as "ModelSim" and Format as "VerilogHDL" in simulation.
- Click on Finish. The project is now created.
- In the Task window, select RTL simulation and run, this would open the ModelSim window.
- Simulate the full adder as you would do using ModelSim by forcing the input values.
- In Compilation -> select compile design.
- Go to Assignments tab -> Pin planner -> Give the location for each i/o pin.
- Go to Hardware Setup -> Select USB.
- Change the file to Fulladder.v in the program/configure option and select Start.

Theory

Seven segment displays are the output display device that provides a way to display information in the form of images or text or decimal numbers which is an alternative to the more complex dot matrix displays. It is widely used in digital clocks, basic calculators, electronic meters, and other electronic devices that display numerical information. It consists of seven segments of light-emitting diodes (LEDs) which are assembled like numerical 8.



Truth Table for an active high 7 segment display
(Note: in Cyclone V 5CSXFC6D6F31C6N the display logic is active low):

Inputs				Segments							
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	For display 0
0	0	0	1	0	1	1	0	0	0	0	For display 1
0	0	1	0	1	1	0	1	1	0	1	For display 2
0	0	1	1	1	1	1	1	0	0	1	For display 3
0	1	0	0	0	1	1	0	0	1	1	For display 4
0	1	0	1	1	0	1	1	0	1	1	For display 5
0	1	1	0	1	0	1	1	1	1	1	For display 6
0	1	1	1	1	1	1	0	0	0	0	For display 7
1	0	0	0	1	1	1	1	1	1	1	For display 8
1	0	0	1	1	1	1	1	0	1	1	For display 9
1	0	1	0	1	1	1	0	1	1	1	For display A
1	0	1	1	0	0	1	1	1	1	1	For display b
1	1	0	0	1	0	0	1	1	1	0	For display C
1	1	0	1	0	1	1	1	1	0	1	For display d
1	1	1	0	1	0	0	1	1	1	1	For display E
1	1	1	1	1	0	0	0	1	1	1	For display F

Source code and Outputs:

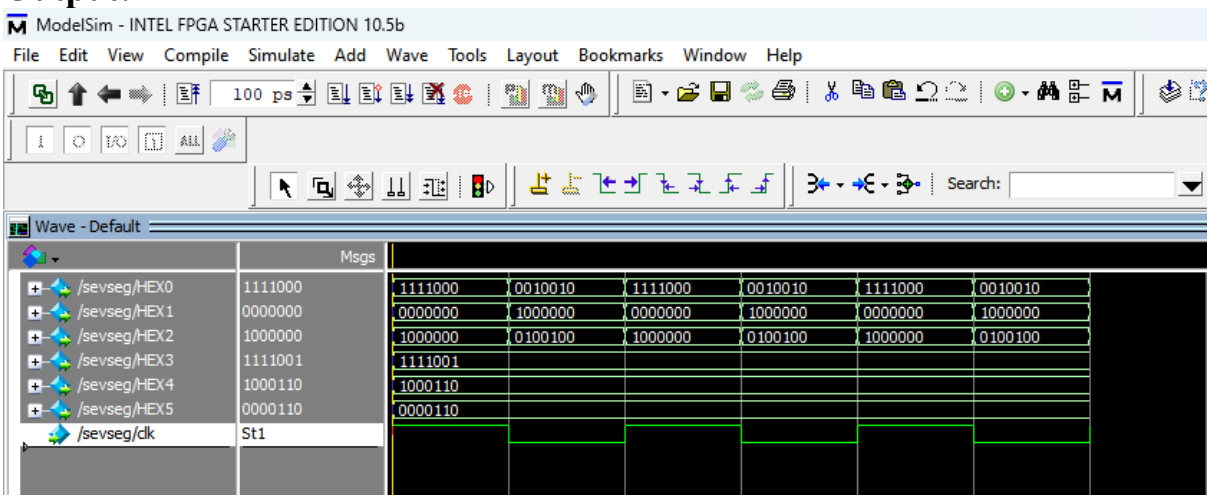
```
module sevseg(
   input wire clk,
   output reg [6:0] HEX0,
   output reg [6:0] HEX1,
   output reg [6:0] HEX2,
   output reg [6:0] HEX3,
output reg [6:0] HEX4,
output reg [6:0] HEX5
);
integer i=0,j=0;
   // 7-segment encoding (Common Anode: Active LOW)
   function [6:0] seg_decode;
      input [3:0] digit;
      case (digit)
         4'h0: seg_decode = 7'b1000000;
         4'h1: seg_decode = 7'b1111001;
         4'h2: seg_decode = 7'b0100100;
         4'h3: seg_decode = 7'b0110000;
         4'h4: seg_decode = 7'b0011001;
         4'h5: seg_decode = 7'b0010010;
         4'h6: seg_decode = 7'b0000010;
         4'h7: seg_decode = 7'b1111000;
         4'h8: seg_decode = 7'b0000000;
         4'h9: seg_decode = 7'b0010000;
4'hE: seg_decode = 7'b0000110;
4'hC: seg_decode = 7'b1000110;
          default: seg_decode = 7'b1111111;
      endcase
   endfunction

always@(posedge clk) begin
if(i==0)begin
HEX0 = seg_decode(4'h7);
HEX1 = seg_decode(4'h8);
HEX2 = seg_decode(4'h0);
HEX3 = seg_decode(4'h1);
HEX4 = seg_decode(4'hC);
HEX5 = seg_decode(4'hE);
end
if(i==1)begin
HEX0 = seg_decode(4'h5);
HEX1 = seg_decode(4'h0);
HEX2 = seg_decode(4'h2);
HEX3 = seg_decode(4'h1);
HEX4 = seg_decode(4'hC);
HEX5 = seg_decode(4'hE);
end
j=j+1;
```

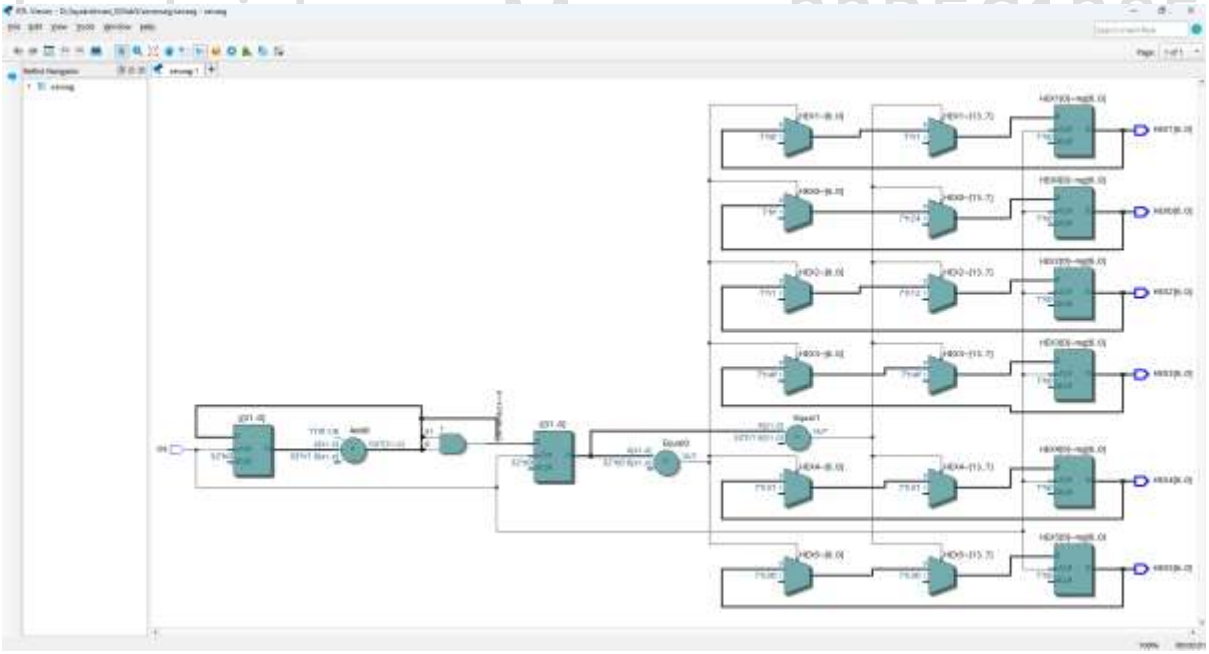
```
i=j%2;

end
endmodule
```

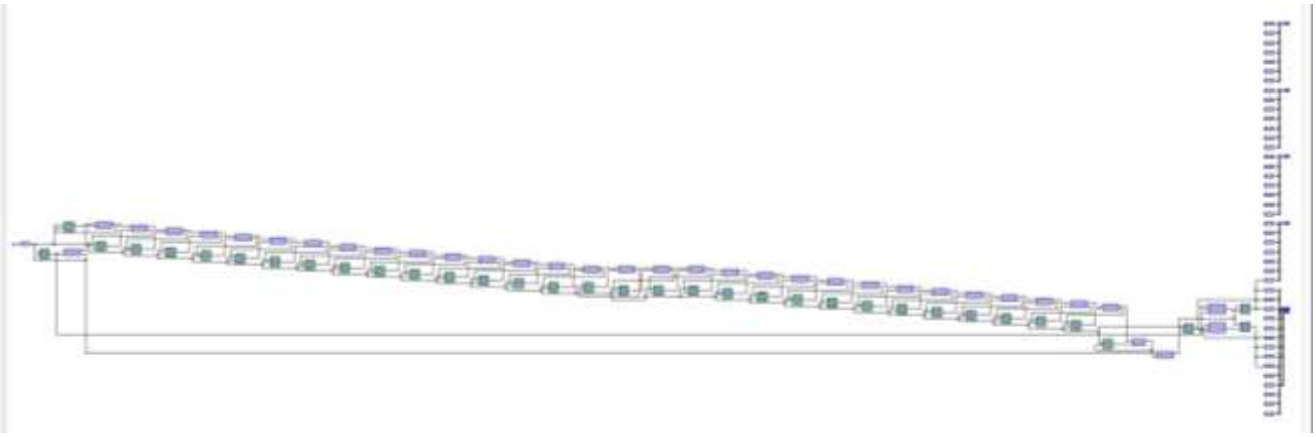
Output:



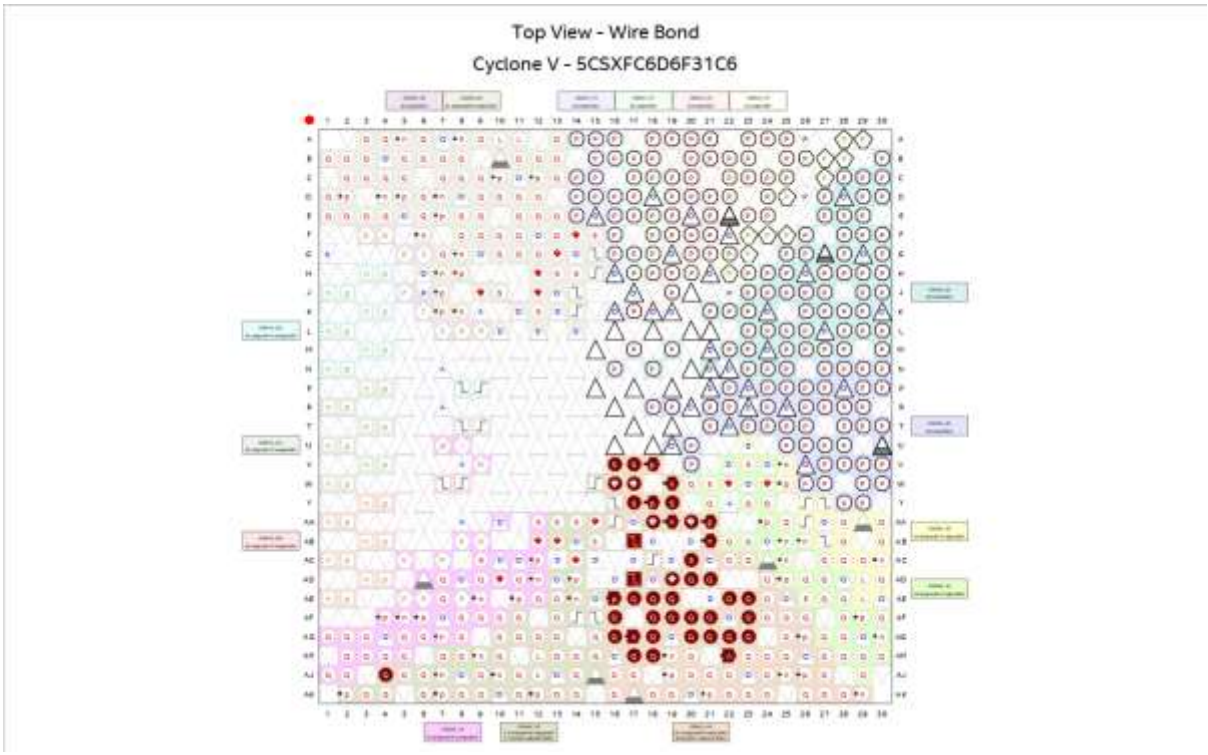
RTL Viewer:



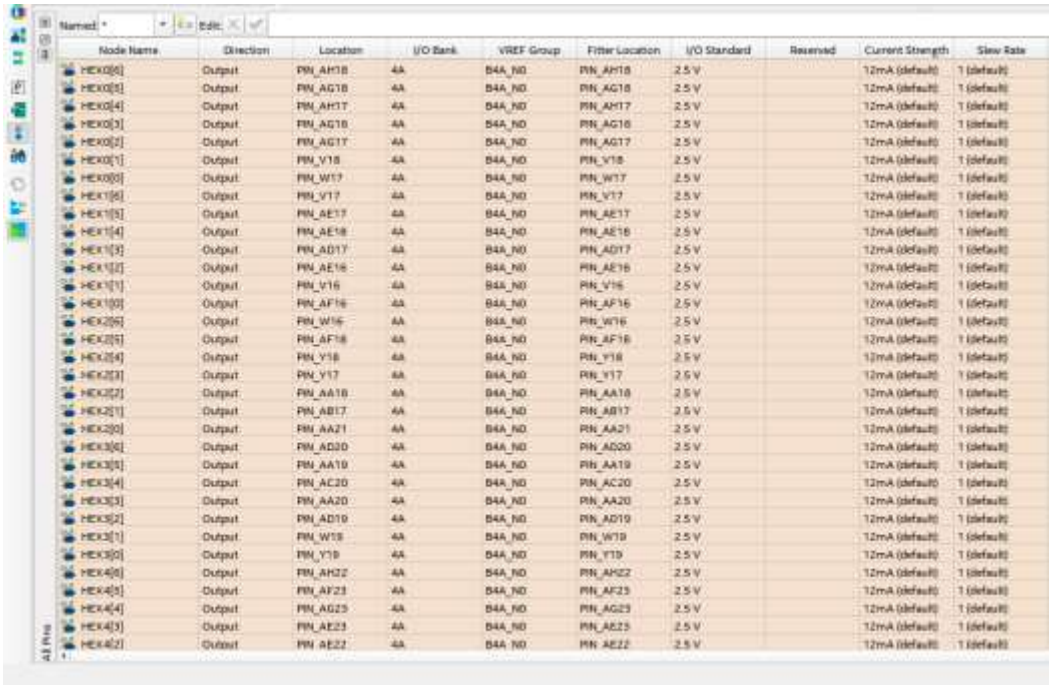
Technology Map Viewer:



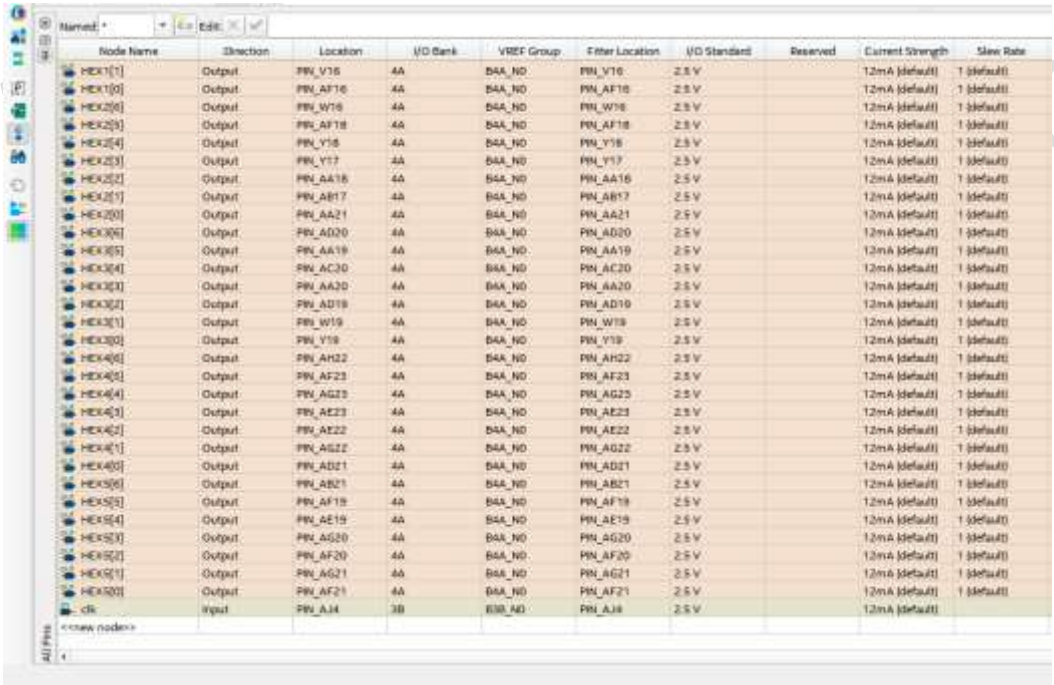
Pin Planning:



Choosing on board 7 Segment Displays:

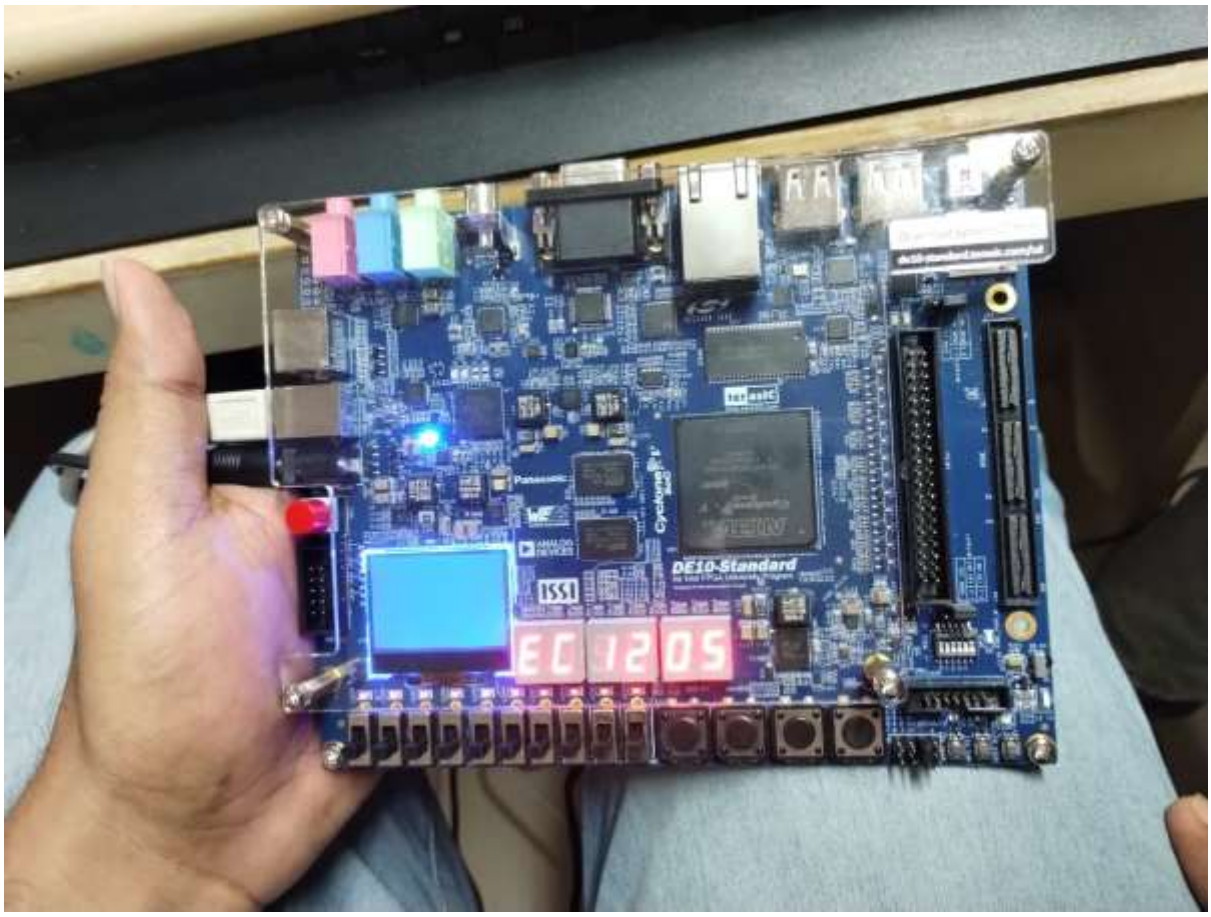


Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
HEX0[6]	Output	PIN_AH18	4A	B4A_N0	PIN_AH18	2.5 V		12mA (default)	1 (default)
HEX0[5]	Output	PIN_AG18	4A	B4A_N0	PIN_AG18	2.5 V		12mA (default)	1 (default)
HEX0[4]	Output	PIN_AH17	4A	B4A_N0	PIN_AH17	2.5 V		12mA (default)	1 (default)
HEX0[3]	Output	PIN_AG18	4A	B4A_N0	PIN_AG18	2.5 V		12mA (default)	1 (default)
HEX0[2]	Output	PIN_AG17	4A	B4A_N0	PIN_AG17	2.5 V		12mA (default)	1 (default)
HEX0[1]	Output	PIN_V18	4A	B4A_N0	PIN_V18	2.5 V		12mA (default)	1 (default)
HEX0[0]	Output	PIN_W17	4A	B4A_N0	PIN_W17	2.5 V		12mA (default)	1 (default)
HEX1[6]	Output	PIN_V17	4A	B4A_N0	PIN_V17	2.5 V		12mA (default)	1 (default)
HEX1[5]	Output	PIN_AE17	4A	B4A_N0	PIN_AE17	2.5 V		12mA (default)	1 (default)
HEX1[4]	Output	PIN_AE18	4A	B4A_N0	PIN_AE18	2.5 V		12mA (default)	1 (default)
HEX1[3]	Output	PIN_AD17	4A	B4A_N0	PIN_AD17	2.5 V		12mA (default)	1 (default)
HEX1[2]	Output	PIN_AE16	4A	B4A_N0	PIN_AE16	2.5 V		12mA (default)	1 (default)
HEX1[1]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)
HEX1[0]	Output	PIN_AF16	4A	B4A_N0	PIN_AF16	2.5 V		12mA (default)	1 (default)
HEX2[6]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)
HEX2[5]	Output	PIN_AF18	4A	B4A_N0	PIN_AF18	2.5 V		12mA (default)	1 (default)
HEX2[4]	Output	PIN_Y18	4A	B4A_N0	PIN_Y18	2.5 V		12mA (default)	1 (default)
HEX2[3]	Output	PIN_Y17	4A	B4A_N0	PIN_Y17	2.5 V		12mA (default)	1 (default)
HEX2[2]	Output	PIN_AA18	4A	B4A_N0	PIN_AA18	2.5 V		12mA (default)	1 (default)
HEX2[1]	Output	PIN_AB17	4A	B4A_N0	PIN_AB17	2.5 V		12mA (default)	1 (default)
HEX2[0]	Output	PIN_AA21	4A	B4A_N0	PIN_AA21	2.5 V		12mA (default)	1 (default)
HEX3[6]	Output	PIN_AD20	4A	B4A_N0	PIN_AD20	2.5 V		12mA (default)	1 (default)
HEX3[5]	Output	PIN_AA19	4A	B4A_N0	PIN_AA19	2.5 V		12mA (default)	1 (default)
HEX3[4]	Output	PIN_AC20	4A	B4A_N0	PIN_AC20	2.5 V		12mA (default)	1 (default)
HEX3[3]	Output	PIN_AA20	4A	B4A_N0	PIN_AA20	2.5 V		12mA (default)	1 (default)
HEX3[2]	Output	PIN_AD19	4A	B4A_N0	PIN_AD19	2.5 V		12mA (default)	1 (default)
HEX3[1]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA (default)	1 (default)
HEX3[0]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA (default)	1 (default)
HEX4[6]	Output	PIN_AH22	4A	B4A_N0	PIN_AH22	2.5 V		12mA (default)	1 (default)
HEX4[5]	Output	PIN_AF23	4A	B4A_N0	PIN_AF23	2.5 V		12mA (default)	1 (default)
HEX4[4]	Output	PIN_AG23	4A	B4A_N0	PIN_AG23	2.5 V		12mA (default)	1 (default)
HEX4[3]	Output	PIN_AE23	4A	B4A_N0	PIN_AE23	2.5 V		12mA (default)	1 (default)
HEX4[2]	Output	PIN_AE22	4A	B4A_N0	PIN_AE22	2.5 V		12mA (default)	1 (default)



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
HEX1[1]	Output	PIN_V16	4A	B4A_N0	PIN_V16	2.5 V		12mA (default)	1 (default)
HEX1[0]	Output	PIN_AF16	4A	B4A_N0	PIN_AF16	2.5 V		12mA (default)	1 (default)
HEX2[6]	Output	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V		12mA (default)	1 (default)
HEX2[5]	Output	PIN_AF18	4A	B4A_N0	PIN_AF18	2.5 V		12mA (default)	1 (default)
HEX2[4]	Output	PIN_Y18	4A	B4A_N0	PIN_Y18	2.5 V		12mA (default)	1 (default)
HEX2[3]	Output	PIN_Y17	4A	B4A_N0	PIN_Y17	2.5 V		12mA (default)	1 (default)
HEX2[2]	Output	PIN_AA18	4A	B4A_N0	PIN_AA18	2.5 V		12mA (default)	1 (default)
HEX2[1]	Output	PIN_AB17	4A	B4A_N0	PIN_AB17	2.5 V		12mA (default)	1 (default)
HEX2[0]	Output	PIN_AA21	4A	B4A_N0	PIN_AA21	2.5 V		12mA (default)	1 (default)
HEX3[6]	Output	PIN_AD20	4A	B4A_N0	PIN_AD20	2.5 V		12mA (default)	1 (default)
HEX3[5]	Output	PIN_AA19	4A	B4A_N0	PIN_AA19	2.5 V		12mA (default)	1 (default)
HEX3[4]	Output	PIN_AC20	4A	B4A_N0	PIN_AC20	2.5 V		12mA (default)	1 (default)
HEX3[3]	Output	PIN_AA20	4A	B4A_N0	PIN_AA20	2.5 V		12mA (default)	1 (default)
HEX3[2]	Output	PIN_AD19	4A	B4A_N0	PIN_AD19	2.5 V		12mA (default)	1 (default)
HEX3[1]	Output	PIN_W19	4A	B4A_N0	PIN_W19	2.5 V		12mA (default)	1 (default)
HEX3[0]	Output	PIN_Y19	4A	B4A_N0	PIN_Y19	2.5 V		12mA (default)	1 (default)
HEX4[6]	Output	PIN_AH22	4A	B4A_N0	PIN_AH22	2.5 V		12mA (default)	1 (default)
HEX4[5]	Output	PIN_AF23	4A	B4A_N0	PIN_AF23	2.5 V		12mA (default)	1 (default)
HEX4[4]	Output	PIN_AG23	4A	B4A_N0	PIN_AG23	2.5 V		12mA (default)	1 (default)
HEX4[3]	Output	PIN_AE23	4A	B4A_N0	PIN_AE23	2.5 V		12mA (default)	1 (default)
HEX4[2]	Output	PIN_AE22	4A	B4A_N0	PIN_AE22	2.5 V		12mA (default)	1 (default)
HEX4[1]	Output	PIN_AG22	4A	B4A_N0	PIN_AG22	2.5 V		12mA (default)	1 (default)
HEX4[0]	Output	PIN_AD21	4A	B4A_N0	PIN_AD21	2.5 V		12mA (default)	1 (default)
HEX5[6]	Output	PIN_AB21	4A	B4A_N0	PIN_AB21	2.5 V		12mA (default)	1 (default)
HEX5[5]	Output	PIN_AF19	4A	B4A_N0	PIN_AF19	2.5 V		12mA (default)	1 (default)
HEX5[4]	Output	PIN_AE19	4A	B4A_N0	PIN_AE19	2.5 V		12mA (default)	1 (default)
HEX5[3]	Output	PIN_AG20	4A	B4A_N0	PIN_AG20	2.5 V		12mA (default)	1 (default)
HEX5[2]	Output	PIN_AF20	4A	B4A_N0	PIN_AF20	2.5 V		12mA (default)	1 (default)
HEX5[1]	Output	PIN_AG21	4A	B4A_N0	PIN_AG21	2.5 V		12mA (default)	1 (default)
HEX5[0]	Output	PIN_AF21	4A	B4A_N0	PIN_AF21	2.5 V		12mA (default)	1 (default)
clk	Input	PIN_AJ4	3B	B3B_N0	PIN_AJ4	2.5 V		12mA (default)	
<<new node>>									

Hardware Implementation:



22B[EC1205]

Result:

The 7-segment display was successfully designed and implemented using Verilog on the DE10 FPGA board. The registration number ‘EC1205’ was displayed correctly on the 7-segment display using proper multiplexing and segment encoding techniques. The functionality was verified through simulation and hardware testing, ensuring correct digit transitions and adequate illumination of segments.