Register Number | | | | | | | | | |

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Computer Science and Engineering

Continuous Assessment Test – II

Question Paper

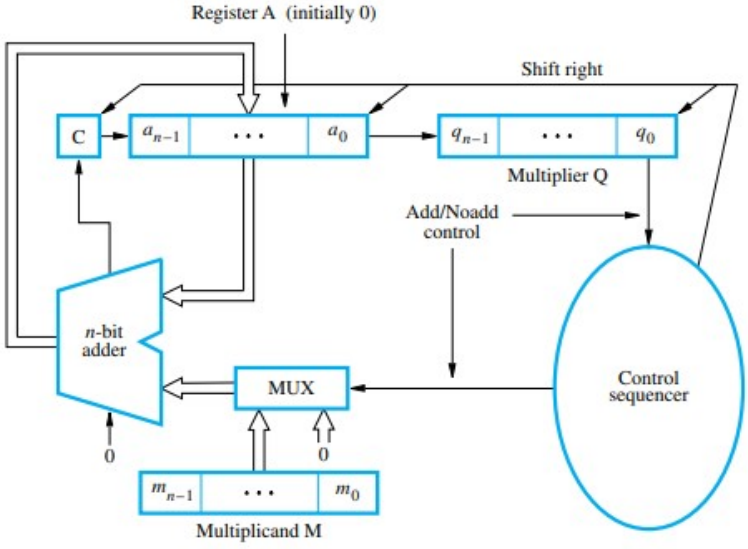
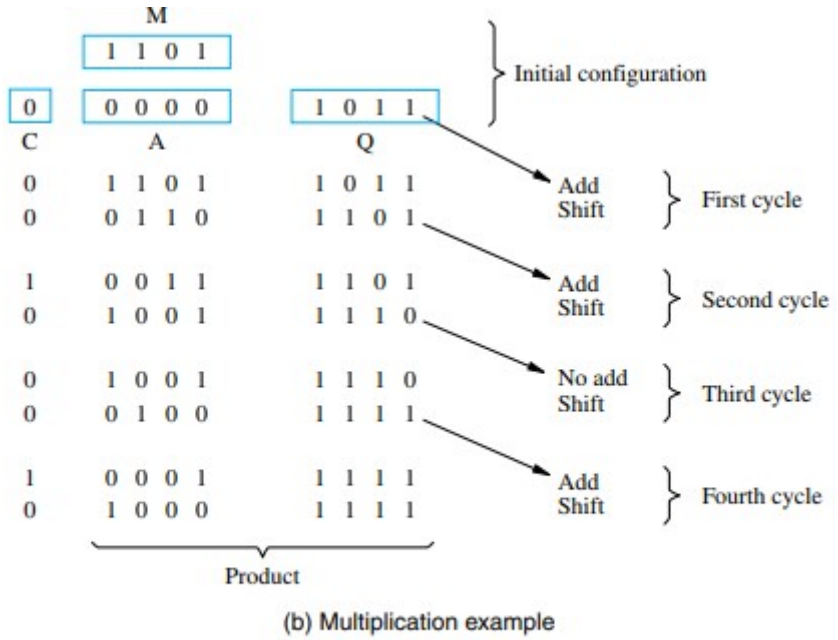
Degree & Branch	B.E. & Computer Science and Engineering				**Semester**	IV
Subject Code & Name	UCS1401 & Computer Organization and Architecture				**Regulation:**	**2018**
Academic Year	2021-2022	**Batch**	2020-2024	**Date**	**3-05-2022**	**FN**
Time: 90 Minutes	**Answer All Questions**				**Maximum: 50 Marks**	

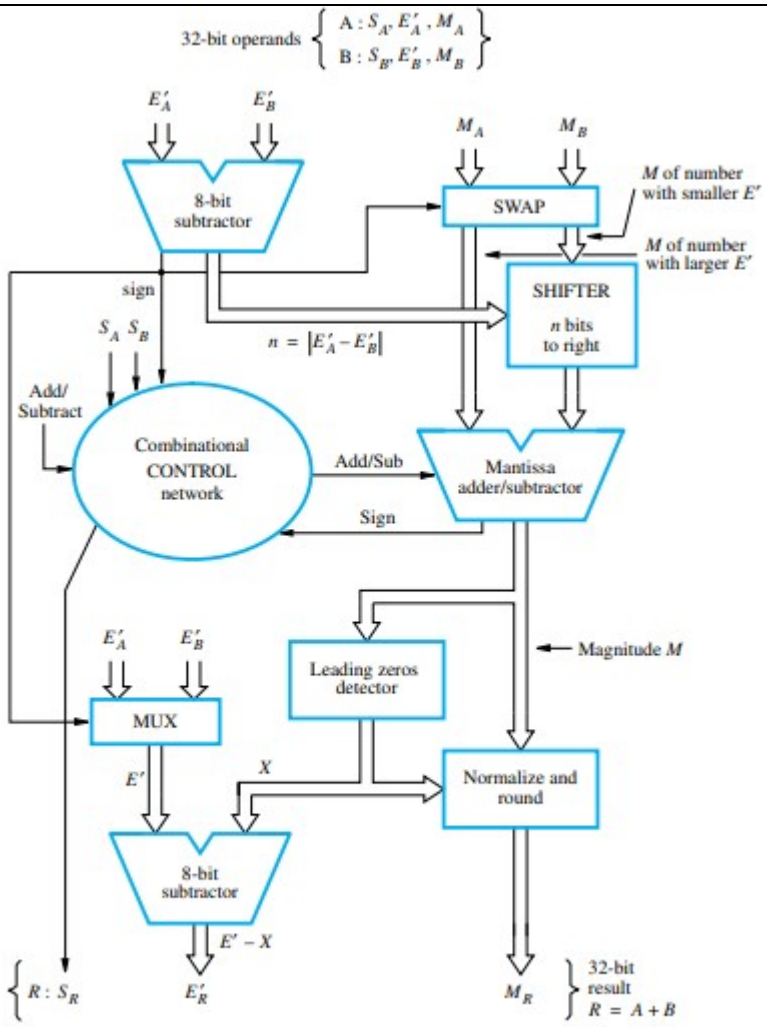
Part – A (6×2 = 12 Marks)

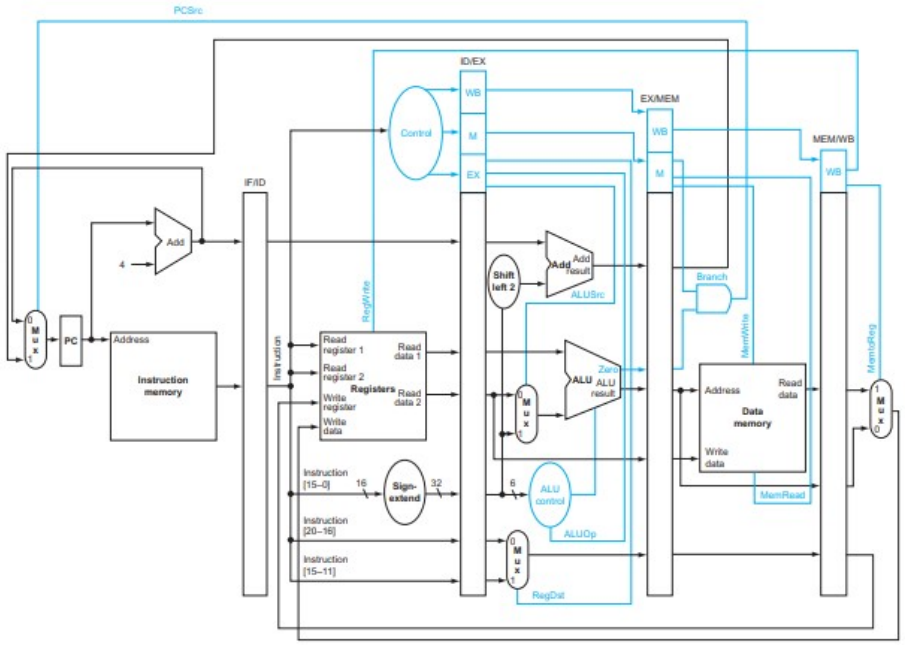
Knowle-dge Level	Question	Course Outcome	Performa-nce Indicator
K2	1. What are the advantages of bit pair recoding in multiplication? ANS: • speeding up the multiplication operation • guarantees that the maximum number of summands (versions of the multiplicand) that must be added is n/2 for n-bit operands	CO2	1.3.1
K2	2. How PCSrc control signal in MIPS datapath is generated? ANS: To generate the PCSrc signal, we will need to AND together a signal from the control unit, which we call Branch, with the Zero signal out of the ALU	CO2	1.4.1
K2	3. During the multiplication process of single precision floating point numbers, What operation needs to be performed for biasing the exponent of result. ANS: Subtract 127	CO2	1.3.1
K2	4. What are the bias values for IEEE single precision and double precision floating point representations? ANS: 127 and 1023	CO2	1.4.1
K2	5. What is need for sign bit extension in MIPS architecture? ANS: Th e sign extension unit has a 16-bit input that is sign-extended into a 32-bit result Sign-extend To increase the size of a data item by replicating the high-order sign bit of the original data item in the highorder bits of the larger, destination data item	CO3	1.3.1
K2	6. List the merits of pipelining. ANS: • Increase in the throughput	CO3	1.3.1

	• Increase in the number of pipeline stages increases the number of instructions executed simultaneously. • Pipelining increases the overall performance of the CPU.		

Part – B (3×6 = 18 Marks)

K3	7. Explain 13 x 11 by using sequential circuit for binary multiplication. ANS: Multiplication of two n-bit numbers can also be performed in a sequential circuit that uses a single n-bit adder  (a) Register configuration  (b) Multiplication example Sequential circuit binary multiplier.	CO2	2.1.3 2.2.2
K2	8. Draw the block diagram of Floating point addition/Subtraction unit and explain ANS:	CO2	1.3.1 1.4.1 2.1.3 2.2.2 13.3.1

	 Floating-point addition-subtraction unit. 1. The first step is to compare exponents to determine the number of times the mantissa of the smaller exponent to be shifted. 2. The shift value n is then given to the shifter unit to shift the mantissa of the smaller number. 3. The sign of the exponent after subtraction determines which is smaller or which is larger no and thereby to shift the mantissa of the smaller number. 4. The mantissas are added / subtracted. 5. The result is normalized by truncating the leading zeros and by subtracting E′ by X, the number of leading zeros		
K2	9. Explain MIPS Pipeline architecture with diagram ANS: Stages of Pipeline 1. IF: Instruction fetch 2. ID: Instruction decode and register fi le read 3. EX: Execution or address calculation 4. MEM: Data memory access 5. WB: Write back	CO3	2.2.2 3.2.2 3.3.1 13.3.1 13.3.2

Part – C (2×10 = 20 Marks)

K3	10. Explain the multiplication of (+13) and (-6) by using Booth Algorithm and bit pair recoding ANS: Booth multiplier recoding table. Table bit-pair recoding. Booth multiplier bit-pair recoding.	CO2	1.3.1 2.1.3
	(OR)		
K3	11. Explain restoring division method for 1010 by 0011. ANS:	CO2	1.3.1 2.1.3

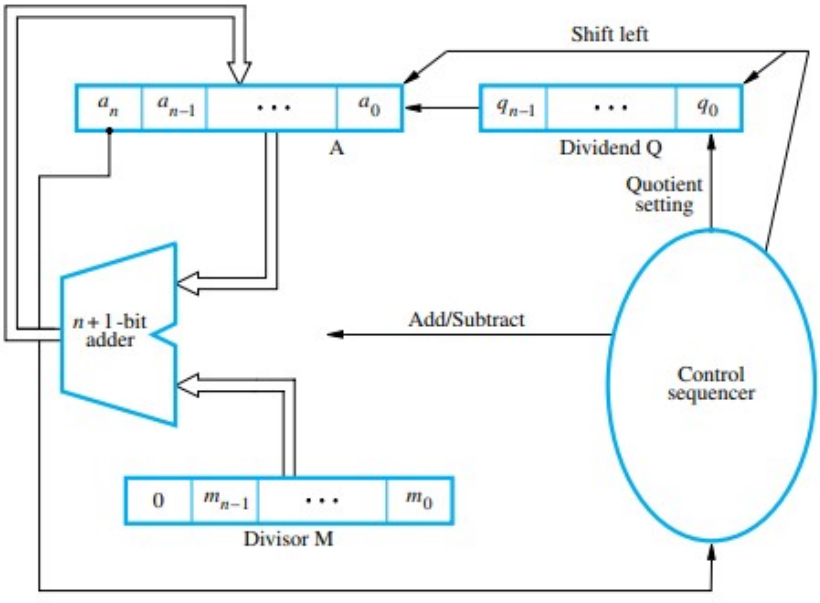
Multiplier		Version of multiplicand selected by bit i
Bit i	Bit $i-1$	
0	0	$0 \times M$
0	1	$+1 \times M$
1	0	$-1 \times M$
1	1	$0 \times M$

Multiplier bit-pair		Multiplier bit on the right	Multiplicand selected at position i
$i+1$	i	$i-1$	
0	0	0	$0 \times M$
0	0	1	$+1 \times M$
0	1	0	$+1 \times M$
0	1	1	$+2 \times M$
1	0	0	$-2 \times M$
1	0	1	$-1 \times M$
1	1	0	$-1 \times M$
1	1	1	$0 \times M$

```
  0 1 1 0 1   (+13)
× 1 1 0 1 0   (−6)
```

```
                    0  1  1  0  1
                    0 −1 +1 −1  0
0 0 0 0 0   0  0  0  0  0
1 1 1 1 1   1  0  0  1  1
0 0 0 0 1   1  0  1
1 1 1 0 0   1  1
0 0 0 0 0   0
1 1 1 0 1   1  0  0  1  0   (−78)
```

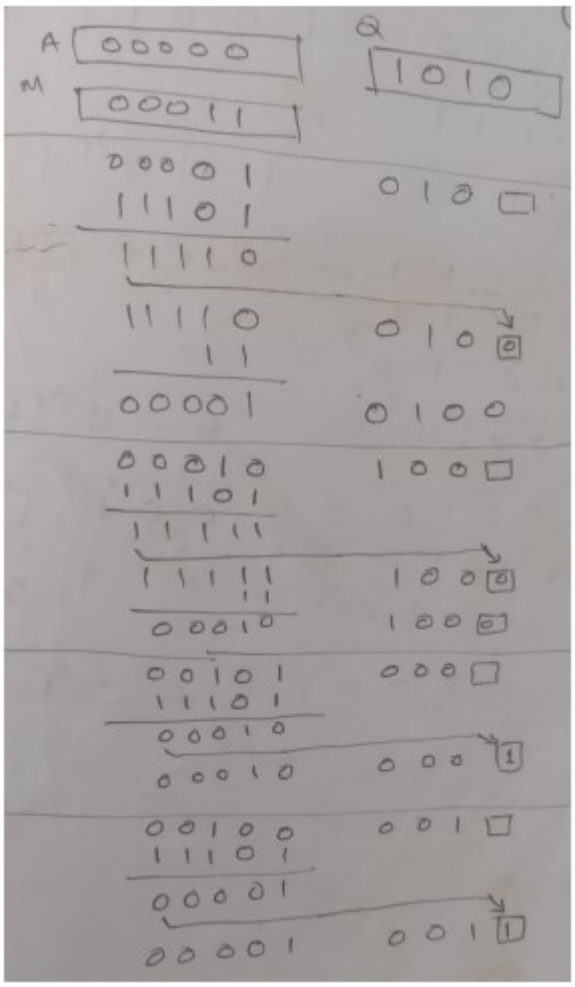
```
                    0  1  1  0  1
                    0    −1    −2
1 1 1 1 1   0  0  1  1  0
1 1 1 1 0   0  1  1
0 0 0 0 0   0  0
1 1 1 0 1   1  0  0  1  0
```



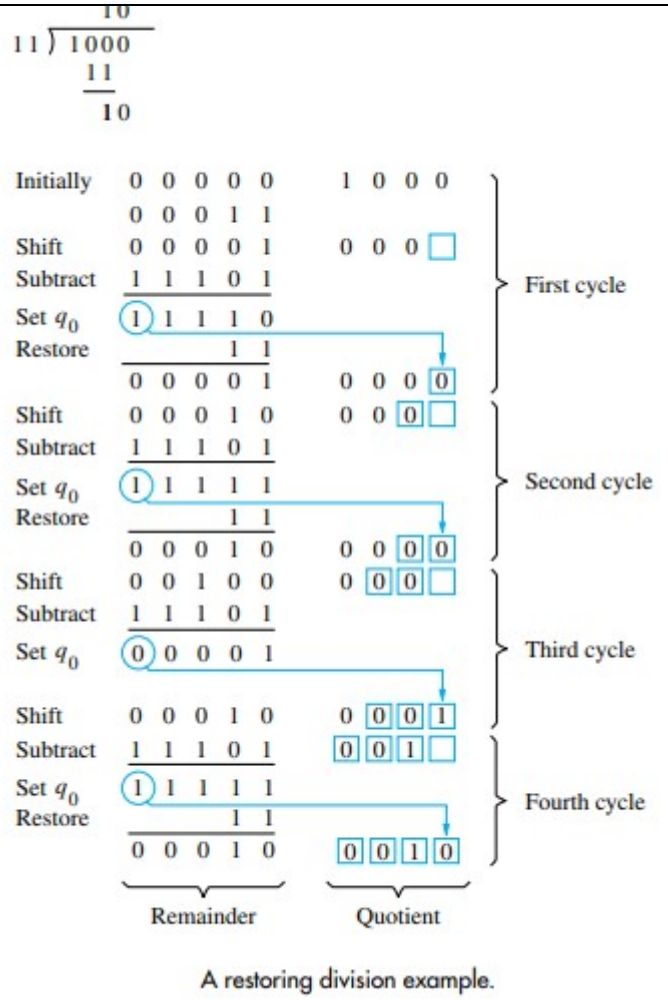
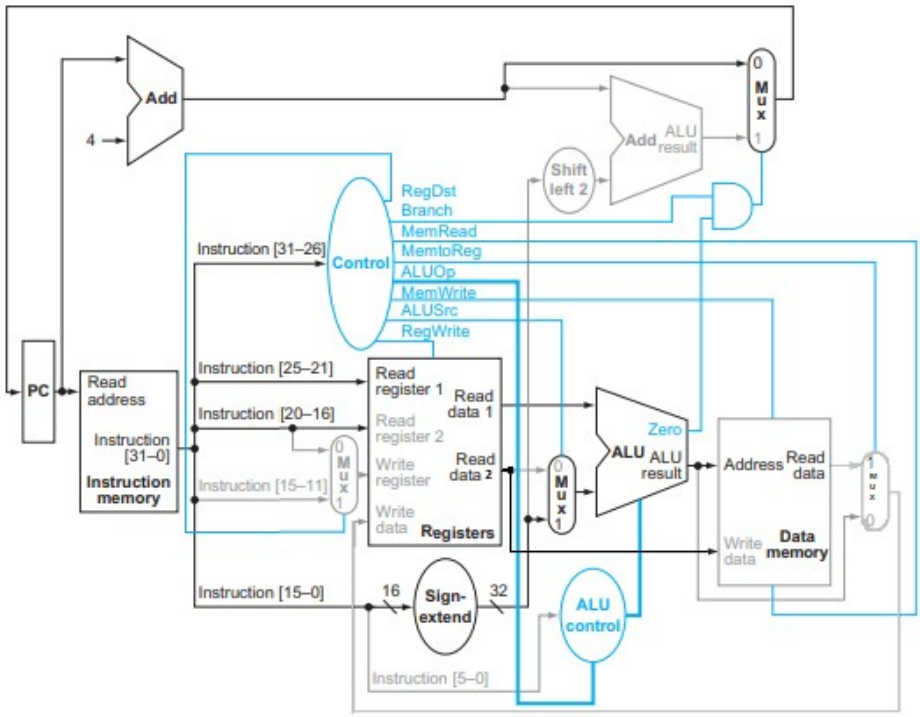
Circuit arrangement for binary division.

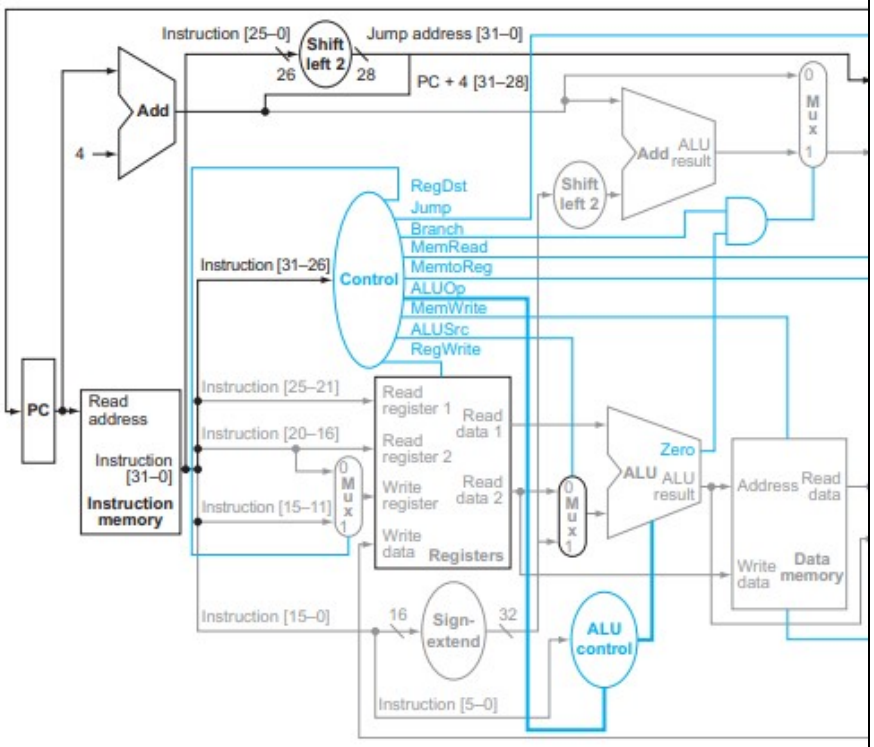
Do the following three steps n times:

1. Shift A and Q left one bit position.
2. Subtract M from A, and place the answer back in A.
3. If the sign of A is 1, set q0 to 0 and add M back to A (that is, restore A); otherwise, set q0 to 1



Book example

	 A restoring division example.		
K3	12. Design a complete data path and control path implementation of MIPS Architecture that supports Store word operations ANS; 	CO3	2.2.2 2.2.3 3.2.2 3.3.1
	(OR)		
K3	12. Design a complete data path and control path implementation of MIPS Architecture that supports unconditional branch	CO3	2.2.2 2.2.3 3.2.2

	ANS:  		3.3.1

Prepared By Dr. D.Venkata Vara Prasad Dr.S.Saraswathi	Reviewed By	Approved By
Course Coordinator	PAC Team	HOD