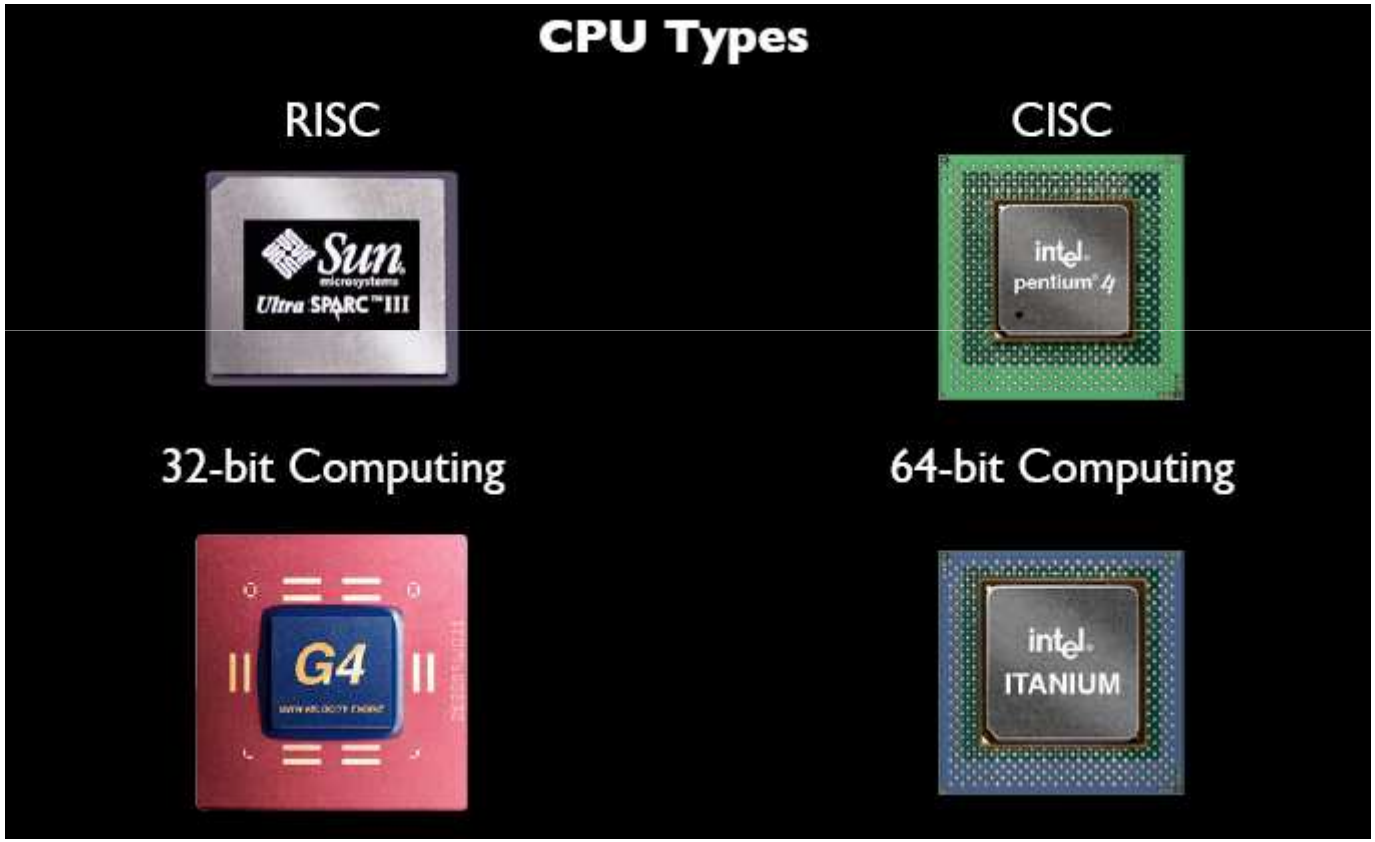
Content Beyond Syllabus

RISC Vs CISC


CPU Types
RISC
CISC
Sun
microsystems
Ultra SPARC™III
intel
pentium 4
32-bit Computing
64-bit Computing
G4
intel
ITANIUM

RISC Vs CISC

- **Reduced Instruction Set Architecture (RISC) –**
  The main idea behind this is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating, and storing operations just like a load command will load data, a store command will store the data.
- **Complex Instruction Set Architecture (CISC) –**
  The main idea is that a single instruction will do all loading, evaluating, and storing operations just like a multiplication command will do stuff like loading data, evaluating, and storing it, hence it's complex.
- Both approaches try to increase the CPU performance
- **RISC:** Reduce the cycles per instruction at the cost of the number of instructions per program.

- **CISC:** The CISC approach attempts to minimize the number of instructions per program but at the cost of an increase in the number of cycles per instruction.
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RISC	CISC
Reduced Instruction Set Computer	Complex Instruction set computer
Less number of instructions (64-100)	More number of instructions. (100-250)
Fixed length instruction formats (32 bits)	Variable length instruction formats (32 bits)
Limited addressing modes (3-5)	More addressing modes (12-24)

RISC	CISC
More no. of general purpose registers (32-192)	Limited no. of general purpose registers (8-20)
It employs H/w control organization.	It employs micro-program control organization. Recent architectures Employ h/w tech
It does not uses control memory	It uses control memory
Memory manipulation instructions are available	No memory manipulation instructions are available. Memory access is limited to simple LOAD/STORE instructions

RISC	CISC
Split caches were used	Unified cache was used. Now a days split caches were used
Clock speed (50-150Mhz in 1992)	Clock speed (33-50Mhz in 1992)
SPARC,DLX,MIPS architectures	Intel 80x86,Motorola MC68000 series