Register Number | | | | | | | | | |

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Computer Science and Engineering

Continuous Assessment Test – III

Question Paper

Degree & Branch	B.E. & Computer Science and Engineering				**Semester**	IV
Subject Code & Name	UCS1401 & Computer Organization and Architecture				**Regulation:**	**2018**
Academic Year	2021-2022	**Batch**	2020-2024	**Date**	**26-05-2022**	**FN**
Time: 90 Minutes 8:30am-10:00am	**Answer All Questions**				**Maximum: 50 Marks**	

Part – A (6×2 = 12 Marks)

Knowle-dge Level	Question	Course Outcome	Performa-nce Indicator
K3	1. Given ROM size of 512KB, estimate the number of address lines and data lines needed to access the memory.	CO4	1.3.1
K2	2. Show the structure of the memory hierarchy.	CO4	1.3.1
K2	3. Classify the different cache mapping methods.	CO4	1.3.1
K2	4. Explain write through policy.	CO4	1.3.1
K1	5. What are multicore architectures?	CO5	1.3.1
K1	6. List examples of processors for SIMD architectures.	CO5	1.3.1

Part – B (3×6 = 18 Marks)

K3	7. In a direct mapped cache with a capacity of 16kB and a line length of 32 bytes. Estimate the number of bits used to access a byte in a cache line. Estimate the number of bits used to select the line in the cache that may contain the data.	CO4	1.3.1 1.4.1
K3	8. A computer uses RAM chips of 1024x1 bit capacity. a) Identify the number of chips needed to construct a memory capacity of 1024 bytes. b) Identify the number of chips needed to provide a memory capacity of 16 kilobytes.	CO4	1.4.1 2.2.3
K2	9. Explain the Flynn's classification of parallel processing models.	CO5	1.3.1

Part – C (2×10 = 20 Marks)

K3	10. A two way set associative cache memory uses a block size of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128k x 32. a) Identify all pertinent information to construct a cache memory. b) Identify the size of the cache memory.	CO4	3.2.2 13.3.1
	(OR)		
K3	11. Construct a static RAM memory of size 2M x 32 memory module using 512K x 8 static memory	CO4	3.2.2 13.3.1

K2	12. What are the differences between CPU and GPU architectures? Explain the architecture of Graphics processing units.	CO5	1.3.1
	(OR)		
K2	13. What are the limitations of single core processors? Explain multicore architectures. List the applications of multicore architectures.	CO5	1.3.1