# Unit-3 Problems

1) Consider the following code.

```
DIV   R2 , R5 , R8
SUB   R9 , R2 , R7
ADD   R5 , R14, R6
MUL   R11, R9 , R5
BEQ   R10, #10 , R12
OR    R8 , R15, R2
```

a. Identify all of the RAW hazards in the above instruction sequence
b. Identify all of the WAR hazards in the above instruction sequence
c. Identify all of the WAW hazards in the above instruction sequence
d. Identify all of the Control hazards in the above instruction sequence

**Ans:** a) RAW ➔ DIV & SUB ; ADD & MUL : SUB & MUL ;DIV & OR
b) WAR ➔ DIV & ADD ; DIV & OR
c) WAW ➔ NONE
d)Control➔ BEQ & OR

2) A unpipeline system tasks 50ns to process a task. The same task can be processed in 6 segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

**Ans:** $t_n = 50ns$
$k = 6$
$t_p = 10ns$
$n = 100$

$$S = \frac{nt_n}{(k+n-1)\,t_p} = \frac{100 \times 50}{(6+99) \times 10} = 4.76$$

$$S_{max} = \frac{t_n}{t_p} = \frac{50}{10} = 5$$

3) Consider an unpipelined processor that has 1ns clock cycle and it uses 4 cycles for ALU operation and branch operations and 5 cycles for memory operations. Assume that the relative frequency of these operations are 40%, 20% and 40% respectively. Suppose that due to clock skew and setup , pipelining the processor adds 0.2ns of overhead to the clock ignoring any latency impact, how much speedup in the instruction execution rate will we gain from the pipeline

**Ans**:
The average instruction execution time on the unpipeline processor is
= clk cycle time *Avg CPI
= 1 ns * ((40%+20%)*4 + 40%*5)
=1 ns *4.4
=4.4ns
In the pipelined implementation the clock must run at the speed of the slowest stage plus the overhead which is to be 1+0.2 ns or 1.2 ns.This is the avg instruction execution time.

Speedup = avg instruction execution time unpipelined / avg instruction execution time pipelined = 4.4/1.2 =3.76time

4) The time delay for the 4 segment in the pipeline are as follows t1= 50 ns, t2 = 30 ns, t3 = 95 ns and t4 = 45 ns. The interface register delay time tr = 5 ns
(a) How long would it take to add 100 pairs of numbers in the pipeline?
(b) How can we reduce the total time to about one half of the time calculate in part(a)

**Ans**:
(a) clock cycle =95 + 5 = 100 ns
(b) for n = 100, k = 4, $t_p$ = 100 ns
time to add 100 number = $(k+n-1)t_p$ = (4+99) x 100 = 10,300 ns = 10.3 s
(b) Divide the segment 3 into two segment of 50 + 5 = 55 ns
and 45 + 5 = 50 ns
This makes the $t_p$ = 55 ns , k = 4
Therefore $(k+n-1)\ t_p$ = (5+99) x 55 = 5720 = 5.72 · s

5) Assume that individual stages of the data path have the following latencies:

| IF | ID | EX | MEM | WB |
|---|---|---|---|---|
| 250ps | 400ps | 150ps | 350ps | 200ps |

What is the clock cycle time in a pipelined and non-pipelined processor?

**Ans)** 400ps and 1350ps
For a pipeline processor the segment with longest processing time(ID) =400ps
For non-pipeline processor the sum of all segments processing time= 1350ps

6)
Assume that instructions executed by the processor are broken down as follows:

| ALU | beq | lw | Sw |
|---|---|---|---|
| 40% | 20% | 25% | 15% |

Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

**Ans**: Since store and branch instructions will not write the result to register unit
Only ALU and load writes the result to Register port : 65%

7) Assume that individual stages of the data path have the following latencies:

| IF | ID | EX | MEM | WB |
|---|---|---|---|---|
| 250ps | 400ps | 150ps | 350ps | 200ps |

If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and identify the new clock cycle time of the processor?

**Ans**: The stage with longest processing time can be chosen. ID stage and next highest processing time 350ps

8) Assume the following fragment of MIPS code:

```
lw $s0, 20($t1)
sub $t2, $s0, $t3
```

The individual stages of the datapath have the following latencies:

| IF | ID | EX | MEM | WB |
|---|---|---|---|---|
| 250ps | 350ps | 150ps | 300ps | 200ps |

If the five stage pipelined processor does not have forwarding unit, identify the total latency for executing the above code.

Ans: 2800ps

9) What is the longest chain of dependent operations (including the name dependencies) in the following program?

```
LD      r7,(r8)
SUB     r10,r11,r12
MUL     r13,r7,r11
ST      (r9),r13
ADD     r13,r2,r1
LD      r5,(r6)
SUB     r3,r4,r5.
```

Ans:

```
LD      r7,(r8)
MUL     r13,r7,r11
ST      (r9),r13
ADD     r13,r2,r1
```