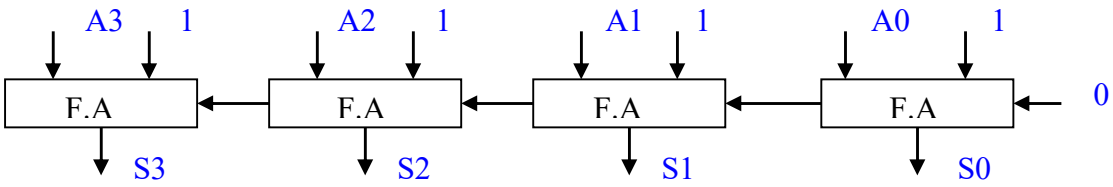
1) Design a 4 bit combinational circuit decrementer using 4 FA's

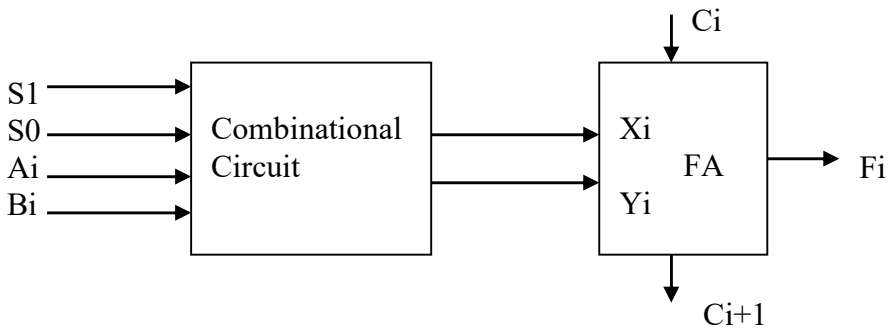


A-1=A + 2'S Complement of 1
= A +1111.

2) An arithmetic circuit has 2 selection variables S1 and S0. The arithmetic operation available in the unit are listed below. Determine the circuit that must be incorporated with the full adder in each stage of the arithmetic circuit.

S1 S0	Ci=0	Ci=1
0 0	F= A+B	F=A+B+1
0 1	F=A	F=A+1
1 0	$F=\overline{B}$	$F=\overline{B}+1$
1 1	$F=A+\overline{B}$	$F=A+\overline{B}+1$

Solution:
Let the input tto the full adder circuit can be Xi & Yi



$Xi = Ai\overline{S1} + Ai\ S0$

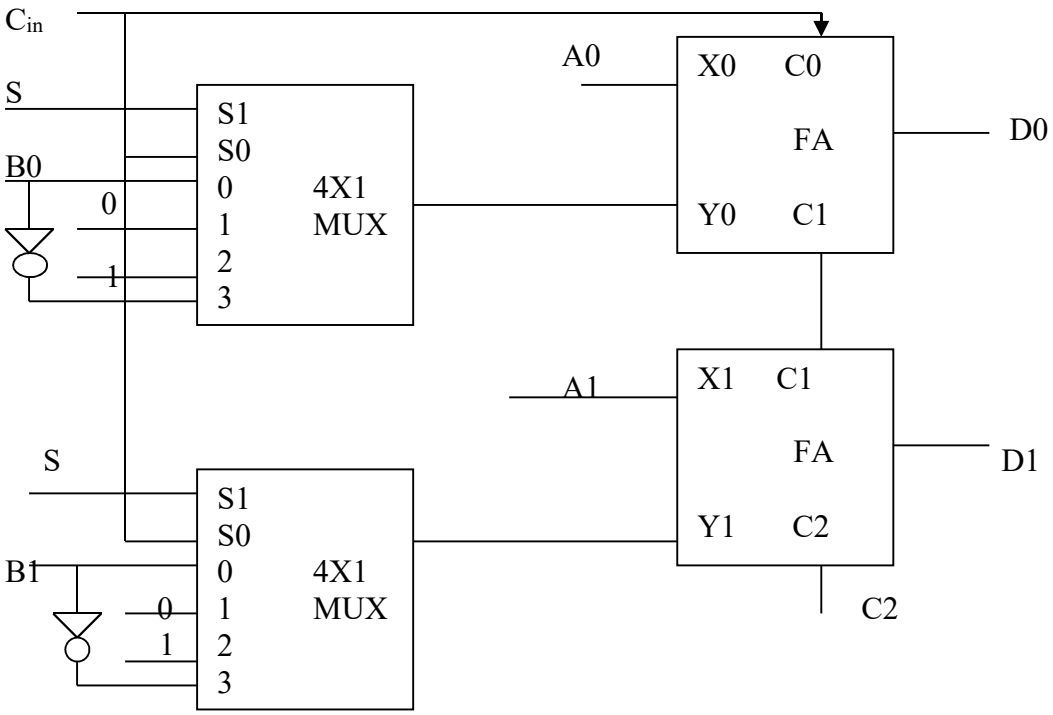
$Yi = Bi\ \overline{S1}\ \overline{S0} + \overline{Bi}\ S1$

S1 S0 Ai Bi	Xi Yi	Function
0 0 0 0	0 0	Xi= Ai Yi= Bi
0 0 0 1	0 1	
0 0 1 0	1 0	
0 0 1 1	1 1	
0 1 0 0	0 0	Xi=Ai Yi=0
0 1 0 1	0 0	
0 1 1 0	1 0	
0 1 1 1	1 0	
1 0 0 0	0 1	Xi=0 Yi=$\overline{Bi}$
1 0 0 1	0 0	
1 0 1 0	0 1	
1 0 1 1	0 0	
1 1 0 0	0 1	Xi=Ai Yi=Bi
1 1 0 0	0 0	
1 1 0 0	1 1	
1 1 0 0	1 0	

3) Design an arithmetic circuit with one selection variable S and two data inputs A & B The circuit generates the following 4 arithmetic operations in conjunction with the input carry Cin . Draw the logic diagram for the first two stages.

S	Cin=0	Cin=1
0	D=A+B (add)	D=A+1(increment)
1	D=A-1(decrement)	D=A+$\overline{B}$+1(sub)

S	Cin	X	Y
0	0	A	B (A+B)
0	1	A	0 (A+1)
1	0	A	1(A-1)
1	1	A	$\overline{B}$ (A-B)


Cin
S
B0
0
1
S1
S0
0
1
2
3
4X1
MUX
A0
X0
C0
FA
Y0
C1
D0
A1
X1
C1
FA
Y1
C2
D1
C2
S
B1
0
1
S1
S0
0
1
2
3
4X1
MUX