# Unit-4 Problems

# Problem 1

- How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes.
- How many lines of address bus must be used to access 2048 bytes of memory. How many of these lines will be common to all chips.
- How many lines must be decoded for the chip select ? specify the size of the decoder.

# Sol 1

- 2048/128 =16 chips.
- 2048 = (2 power 11) = 11 address lines are needed to address 2048 bytes.
- 128 = (2 power 7) = 7 lines to address the chip.

  ----

  4 lines to decoders for selecting the16 chips.
- 4x16 decoder.

# Problem2

- A computer uses RAM chips of  1024x1 capacity.
  - How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes. The memory is bit addressable.
  - How many chips are needed to provide a memory capacity of 16kB. Explain in words how the chips are to be connected to the address bus

# Sol 2

- 8 chips are needed with the address lines connected in parallel.
- 16x8 = 128 chips.
- Use 17 address lines ( 16x1024x8 )
- 7 lines to specify the chip address
- 10  lines are to select a location in a chip.

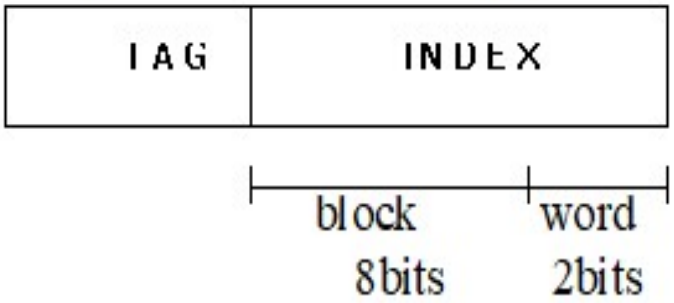
# Problem 3

- A two way set associative cache memory uses a block size of 4 words . The cache can accommodate a total of 2048 words from main memory. The main memory size is 128kx32.
- Formulate all pertinent information required to construct the cache memory.
- What is the size of the cache memory.

# Sol 3

128k =(2 power 17) ; for a set size of 2, the index address has 10 bits to accommodate 2048/2=1024 words of cache.

a) 7 10 =17 Bits




b)


size of the cache is →1024*2(7+32)=1024*78

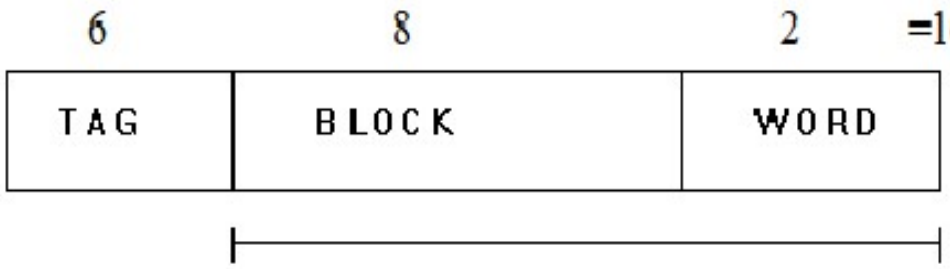
# Problem 4

- A digital computer has a memory capacity of 64kx16 and a cache memory of 1k words. The cache uses a direct mapping with a block size of 4 words
- How many bits are there in the tag , index, block and word fields of the address formats.
- How many bits are there in each word of the cache , how they are divided in to function ? Include a valid bit.
- How many blocks can the cache can accommodate.

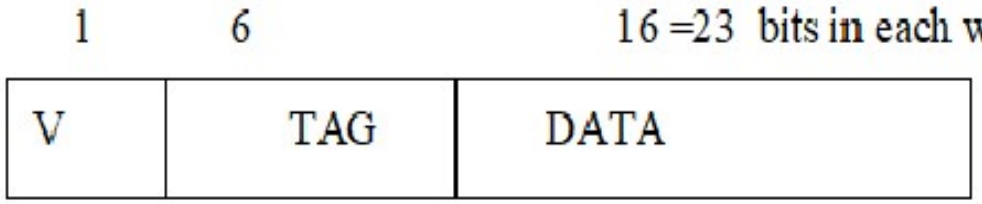
# Sol 4

64kx16=16bit address ; 16 bit data

a)




b)




c)2( power 8) =256 blocks of 4 words each.

# Problem 5

- In a direct mapped cache with a capacity of 16kB and a line length of 32 bytes . How many  bits are used to determine the byte that a memory operation reference with in a cache line , and how many bits are used to select the line in the cache that may contain the data

# Sol 5

- Log32 =5 . 5 bits are required to determine which byte in a cache line is being referenced .
- With 32 byte lines , there are 512 lines in the 16kB cache , so 9 bits are requested to select the line that may contain the address. (log512=9)

# Problem 6

- If a cache has 64 byte cache lines how long does it take to fetch cache line , if the main memory takes 20 cycles to responds to each memory request and return 2 bytes of data in response to each request.

# Sol 6

- Since the main memory  returns 2 bytes of data in response to each request , 32 memory requests are needed to fetch the line. At 20 cycles per request fetching a cache line will take 640 cycles