SSN COLLEGE OF ENGINEERING, KALAVAKKAM
Autonomous
Affiliated to Anna University, Chennai
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Subject	: Computer Organization And Architecture	Class	: IV Sem A / B
Sub. Code	: UCS1401	Acad. Year	: 2021-2022 (Even)
Staff Incharge	: Dr. D. Venkata Vara Prasad /Dr. S.Saraswathi	Batch	: 2020-2024
Regulation	:2018	LTPC	: 3 0 0 3

LESSON PLAN

Content Delivery Methods (CDM) : Chalk and Blackboard , LMS, Use of ICT / (for all topics); T - Tutorial

S.No.	Topic	KnowledgeLevel	No of Hours		Remarks
			Proposed	Actual	
UNIT I – BASIC STRUCTURE OF A COMPUTER SYSTEM –			**9 Hrs**		
1	Introduction and functional Units.	K1	1		
2	Basic Operational Concepts–Performance	K2	1		
3	Instructions: Language of the Computer – Operations, Operands	K2	2		
4	Instruction representation and addressing modes	K2	1		
5	Logical operations	K1	1		
6	decision making	K2	1		
7	MIPS Addressing	K2	2		
UNIT II – ARITHMETIC FOR COMPUTERS –			**9 Hrs**		
8	Addition and subtraction	K2	2		
9	Multiplication	K3	3		
10	Division	K2	1		
11	Floating Point Representation and operations	K3	2		
12	Subword parallelism	K2	1		
UNIT III – PROCESSOR AND CONTROL UNIT -			**9 Hrs**		
14	A Basic MIPS implementation	K2	1		
15	Building datapath	K3	1		
16	Control Implementation scheme	K3	1		
17	Pipelining	K2	1		
18	Pipelined datapath and control	K3	2		
19	Handling Data hazards & Control hazards	K3	1		
20	Exception handling.	K2	1		

21	Issues in predictive branching: Spectre andmeltdown	K2	1		
UNIT IV - MEMORY AND I/O SYSTEMS -			**9 Hrs**		
22	Memory Introduction and hierarchy	K1	1		
23	Memory technologies	K1	1		
24	Cache memory	K3	1		
25	Measuring and improving cache Performance	K3	1		
26	Virtual memory and TLBs	K2	1		
27	Accessing I/O Devices	K2	1		
28	Interrupts, Direct Memory Access	K2	1		
29	Bus structure – Bus operation – Arbitration	K1	1		
30	Interface circuits - USB	K1	1		
UNIT V – PARALLEL PROCESSORS –			**9 Hrs**		
31	Parallel processing challenges	K2	1		
32	Flynn's classification	K1	1		
33	Vector Architectures	K1	2		
34	Hardware multithreading	K2	1		
35	Multicore processors and other SharedMemory Multiprocessors	K2	3		
36	Introduction to Graphics ProcessingUnits	K1	1		
TOTAL			45		

Total Number of Syllabus Hours : 45
Total Number of Planned Hours : 45

Assessment Tools for assessing COs

Assessment Tool	CO1	CO2	CO3	CO4	CO5	Weightage
CAT 1 (Units 1, 2)	**Y**	**Y**				Best 2 X15=30
CAT 2 (Units 2, 3)		**Y**		**Y**		
CAT 3 (Units 4,5)			**Y**		**Y**	
Assignment			**Y**			10
Semester Examination	**Y**	**Y**	**Y**	**Y**	**Y**	**60**
					Total	**100**

Prepared By **Reviewed by** **Approved by**

Dr. D. Venkata Vara Prasad
Dr.S.Saraswathi PAC Team HOD/CSE