Problem 1

- How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes.
- How many lines of address bus must be used to access 2048 bytes of memory. How many of these lines will be common to all chips.
- How many lines must be decoded for the chip select ? specify the size of the decoder.

Soln:

2048*8 = 16*128*8

16 chips are needed

2048 = 2^{11} -> so 11 address lines needed to access 2048 bytes (byte addressable memory)

16 chips =2^4 chips -> so 4 address line to refer to 16 chip -> we need 4 to 16 line decoder

Problem2

A computer uses RAM chips of 1024x1 capacity.

- How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes. The memory is **bit addressable**.
- How many chips are needed to provide a memory capacity of 16kB. Explain in words how the chips are to be connected to the address bus

oln:

1024*8 need 8 chips of 1024 * 1 capacity

address lines connected in parallel

16KB = 16*1024*8 = 16*8*1024*1 = 16*8 chips of 1024 * 1 capacity

= 128 chips are needed $=2^7$ chips

address lines (16x1024x8) = $2^4 * 2^{10} * 2^3$

$= 2^{17}$

= 17 address lines are needed

128 chips $=2^7$ chips need 7 lines to specify the chip address

10 lines are to select a location in a chip (bit address)

Problem 3

- A two way set associative cache memory uses a block size of 4 words . The cache can accommodate a total of 2048 words from main memory. The main memory size is 128kx32.
- Formulate all pertinent information required to construct the cache memory.
- What is the size of the cache memory.

Soln:

Cache size = 2048 words = 2^{11} address lines

=2048/4 =512 blocks of 4 words each

= 512/2 = 256 set with 2 blocks each

Main memory 128K*32 = 128K words

=128*1024 words

=2^7 * 2^{10}

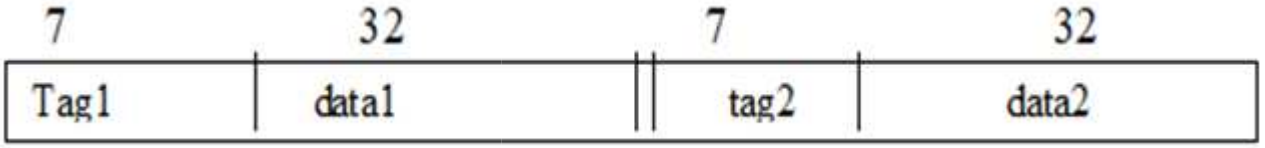
=2^{17}

=2^{15} * 2^2 words = 2^7 * 2^8 * 2^2

7 Tag	8 set	2 word

A cache memory holds 7 bit tag field and 32 bit data

A set consists of two 7 bit tag and 32 bit data



Problem 4

- A digital computer has a memory capacity of 64kx16 and a cache memory of 1k words. The cache uses a direct mapping with a block size of 4 words
- How many bits are there in the tag , index, block and word fields of the address formats.
- How many bits are there in each word of the cache , how they are divided in to function ? Include a valid bit.
- How many blocks can the cache can accommodate.

Soln:

MM: 64K*16 = 64*1024 words $= 2^6 * 2^{10}$ words

= 64*1024/4 blocks = 64*256 blocks

= $2^6 * 2^8$ blocks (of 2^2 words)

Cache: 1K words =1024 words = 1024/4 blocks

= 256 blocks = 2^8 blocks

Each word of the cache has

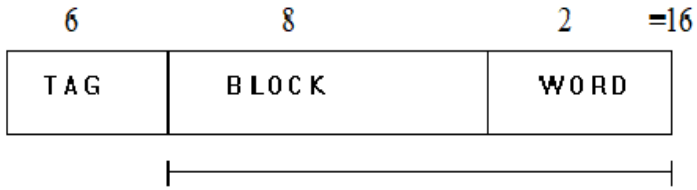
1 bit for V

6 bit tag

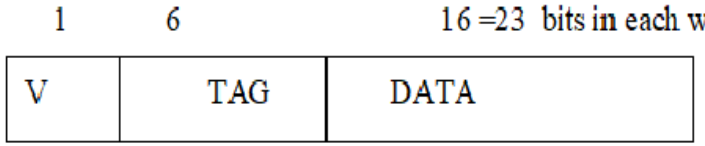
16 bit of data (word)

64kx16=16bit address ; 16 bit data

a)



b)



c)2(power 8) =256 blocks of 4 words each.

Problem 5

- In a direct mapped cache with a capacity of 16kB and a line length of 32 bytes . How many bits are used to determine the byte that a memory operation reference with in a cache line , and how many bits are used to select the line in the cache that may contain the data

Soln:

Cache: 16KB of Block size =32 bit

16*1024 bytes

(16*1024)/ 32 blocks

512 blocks = 2^9 blocks of 2^5 bytes

5 bits are required to determine which byte in a cache line is being referenced

9 bits are requested to select the line

Problem 6

- If a cache has 64 byte cache lines how long does it take to fetch cache line , if the main memory takes 20 cycles to responds to each memory request and return 2 bytes of data in response to each request.

Soln:

64 byte cache line (block)

2 bytes are accessed for each memory access

64/2 =32 so 32 memory access is needed

Each access takes 20 cycles

32*20 =640 cycles to load 64 bytes into cache