COURSE CODE	COURSE TITLE	L	T	P	C
UCS1401	**COMPUTER ORGANIZATION AND ARCHITECTURE**	3	0	0	3

OBJECTIVES
- To learn the basic structure and operations of a computer
- To learnthe arithmetic andlogic unitandimplementation of fixed-point and floating-point arithmetic unit
- To learn the basics of pipelined execution
- To understand the memory hierarchies, cache andvirtual memories and communication with I/O devices
- To understand parallelism and multi-core processors.

UNIT I   BASIC STRUCTURE OF A COMPUTER SYSTEM   9

Functional Units -- Basic Operational Concepts -- Performance; Instructions: Language of the computer -- Operations, Operands -- Instruction representation; Logical operations -- Decision making; MIPS addressing.

UNIT II   ARITHMETIC FOR COMPUTER   9

Addition and subtraction; Multiplication; Division; Floating Point Representation: Floating point operations; Sub word parallelism.

UNIT III   PROCESSOR AND CONTROL UNIT   9

A Basic MIPS implementation: Building a data path – Control implementation scheme; Pipelining: Pipelined data path and control -- Handling data hazards & Control hazards -- Exceptions -- Issues in predictive branching: Spectre and Meltdown.

UNIT IV   MEMORY & I/O SYSTEMS   9

Memory Hierarchy; Memory technologies; Cache Memory: Measuring and improving cache performance; Virtual Memory: TLBs; Accessing I/O devices -- Interrupts; Direct memory access; Bus structure – Bus operation -- Arbitration; Interface circuits; USB.

UNIT V   PARALLEL PROCESSORS   9

Parallel processing challenges; Flynn's classification: SISD – MIMD -- SIMD -- SPMD and Vector Architectures; Hardware multithreading; Multi-core processors and other shared memory multiprocessors; Introduction to Graphics Processing Units.

                    TOTAL PERIODS: 45

OUTCOMES
On successful completion of this course, the student will be able to:
- Understand the basics structure of computers, operations and instructions(K2)
- Designarithmetic and logic unit (K3)
- Understand pipelined execution and design controlunit (K3)
- Designof various memory systems andunderstand I/O communication(K3)
- Understand parallel processing architectures (K2).

TEXTBOOKS

1. DavidA Patterson, John L Hennessy, "Computer Organization andDesign: The Hardware/Software Interface", 5th Edition,Morgan Kaufmann/ Elsevier, 2014 (Units I, III, IV, V).
2. Carl Hamacher, ZvonkoVranesic, SafwatZaky, NaraigManjikian, "Computer Organization andEmbedded Systems", 6th Edition,Tata McGraw Hill, 2012 (Unit II).

REFERENCE BOOKS

1. William Stallings, "Computer Organization and Architecture – Designing for Performance", 8th Edition,Pearson Education, 2010.
2. John P Hayes,"Computer Architecture andOrganization", 3rdEdition, Tata McGrawHill, 2012.
3. John L Hennessey, David A Patterson, "Architecture – A Quantitative Approach", 5th edition, Morgan Kaufmann / Elsevier, 2012 (Units I, III).
4. MorrisManoM, "Computer SystemArchitecture", Revised3rd Edition, Pearson Publication, 2017.
5. Chakraborty P, "Computer Architecture andOrganization", JAICO PublishingHouse, 2010.