Register Number | | | | | | | | | |

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

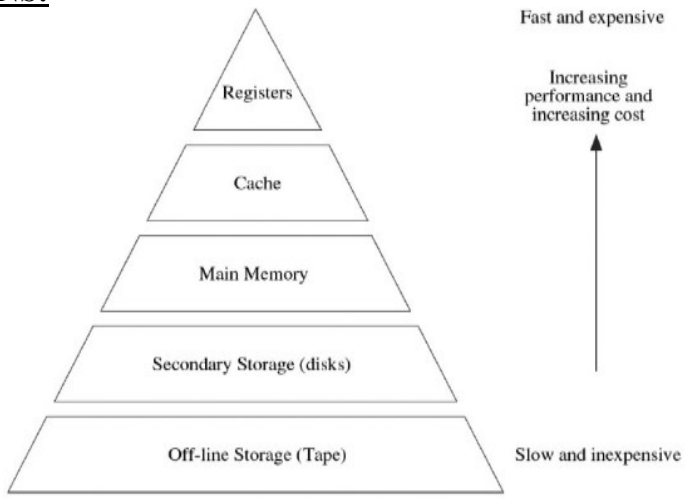
Department of Computer Science and Engineering

Continuous Assessment Test – III KEY

Question Paper

Degree & Branch	B.E. & Computer Science and Engineering				**Semester**	IV
Subject Code & Name	UCS1401 & Computer Organization and Architecture				**Regulation:**	**2018**
Academic Year	2021-2022	**Batch**	2020-2024	**Date**	**26-05-2022**	**FN**
Time: 90 Minutes	**Answer All Questions**				**Maximum: 50 Marks**	

Part – A (6×2 = 12 Marks)

Knowle-dge Level	Question	Course Outcome	Performa-nce Indicator
K1	**1 ANS:** 512 KB Memory needs 19 address lines and 8 data lines.	CO4	1.3.1
K2	2. Show the structure of the memory hierarchy. **ANS:** 	CO4	1.3.1
K2	3 Classify the different cache mapping methods? **ANS:** Direct, Associative and set associative mappings	CO4	1.3.1
K2	4. Explain write through policy. **ANS:** Content of Main memory updated while updating content of cache	CO4	1.3.1
K1	5. What are multicore architectures? **ANS:** A single IC package has core logic of more than one processor. Each core has its own resources like execution pipelines, caches,registers, etc Eg:Dual core, Quad core processors	CO5	1.3.1
K1	6. List examples processors for SIMD architectures. **ANS:**	CO5	1.3.1

	Vector Processors, Multimedia extensions architectures (MMX), GPU processors		

Part – B (3×6 = 18 Marks)

K2	**ANS:** 16KB CACHE MEMORY line size 32 bytes no of lines =16 x 1023/32 = 512 lines line no = 9 bits line offset =5 bits	CO4	1.3.1
K3	8. A computer uses RAM chips of 1024x1 bit capacity. a) Identify the number of chips needed to construct a memory capacity of 1024 bytes b) Identify the number of chips are needed to provide a memory capacity of 16 kilobytes. **ANS:** a) 8 chips are needed with the address lines connected in parallel. b) 16x8 = 128 chips. Use 14 address lines (16k =(2 power 14)) 10 lines to specify the chip address 4 lines are decoded in to 16 chip select inputs.	CO4	1.4.1 2.2.3
K2	9. Explain the Flynn's classification of parallel processing models. **ANS:** SISD, SIMD, MISD, MIMD	CO5	1.3.1

Part – C (2×10 = 20 Marks)

K3	10. A two way set associative cache memory uses a block size of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128k x 32. a) Identify all pertinent information to construct a cache memory. b) Identify the size of the cache memory. **ANS:** 128k =(2 power 17) ; for a set size of 2, the index address has 10 bits to acco 2048/2=1024 words of cache. a) 7 10 =17 Bits TAG INDEX block word 8bits 2bits b) 7 32 7 32 Tag1 data1 tag2 data2 size of the cache is →1024*2(7+32)=1024*78	CO4	3.2.2 13.3.1
	(OR)		
K3	11. Construct a static RAM memory of size 2M x 32 memory module using 512K x 8 static memory **ANS:** 4*4 matrix of 512K * 8 chips	CO4	3.2.2 13.3.1
K2	12. What are the differences between CPU and GPU architectures. Explain the architecture of Graphics processing units. **ANS:**	CO5	1.3.1

	• A GPU is tailored for highly parallel operation while a CPU executes programs serially • For this reason, GPUs have many parallel execution units and higher transistor counts, while CPUs have few execution units and higher clock speeds • A GPU is for the most part deterministic in its operation • GPUs have much deeper pipelines (several thousand stages vs 10-20 for CPUs) • GPUs have significantly faster and more advanced memory interfaces as they need to shift around a lot more data than CPUs		
	(OR)		
K2	• What are the limitations of single core processors. Highlight the merits and demerits of multicore architectures. List the applications of multicore architectures ANS: • Smaller transistors = faster processors. • Faster processors = increased power consumption. • Increased power consumption = increased heat. • Increased heat = unreliable processors • A simple Thump rule is that o For every 1% rise in the clock frequency you will see 3% rise in the power consumption o Thus the heat dissipation also increases. Merits ■ Occupies less space on PCB ■ Higher throughput ■ Consume less power ■ Cache coherency can be greatly improved ■ Performs more operations/sec with less frequency Demerits ■ Maximizing the utilization of the computing resources provided by multi-core processors requires adjustments both to the operating system (OS) support and to existing application software ■ They are more difficult to manage thermally than lower-density single-chip designs Applications: ■ Data base servers	CO5	1.3.1

	■ Web servers ■ Compilers ■ Multimedia Applications ■ Scientific Applications ■ General applications with TLP as opposed to ILP ■ Downloading s/w while running Anti virus s/w ■ Editing photo while recording TV show.		

Prepared By	Reviewed By	Approved By
Dr. D.Venkata Vara Prasad Dr.S.Saraswathi		
Course Coordinator	PAC Team	HOD