Register Number | | | | | | | | | |

Sri Sivasubramaniya Nadar College of Engineering, Kalavakkam – 603 110

(An Autonomous Institution, Affiliated to Anna University, Chennai)

Department of Computer Science and Engineering

Continuous Assessment Test – I

Question Paper

Degree & Branch	B.E. & Computer Science and Engineering				**Semester**	IV
Subject Code & Name	UCS1401 & Computer Organization and Architecture				**Regulation:**	**2018**
Academic Year	2021-2022	**Batch**	2020-2024	**Date**	**26-03-2022**	**FN**
Time: 90 Minutes	**Answer All Questions**				**Maximum: 50 Marks**	

Part – A (6×2 = 12 Marks)

Knowle-dge Level	Question	Course Outcome	Performa-nce Indicator
K1	1. Define Amdahl's law.	CO1	1.3.1 2.1.3
K2	2. Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Infer the addressing mode implemented by this instruction.	CO1	1.3.1
K3	3. The 32-bit Hex value B0A29C47 is stored in the location starting from address 1000. Apply the concept of byte addressing in both Big endian representation and Little endian representation. Identify the value of the byte in address 1002 if the representation is Big endian and if it is Little endian?	CO1	1.3.1
K1	4. A computer has a processor with 24 bit address bus, 32 bit data bus and 8 control lines. Find the maximum amount of memory that the computer can address.	CO1	1.3.1 2.1.3
K3	5. Apply the 2's complement subtraction for the given operation (-2) - (-7). (use 8-bit representation)	CO2	1.3.1 1.4.1 2.1.3 13.3.1
K1	6. What are the advantages of 2's complement over 1's complement?.	CO2	1.3.1

Part – B (3×6 = 18 Marks)

K3	7. A memory unit with a capacity of 65,536 words of 25 bits each. It is used in conjunction with a general-purpose computer. The instruction code is divided into four parts an indirect mode bit, opcode, two bits that specify a processor register and an address part. a. Construct the instruction word format indicating the number of bits and the function of each part. Estimate the following: b. The maximum number of operations that can be in the computer if the instruction is stored in one memory word.	CO1	1.3.1 2.1.3

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<tr><td></td><td>c. How many processor registers are there in the computer and how many bits are there in each processor register?
d. How many bits are there in MAR, MBR and PC?</td><td></td><td></td></tr>
<tr><td>K3</td><td>8. Develop MIPS assembly language program for the following high level language statement while (save[i] == k) i += 1
Assume i in $s3, k in $s5, address of save in $s6.</td><td>CO1</td><td>1.3.1</td></tr>
<tr><td>K2</td><td>9. Explain with neat block diagram a 4 bit adder using carry Look ahead Logic.</td><td>CO2</td><td>1.3.1
1.4.1
2.2.2
13.3.1
13.3.2</td></tr>
</table>

Part – C (2×10 = 20 Marks)

<table>
<tr><td>K3</td><td>10. Consider a Graphics card which is executing a program that consists of 50% of its total execution time is spent in floating point operations(FP) and 20% of its total execution time is spent in floating point square root operations (FPSQR).
Option 1: improve the FPSQR operation by a factor of 10.
Option 2: improve all FP operations by a factor of 1.6
Choose the best design alternative.</td><td>CO1</td><td>1.3.1
2.1.3</td></tr>
<tr><td colspan="3">(OR)</td></tr>
<tr><td>K3</td><td>11. It is required to compare the computers R1 and R2, which differ that R1 has the machine instructions for the floating-point operations, while R2 does not have those instructions. (FP operations are implemented in the software using several non-FP instructions). Both computers have a clock frequency of 400 MHz. If the same program is executed on both the computers, which has the following mixture of instructions:
<table>
<tr><th rowspan="2">Type of the Instruction</th><th rowspan="2">Dynamic share of instructions in program(p)</th><th colspan="2">Instruction Duration (Number of clock periods(CPI))</th></tr>
<tr><th>R1</th><th>R2</th></tr>
<tr><td>FP addition</td><td>16%</td><td>6</td><td>20</td></tr>
<tr><td>FP multiplication</td><td>10%</td><td>8</td><td>32</td></tr>
<tr><td>FP division</td><td>8%</td><td>10</td><td>66</td></tr>
<tr><td>Non- FP instructions</td><td>66%</td><td>3</td><td>3</td></tr>
</table>
a) Calculate the CPI for the computers R1 and R2.
b) Calculate the CPU program execution time on the computers R1 and R2, if there are 12000 instructions in the program?</td><td>CO1</td><td>1.3.1
2.1.3</td></tr>
<tr><td>K2</td><td>12. Explain different types of addressing modes in MIPS architecture with examples.</td><td>CO1</td><td>1.3.1</td></tr>
<tr><td colspan="3">(OR)</td></tr>
<tr><td>K2</td><td>13. Explain different MIPS instruction formats.</td><td>CO1</td><td>1.3.1</td></tr>
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