COURSE: UCS1502 - MICROPROCESSORS AND INTERFACING

8255 – Programmable Peripheral Interface (PPI)

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This presentation covers

• Details of 8255 chip

Learning outcome of this module

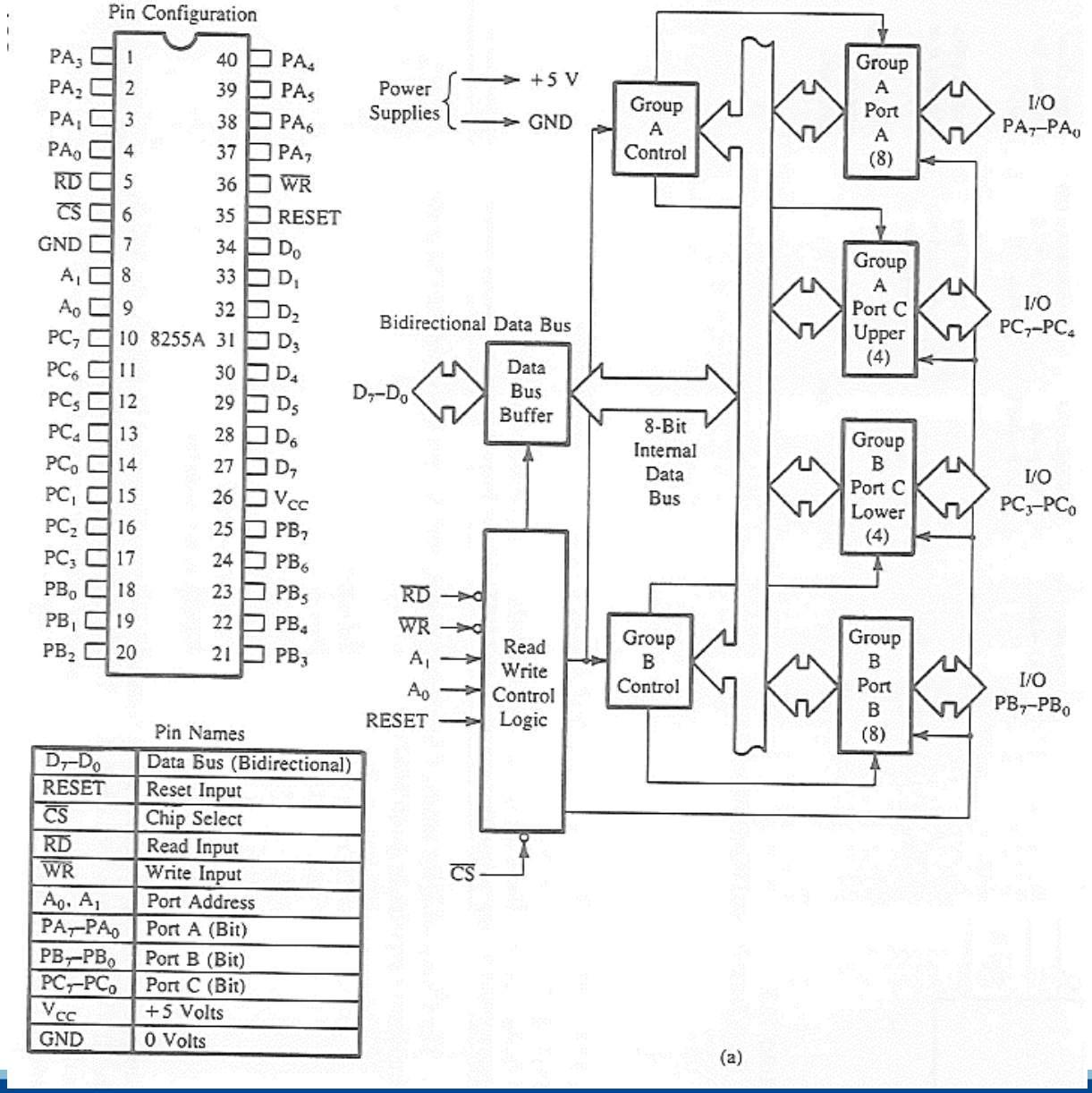
• To understand the programmable peripheral interface.

8255 - Programmable Peripheral Interface (PPI)

- 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world. We can program it according to the given condition. It can be used with almost any microprocessor.

- It consists of three 8-bit bidirectional I/O ports i.e. PORT A, PORT B and PORT C. We can assign different ports as input or output functions

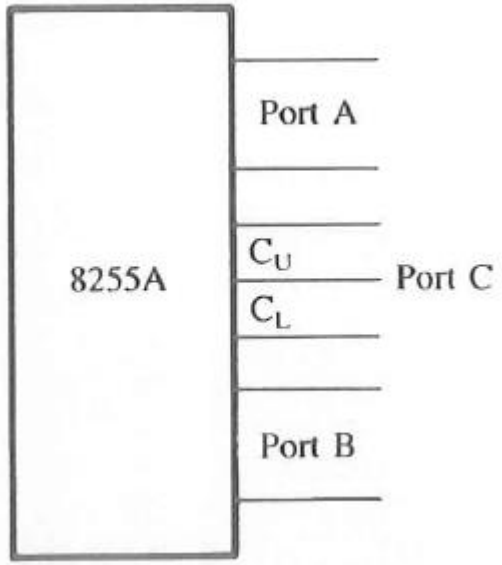
8255 – Block diagram



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

8255 - Programmable Peripheral Interface (PPI)



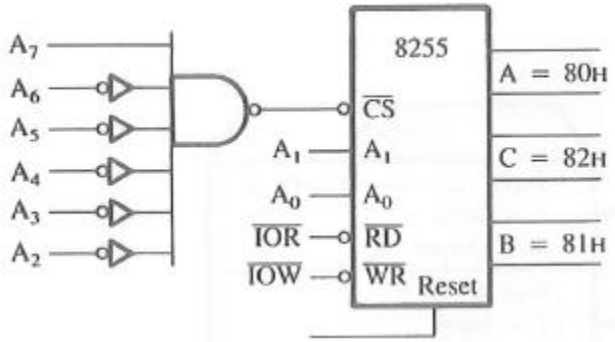
Group A

Port A + CU

Group B

Port B + CL

$\overline{CS}$	A1	A0	Selects:
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control register
1	x	x	8255 is not selected



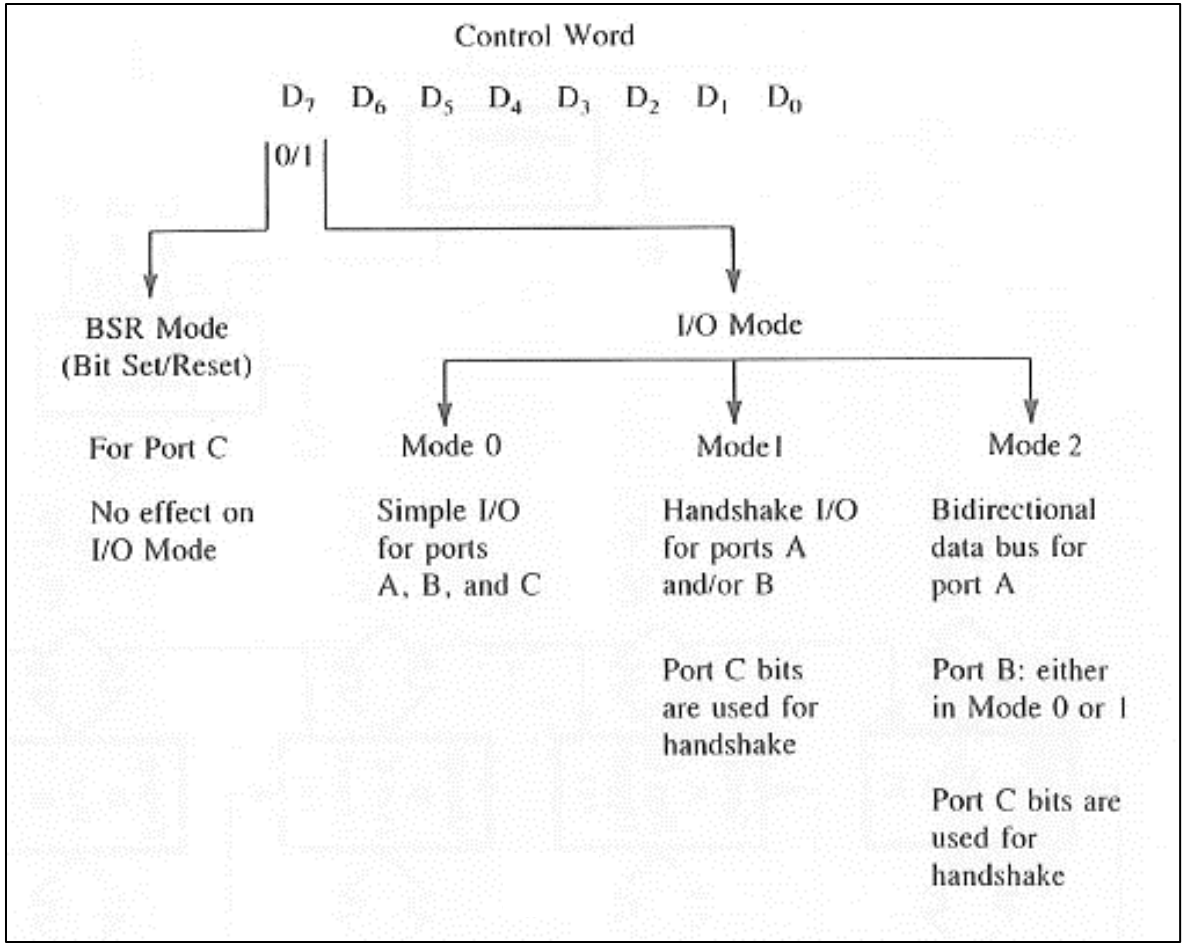
$\overline{CS}$		Hex Address	Port
A_7 A_6 A_5 A_4 A_3 A_2	A_1 A_0		
1 0 0 0 0 0	0 0	= 80H	A
	0 1	= 81H	B
	1 0	= 82H	C
	1 1	= 83H	Control Register

8255 – Modes and control word

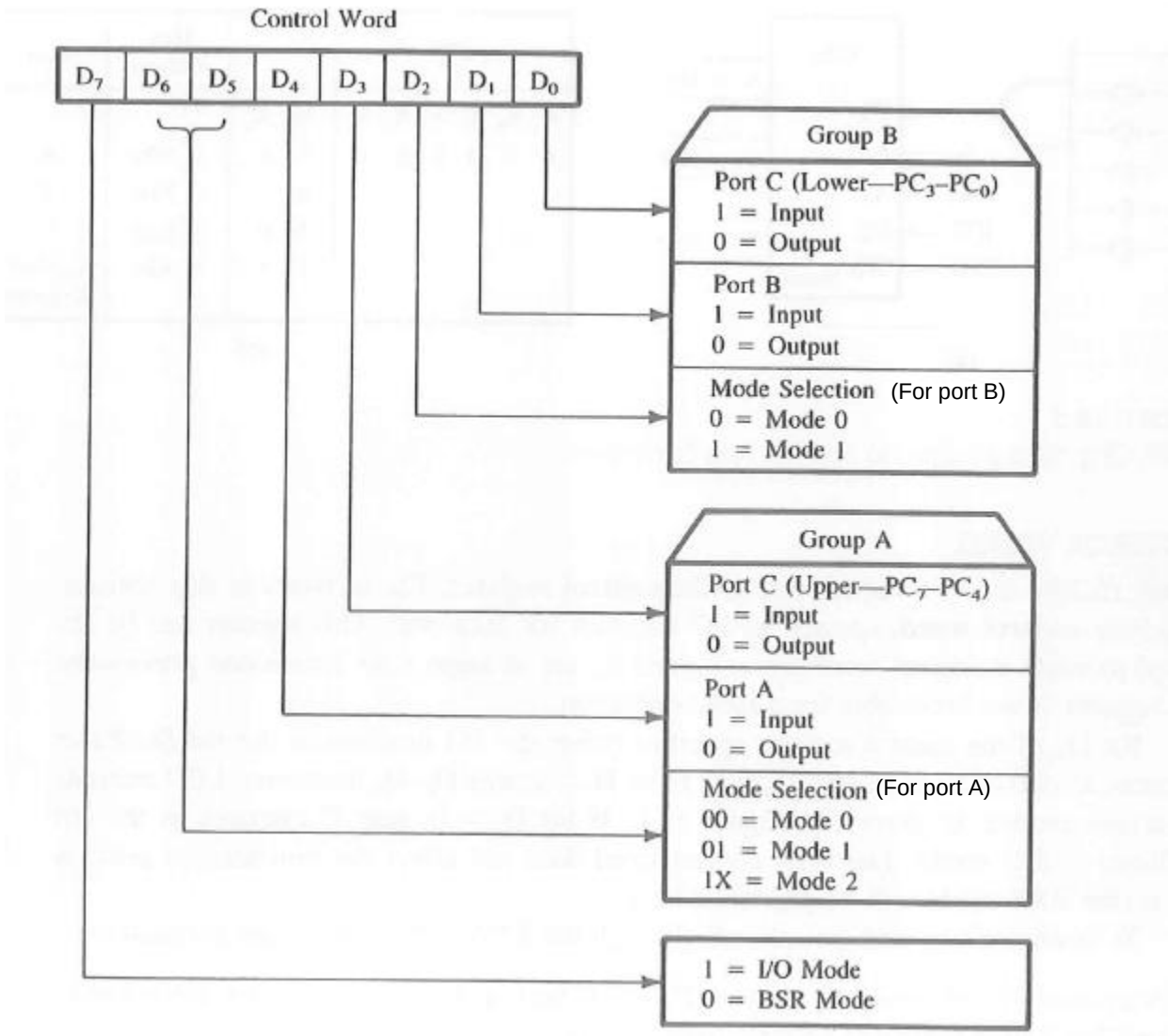
2 Modes

- BSR mode (Bit Set/Reset mode)
- I/O mode

- Control register controls the overall operation of 8255.
- Content of this register, called "**control word**", specifies the operations



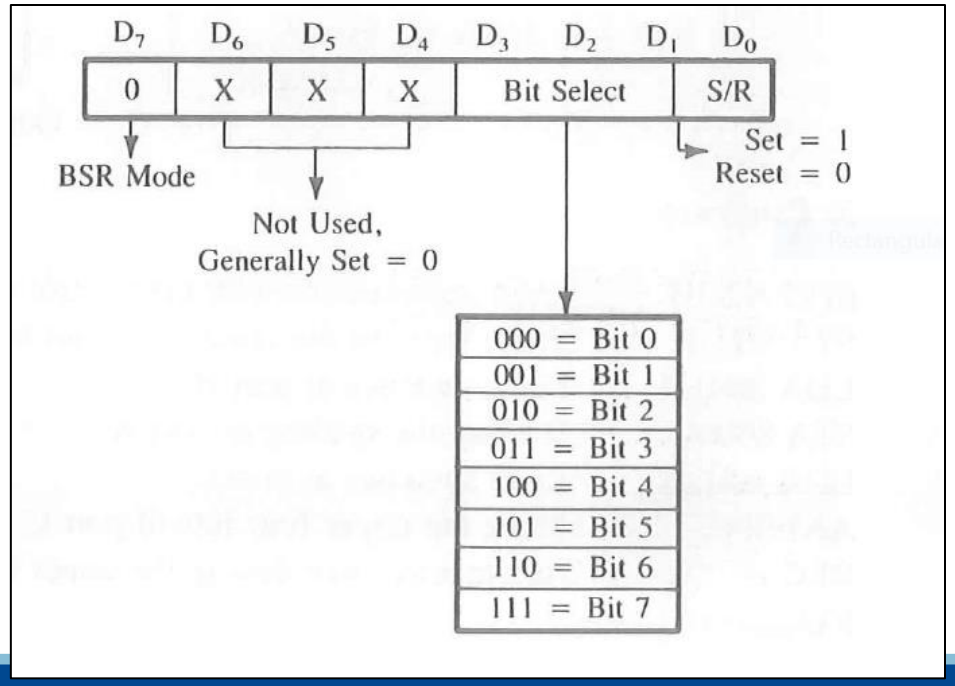
8255 – Control word format for I/O mode



8255 – BSR mode

The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register. A control word with bit $D_7 = 0$ is recognized as a BSR control word, and it does not alter any previously transmitted control word with bit $D_7 = 1$; thus the I/O operations of ports A and B are not affected by a BSR control word. In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

BSR mode control word



BSR CONTROL WORDS

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
To set bit PC_7	0	0	0	0	1	1	1	1	=	0FH
To reset bit PC_7	0	0	0	0	1	1	1	0	=	0EH
To set bit PC_3	0	0	0	0	0	1	1	1	=	07H
To reset bit PC_3	0	0	0	0	0	1	1	0	=	06H

1. To set/reset bits in port C, a control word is written in the control register and not in port C.
2. A BSR control word affects only one bit in port C.
3. The BSR control word does not affect the I/O mode.

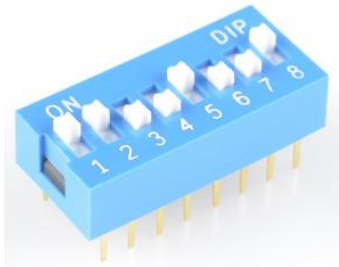
Instructions for setting PC7
MOV AL, 0F
OUT 83, AL

8255 – I/O Mode – Mode 0

- In this mode, ports **A**, **B** are used as **two simple 8-bit I/O** ports & port **C** as **two independent 4-bit ports**.
- **Each port** can be programmed to function as simply an input port or an output port.
- The **input/output features** in Mode 0 are as follows.
    1. Outputs are latched.
    2. Inputs are not latched.
    3. Ports don’t have handshake or interrupt capability

8255 – I/O MODE – Mode 0 example

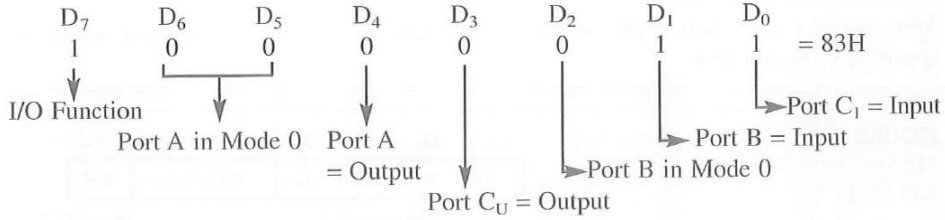
Write a program to read the DIP switches and display the reading from port B at port A and from port C_L at port C_U. (Use memory mapped I/O).

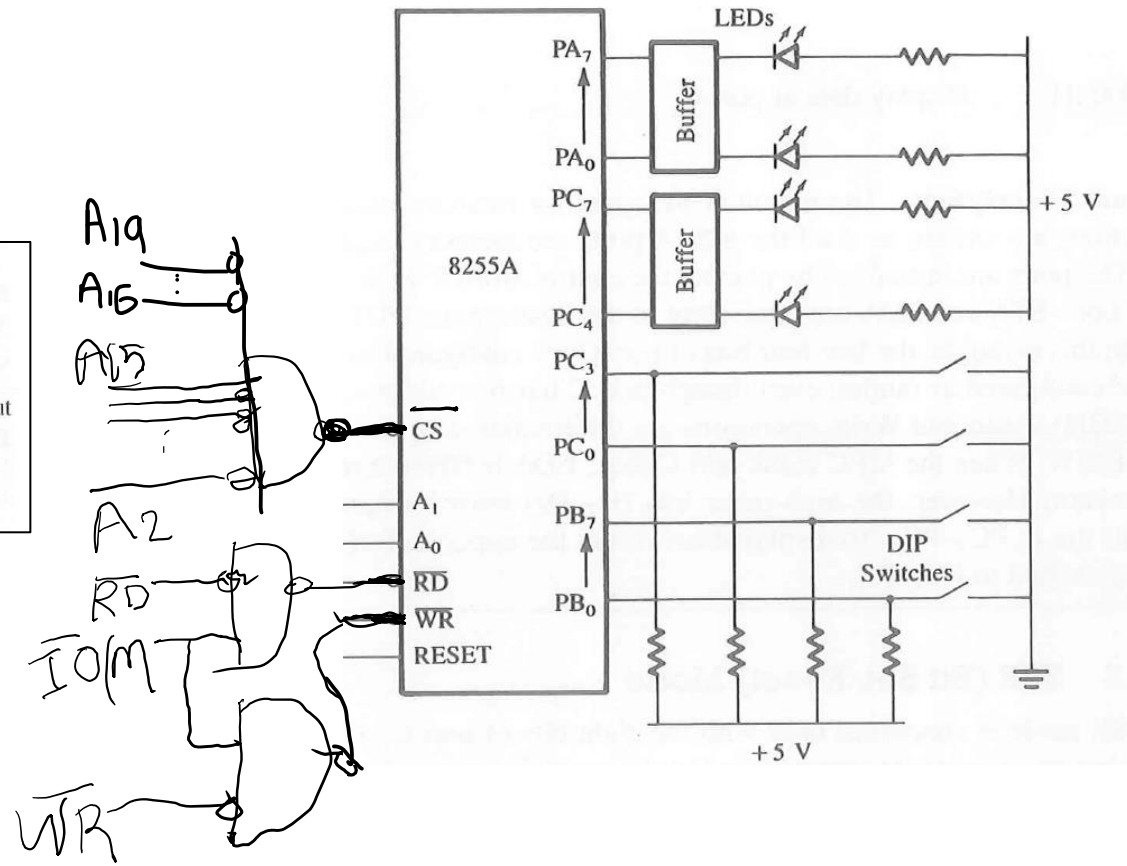


1. Port addresses:

Port A	=	08000H ($A_1 = 0, A_0 = 0$)
Port B	=	08001H ($A_1 = 0, A_0 = 1$)
Port C	=	08002H ($A_1 = 1, A_0 = 0$)
Control Register	=	08003H ($A_1 = 1, A_0 = 1$)

2. Control Word






```
MOV AL,83
MOV [8003],AL

MOV AL,[8001]
MOV [8000],AL

MOV AL,[8002]
AND AL,0F
MOV CL, 04
ROL AL,CL
MOV [8002],AL
```

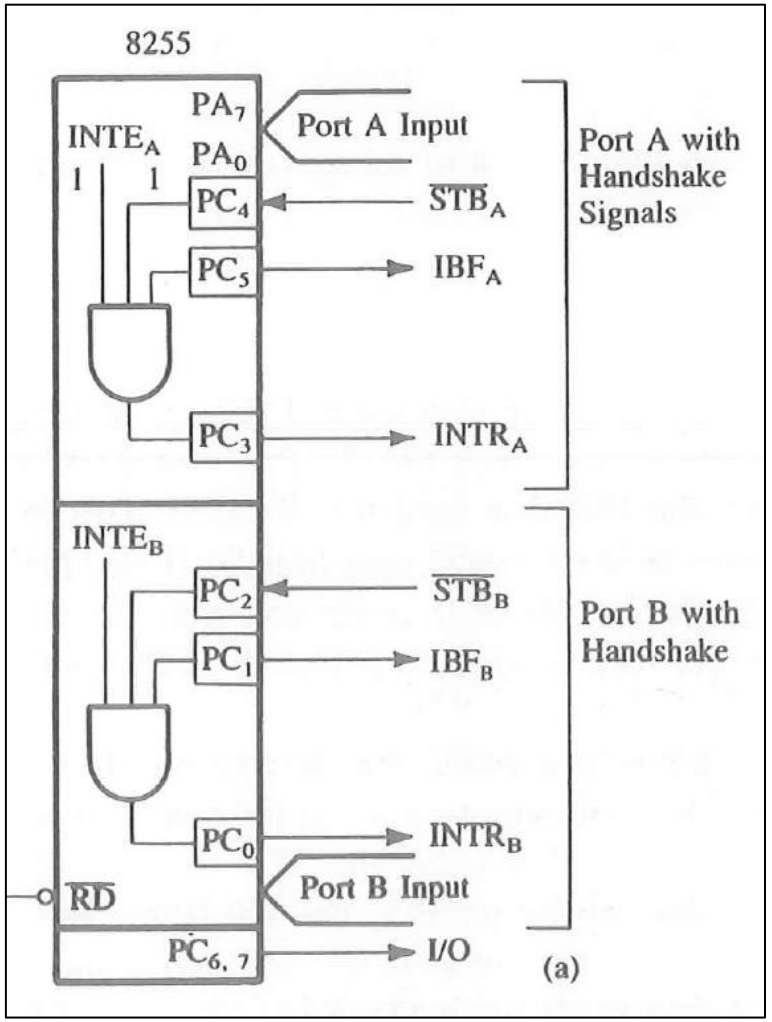
8255 – I/O Mode – Mode 1

In this mode, **handshake signals are exchanged** prior to data transfer.

The **features** of the mode include the following:

1. Two ports (**A** and **B**) function as 8-bit I/O ports.
   They can be configured as either as input or output ports.
2. Each port uses **three lines from port C as handshake signals**.
   The remaining two lines of Port C can be used for simple I/O operations.
3. Input and Output data are latched.
4. Interrupt logic is supported.

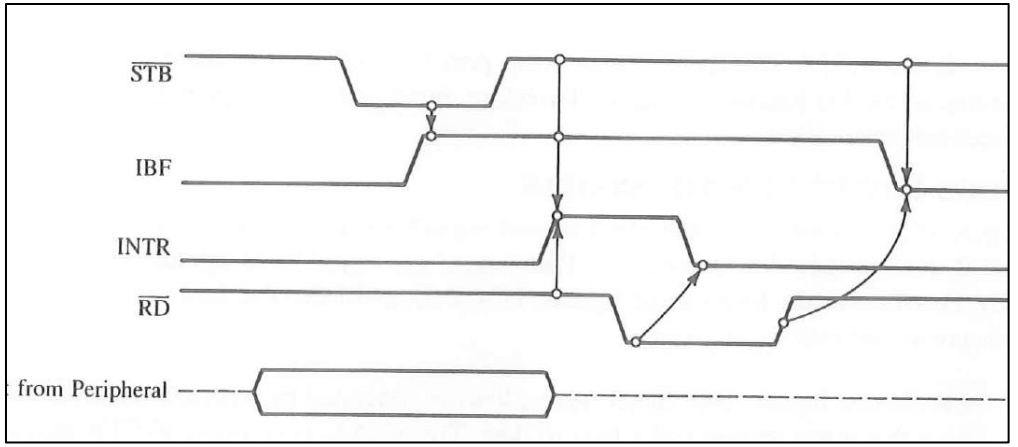
8255 – I/O Mode – Mode 1 – Input control signals

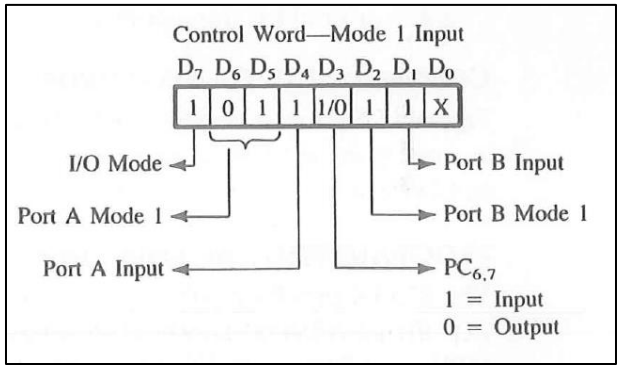


- $\overline{STB}$ (Strobe Input): This signal (active low) is generated by a peripheral device to indicate that it has transmitted a byte of data. The 8255A, in response to $\overline{STB}$, generates IBF and INTR, as shown in Figure ____.
- **IBF (Input Buffer Full):** This signal is an acknowledgment by the 8255A to indicate that the input latch has received the data byte. This is reset when the MPU reads the data
- **INTR (Interrupt Request):** This is an output signal that may be used to interrupt the MPU. This signal is generated if $\overline{STB}$, IBF, and INTE (Internal flip-flop) are all at logic 1. This is reset by the falling edge of the $\overline{RD}$ signal
- **INTE (Interrupt Enable):** This is an internal flip-flop used to enable or disable the generation of the INTR signal. The two flip-flops $INTE_A$ and $INTE_B$ are set/reset using the BSR mode. The $INTE_A$ is enabled or disabled through PC_4, and $INTE_B$ is enabled or disabled through PC_2.

Status Word—Mode 1 Input

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$





8255 – I/O Mode – Mode 1 – Programming

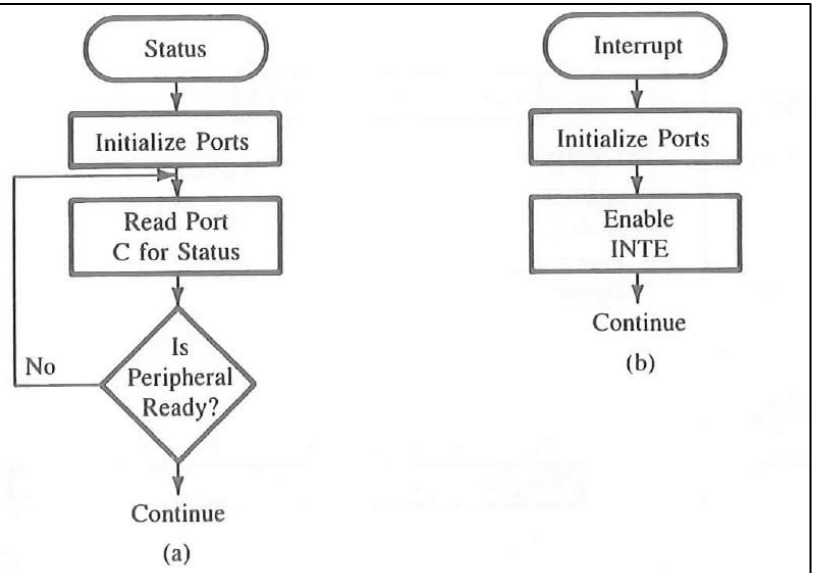
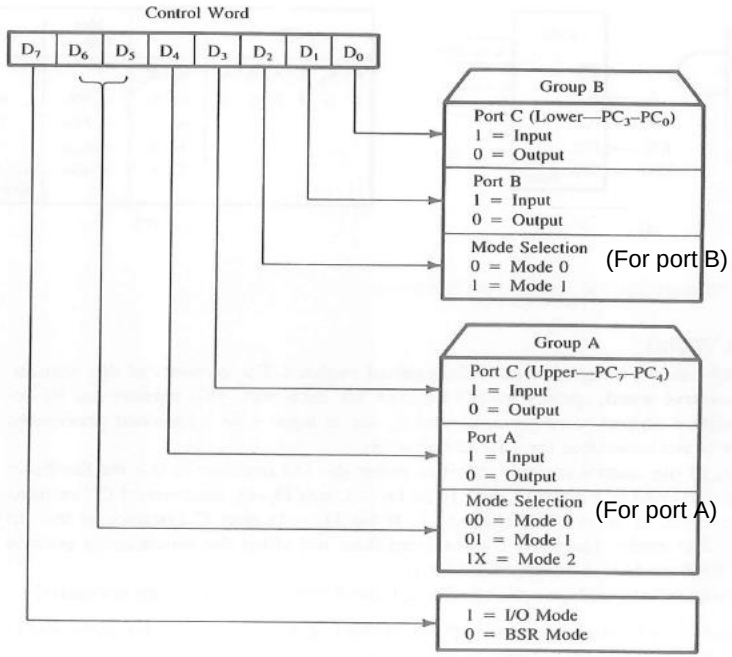


FIGURE 15.10
Flowcharts: Status Check I/O (a) and Interrupt I/O (b)



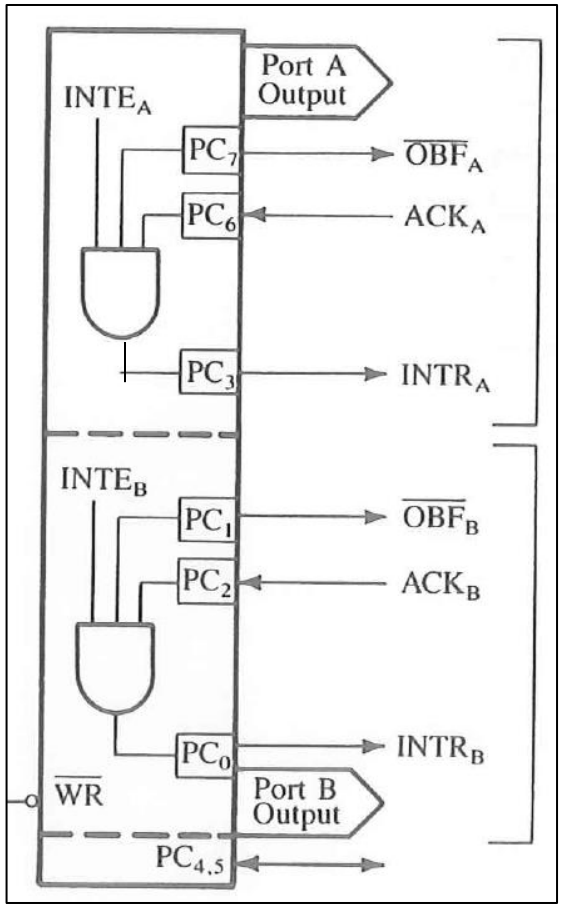
Status Word—Mode 1 Input

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$

Eg: Read the input device connected in port A and display the data in port B. Configure port A in mode 1 and use status check I/O to communicate. Assume control register address=C6, port A address = C0, port B address = C2, port C address = C4

```
        MOV AL, B4
        OUT C6, AL
READ:   IN AL, C4
        AND AL, 20
        JZ READ
        IN AL,C0
        OUT C2,AL
        HLT
```

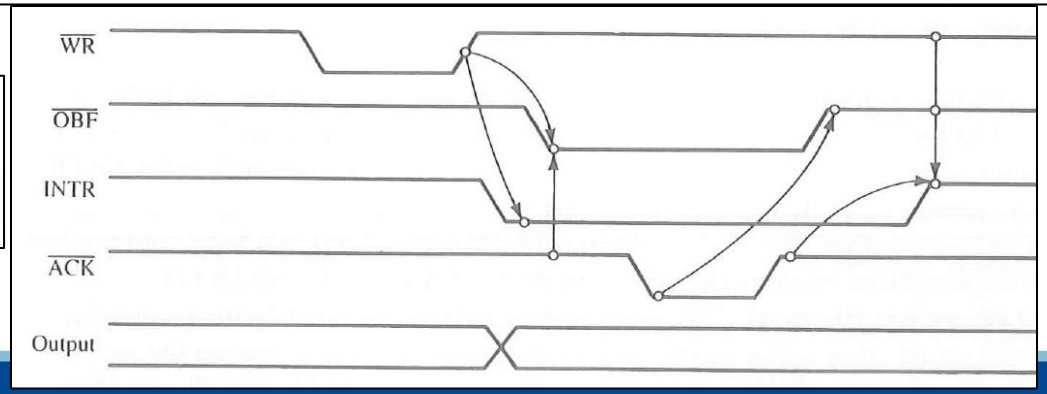
8255 – I/O Mode – Mode 1 – Output control signals

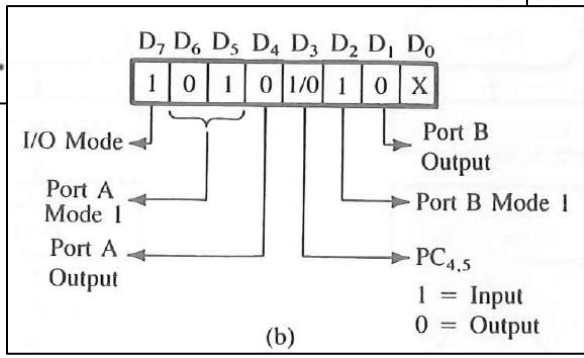


- **$\overline{OBF}$ (Output Buffer Full):** This is an output signal that goes low when the MPU writes data into the output latch of the 8255A. This signal indicates to an output peripheral that new data are ready to be read (Figure). It goes high again after the 8255A receives an $\overline{ACK}$ from the peripheral.
- **$\overline{ACK}$ (Acknowledge):** This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255A ports (Figure).
- **INTR (Interrupt Request):** This is an output signal, and it is set by the rising edge of the $\overline{ACK}$ signal. This signal can be used to interrupt the MPU to request the next data byte for output. The INTR is set when $\overline{OBF}$, $\overline{ACK}$, and INTE are all one (Figure) and reset by the falling edge of $\overline{WR}$.
- **INTE (Interrupt Enable):** This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTE$_A$ and INTE$_B$ are controlled by bits PC$_6$ and PC$_2$, respectively, through the BSR mode.
- **PC$_{4,5}$:** These two lines can be set up either as input or output.

Status Word

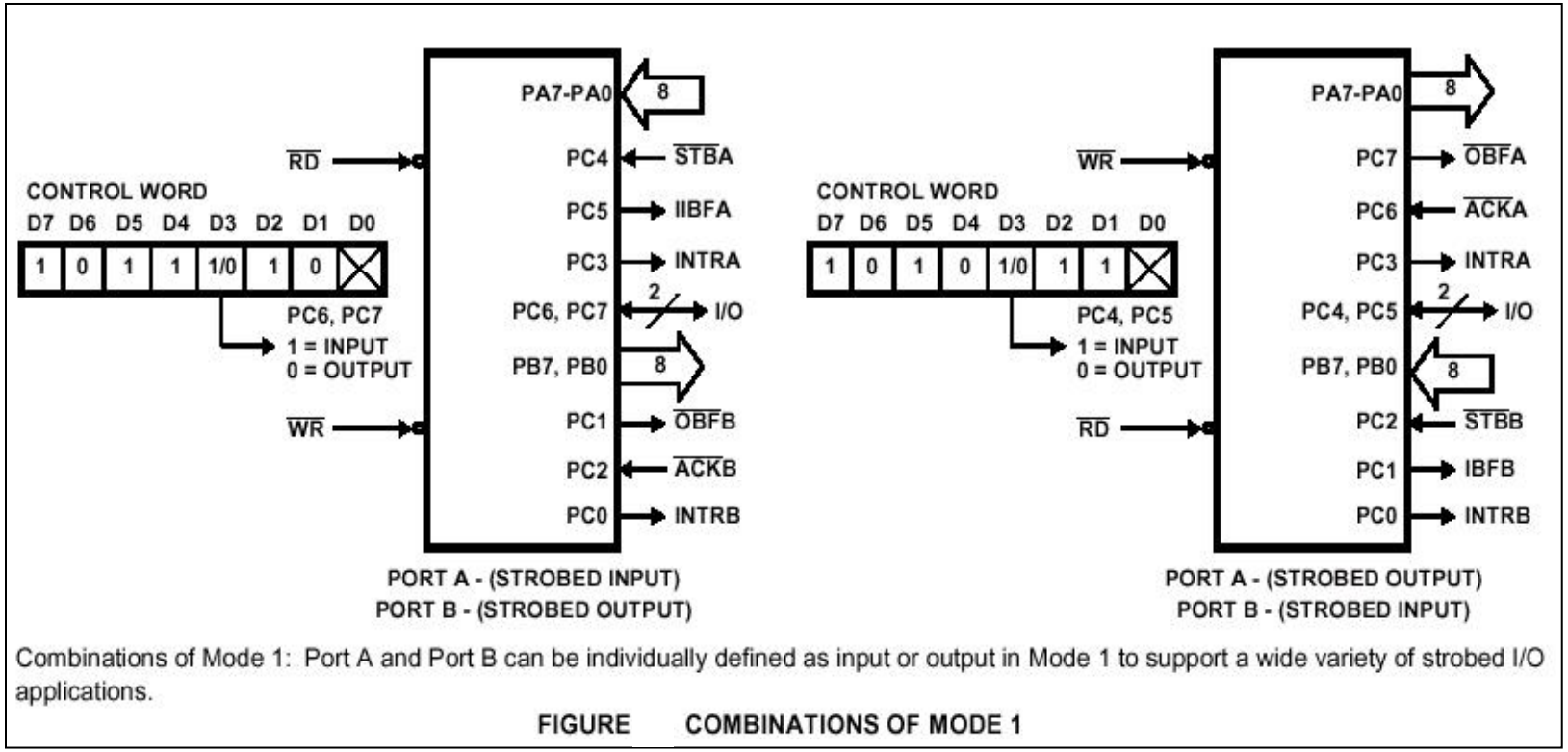
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	INTE$_A$	I/O	I/O	INTR$_A$	INTE$_B$	$\overline{OBF}_B$	INTR$_B$





Control word

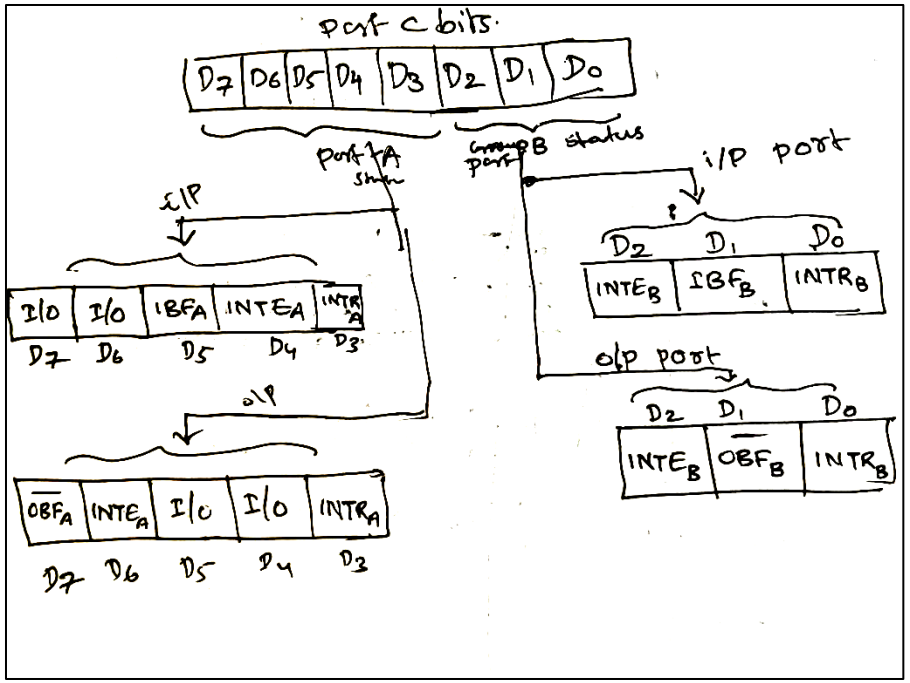
8255 – I/O Mode – Mode 1 – Input /Output combination



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE COMBINATIONS OF MODE 1

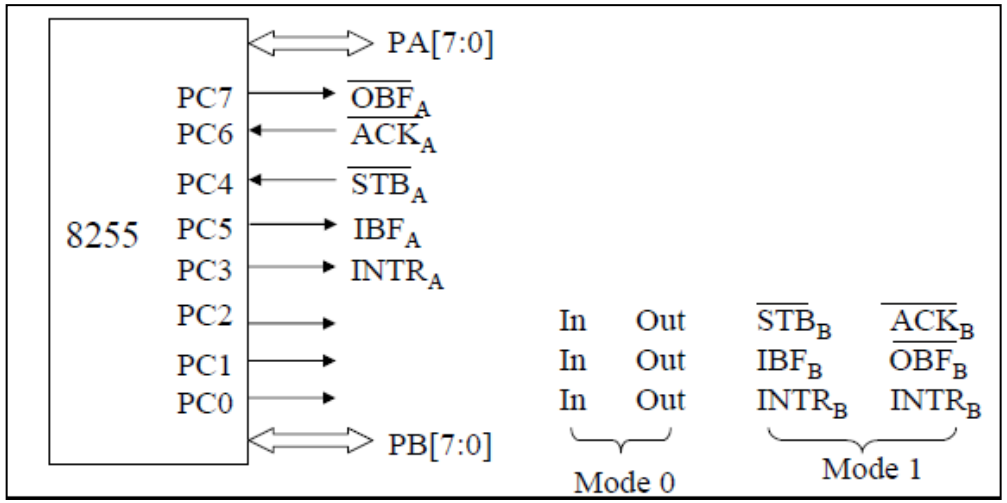
Status word

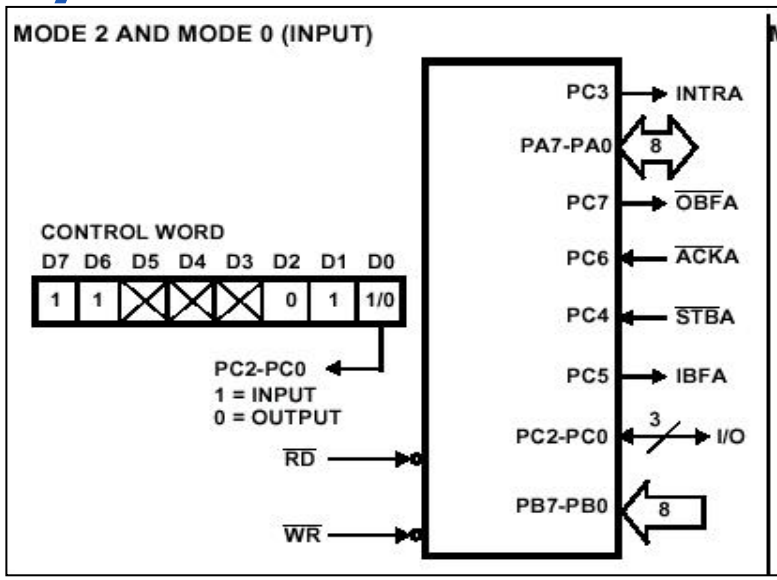


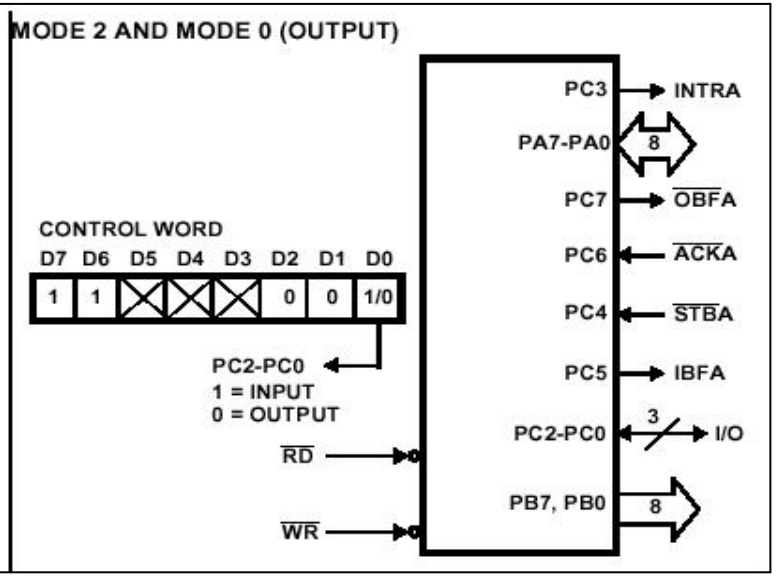
8255 – I/O Mode – Mode 2

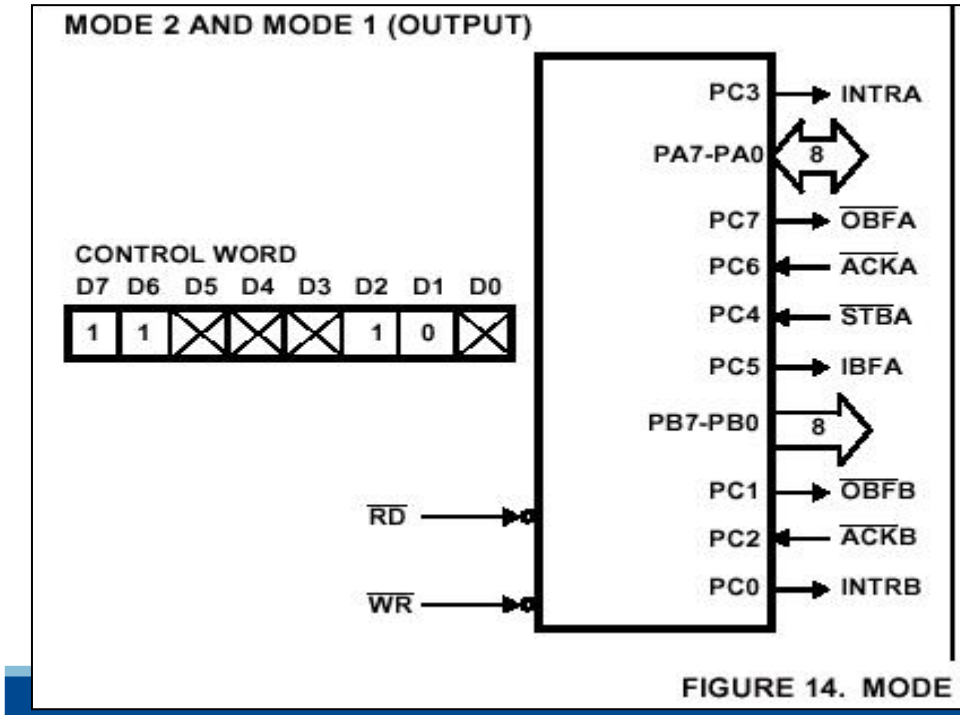
- This mode is used primarily in applications such as **data transfer between two computers.**
- In this mode, **Port A** can be configured as the bidirectional port, **Port B** either in Mode 0 or Mode 1.
- **Port A uses five signals from Port C as handshake signals for data transfer.**
- The remaining three signals from **Port C** can be used either as simple I/O or as handshake for port B.

8255 – I/O Mode – Mode 2









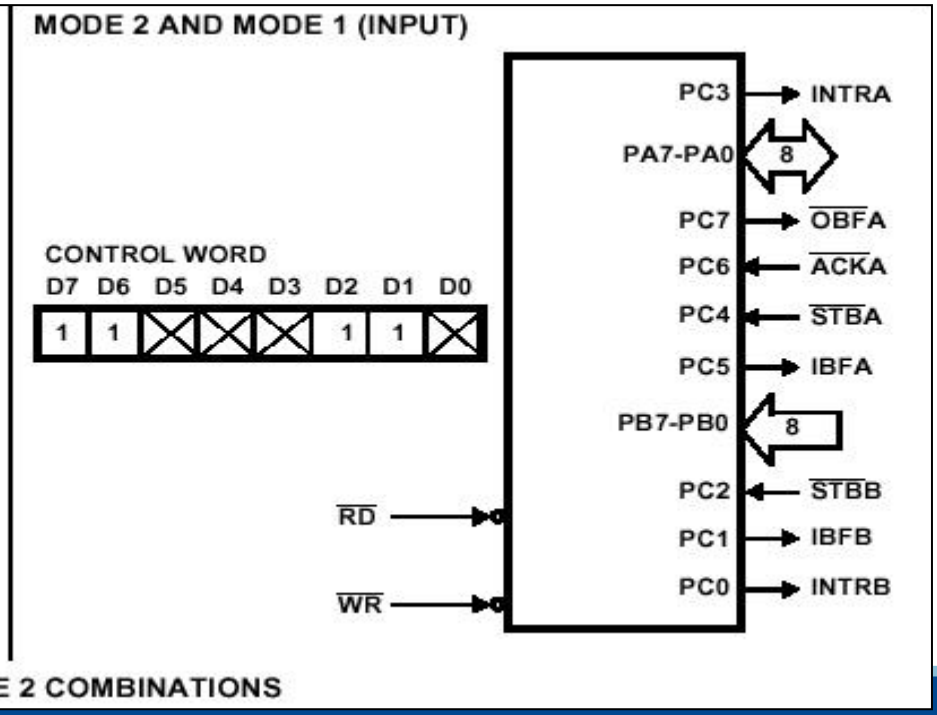


FIGURE 14. MODE 2 COMBINATIONS

References

- Doughlas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH.
- 8255 Intel data sheet
- Microprocessor Architecture, Programming, and Applications with the 8085, 5th edition, Ramesh Gaonkar.

Thank you