COURSE: UCS1502 - MICROPROCESSORS AND INTERFACING

Minimum and maximum mode configurations with system bus timings

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This presentation covers

- Details of minimum and maximum modes

Learning Outcome of this module

- To understand about minimum and maximum mode configurations and its timings

Minimum mode

- **If MN/$\overline{\text{MX}}$ pin = 1**, 8086 works in minimum mode.
- In this mode, all the control signals are given out by 8086 itself.
- It is a single processor mode
- The remaining components in the system are latches, transceivers, clock generator, memory and I/O devices. Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.
- Latches are generally ‘buffered output D-type flip-flops’ like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.
- Transceivers are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals. They are controlled by two signals namely, $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$.
- Usually, EPROM is used for monitor program storage, while RAM for users program storage.

Minimum mode

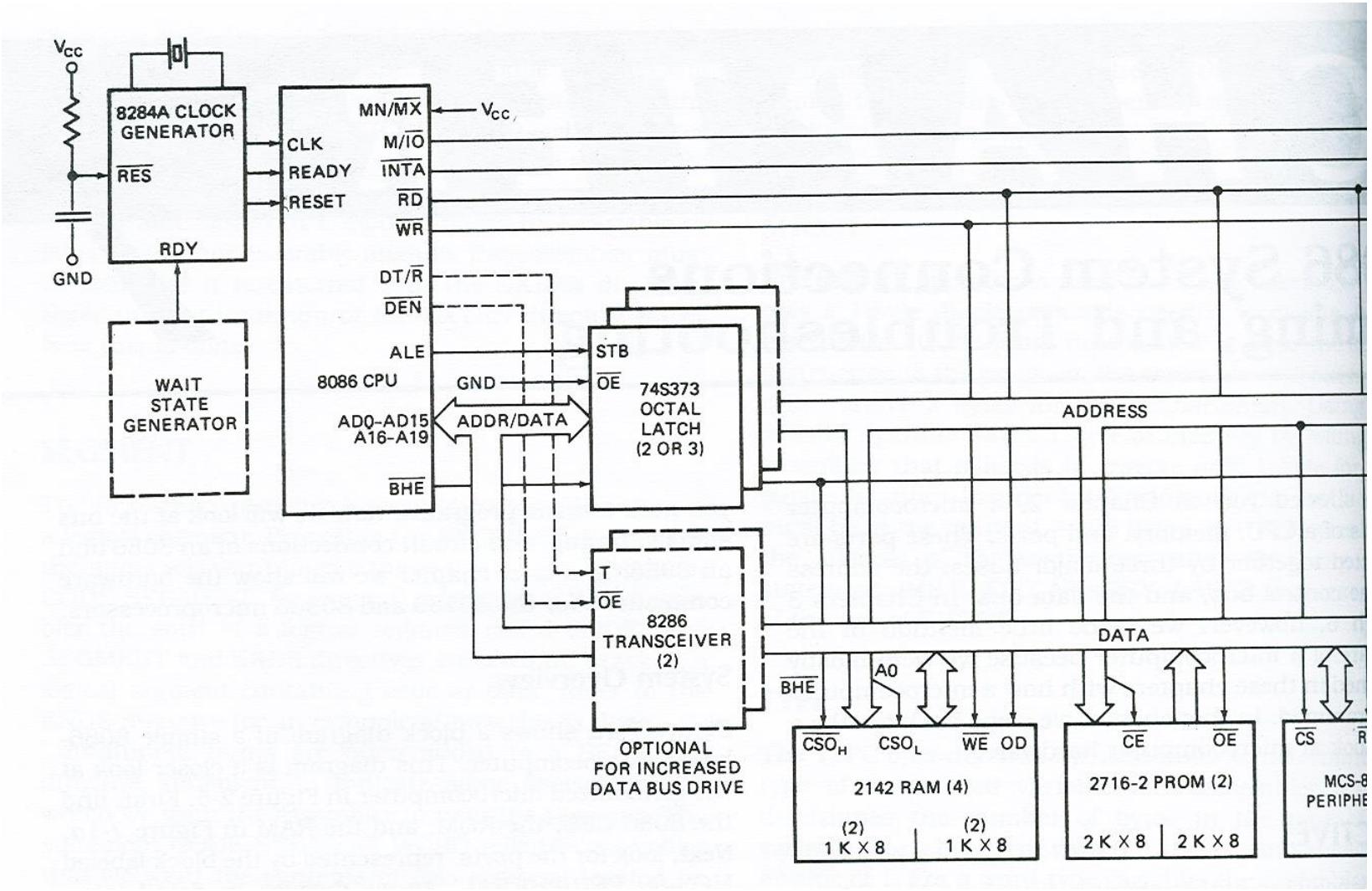
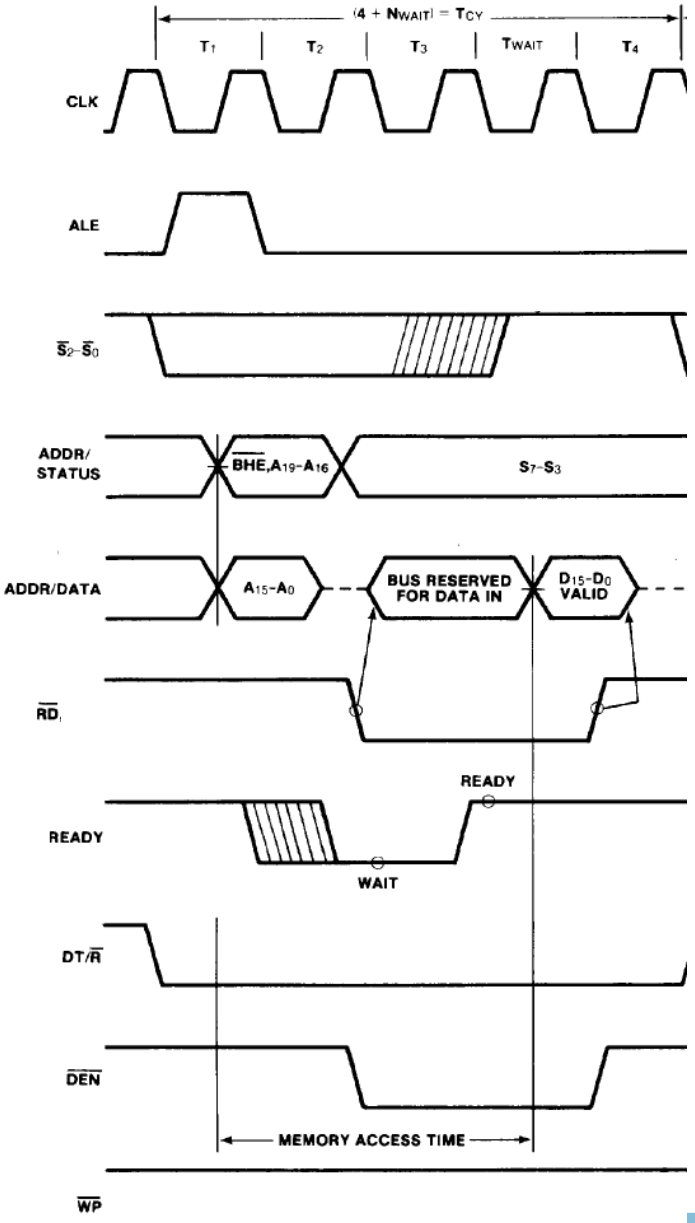
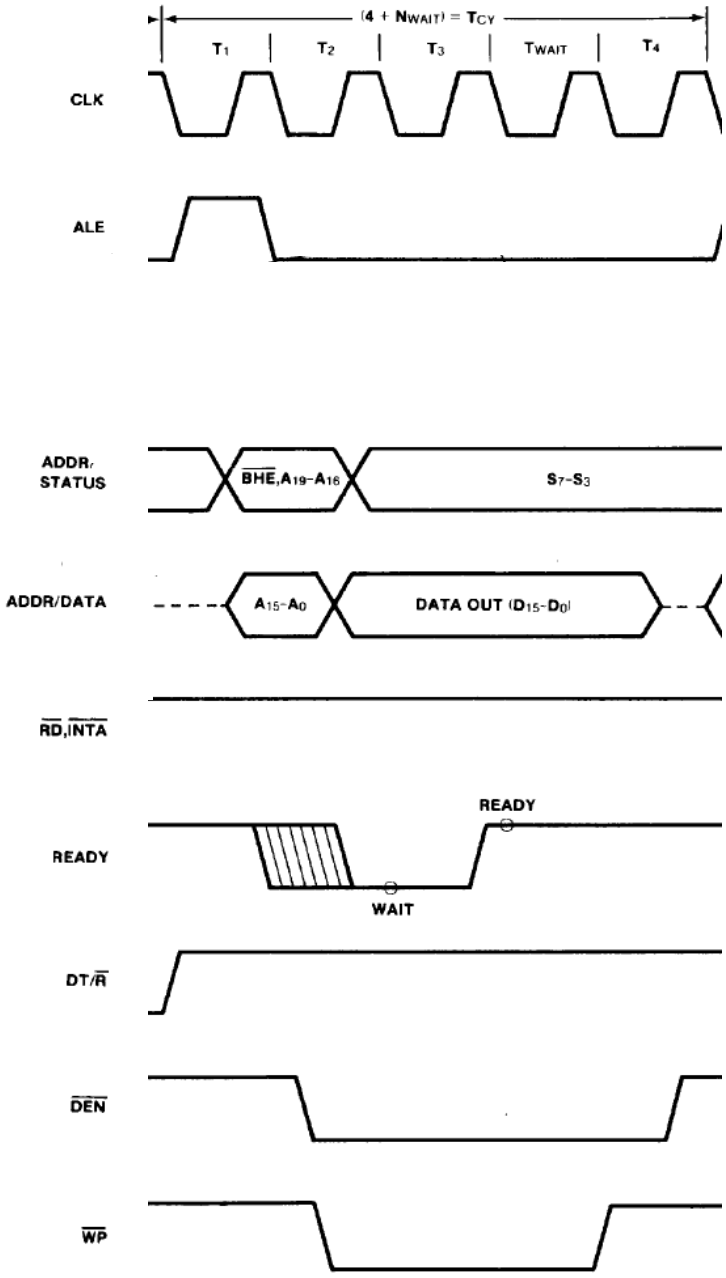


Fig: Minimum mode 8086 typical configuration

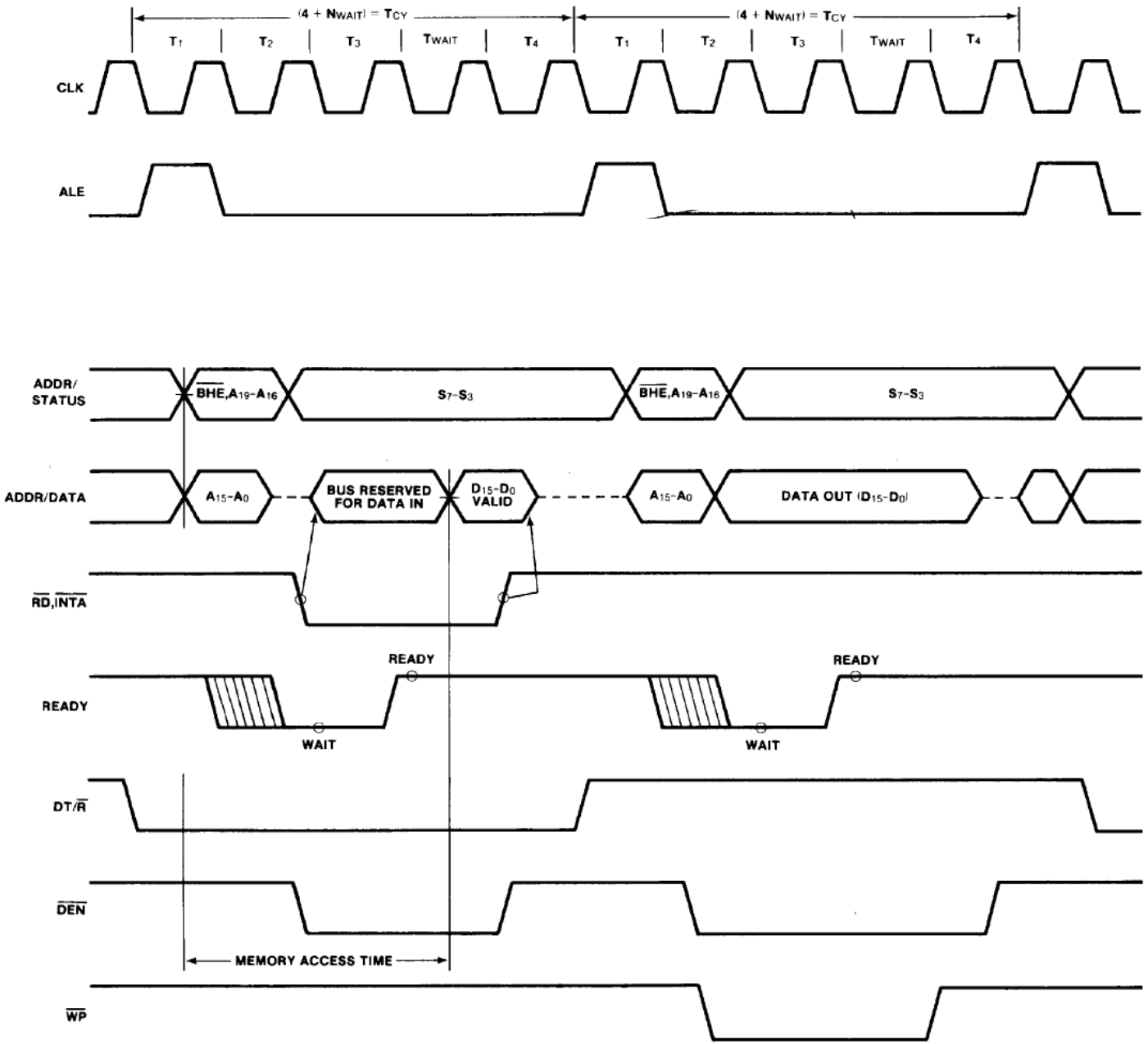
Minimum mode – Memory read timing



Minimum mode – Memory write timing



Minimum mode : Memory read and write timings



Maximum mode

- **If MN/$\overline{\mathbf{MX}}$ pin = 0**, 8086 works in maximum mode.
- In this mode, the processor generates the status signals $\overline{\mathbf{S2}}$,$\overline{\mathbf{S1}}$ and $\overline{\mathbf{S0}}$. Another chip called bus controller (8288) derives the control signals using this status information.
- In the maximum mode, there may be more than one microprocessor in the system configuration.

Maximum mode

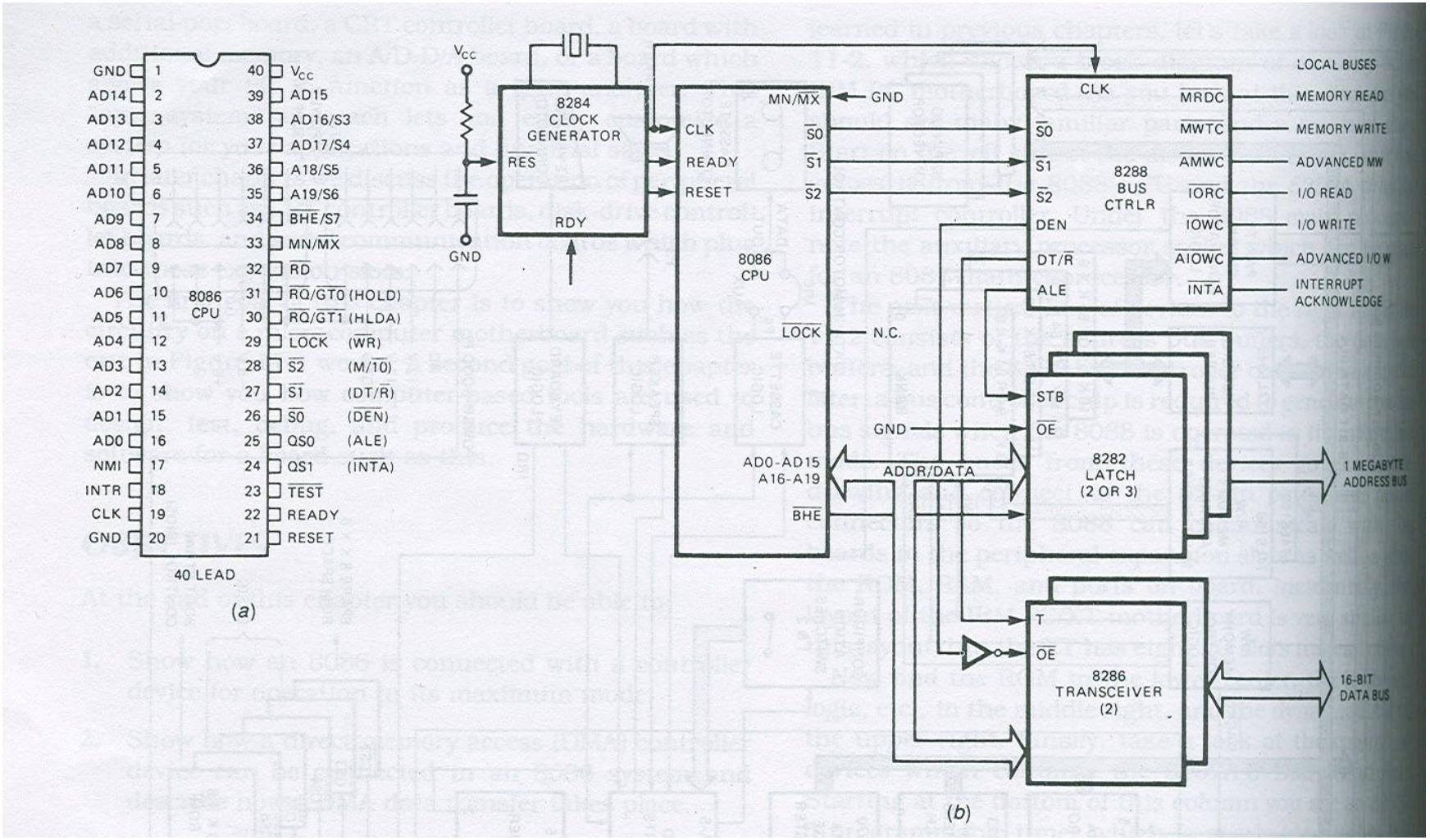


Fig: Maximum mode configuration

Maximum mode

- 8288 bus controller generates $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{MRDC}$ (memory and I/O read/write control/command signals - all are active low signals), $\overline{INTA}$, DEN, ALE and DT/$\overline{\mathbf{R}}$.

- $\overline{AIOWC}$, $\overline{AMWC}$ - These signals are activated one clock cycle earlier than normal write signals.

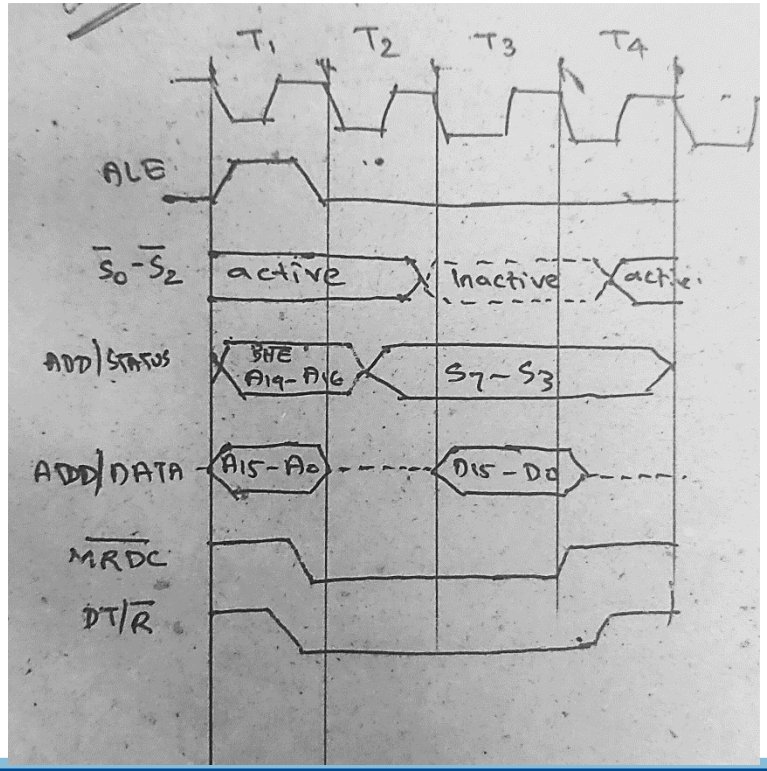


Fig: Timing diagram of maximum mode memory read cycle

References

- Doughlas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH.

Thank you