COURSE: UCS1502 - MICROPROCESSORS AND INTERFACING

Pin details of 8086 and memory organization of 8086 based system

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This presentation covers

- The pin details of 8086 and memory organization

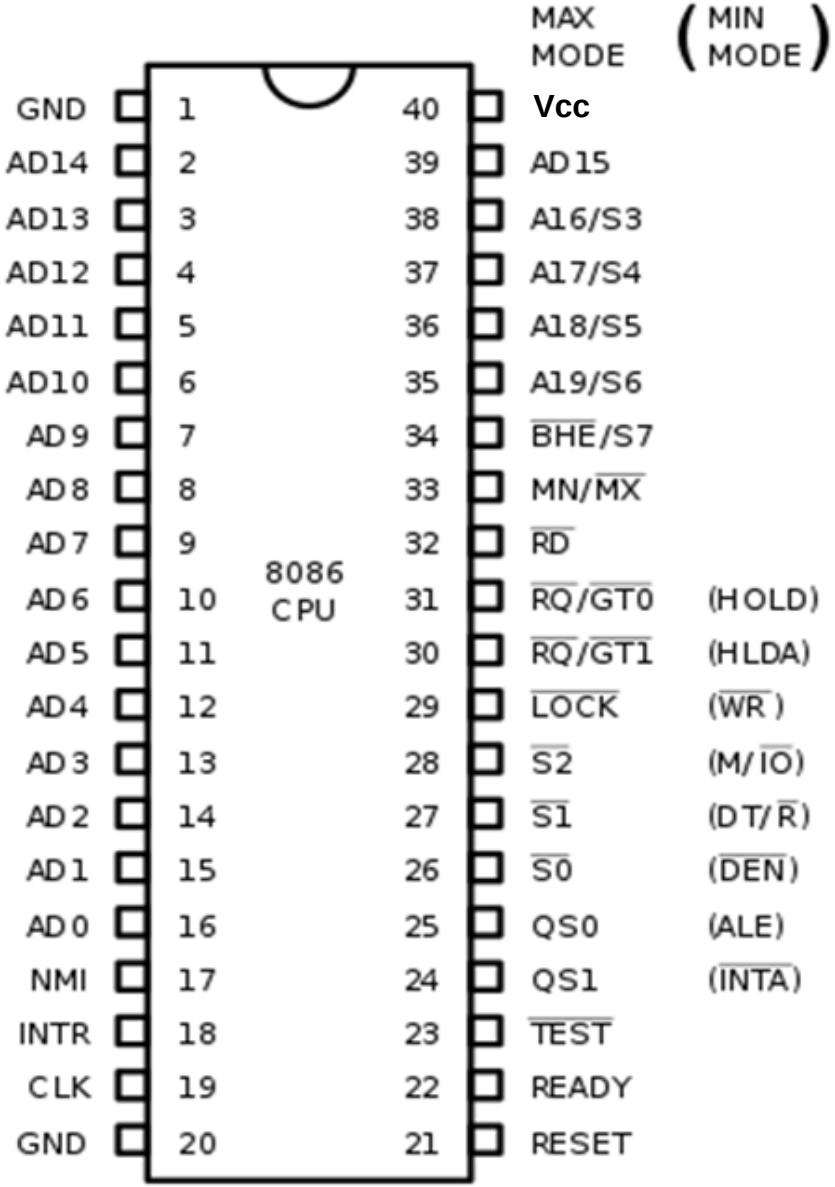
Learning Outcome of this module

- To understand various pins of 8086 and its memory organization

Do you know ??

- What are the modes of operations in 8086 and related pins ?
- What are the multiplexed pins in 8086 ?
- How the memory is organized to reduce the access latency?
- Differences between 8086 and 8088.

Pin details of 8086



2 modes of operations

- **Minimum mode** **(if the input pin 33=1)**
  - Single processor mode
  - All control signals will be generated by 8086 itself.
- **Maximum mode** **(if the input pin 33=0)**
  - Multi-processor mode.
  - External bus controller (8288) generates the control signals according to the signals from pins $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$.

Pin no. 24-31 will have different functions based on this modes.

Pin details of 8086

- **Vcc**: (i*) 5V DC supply
- **GND**: (i) 2 ground pins
- **AD15 – AD0 :**(b*) Multiplexed address/data bus.

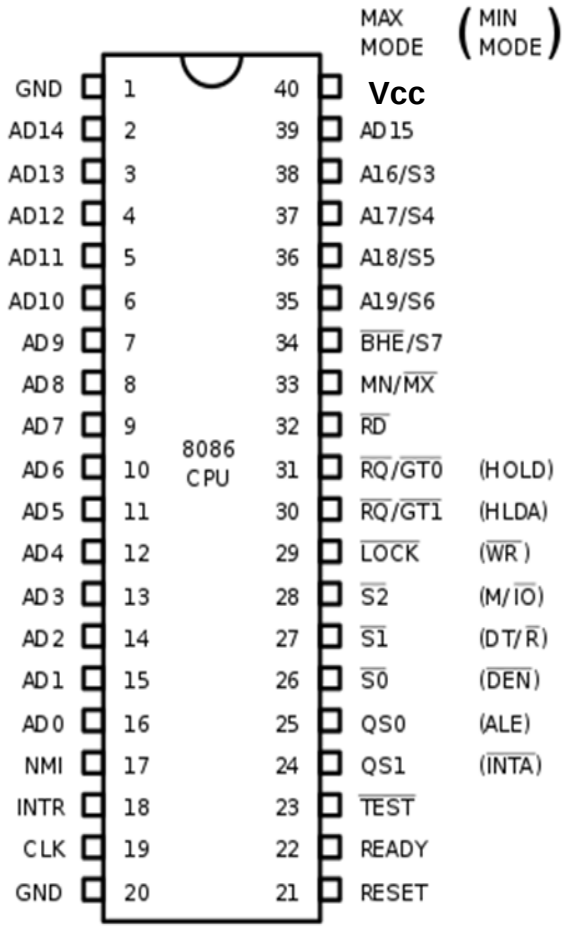
  During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data.
- **A16-A19/S3-S6**: (o*)

  These are the 4 address/status buses. During the first clock cycle, it carries 4-bit address and later it carries status signals. During T2, T3, Tw and T4 ⇨ status

  S5: status of IE flag bit.

  S4, S3: info about currently which segment is being used.

  S6: always low.

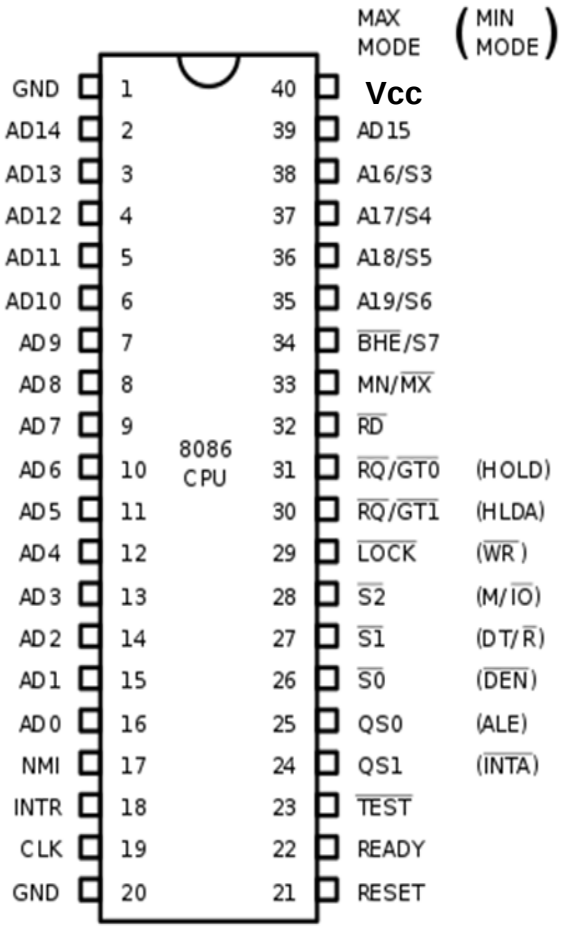


S4	S3	
0	0	Alternate data (Extra segment)
0	1	Stack segment
1	0	Code or none
1	1	Data segment

i represents input pin*
o represents output pin*
b represents bi-directional*

Pin details of 8086

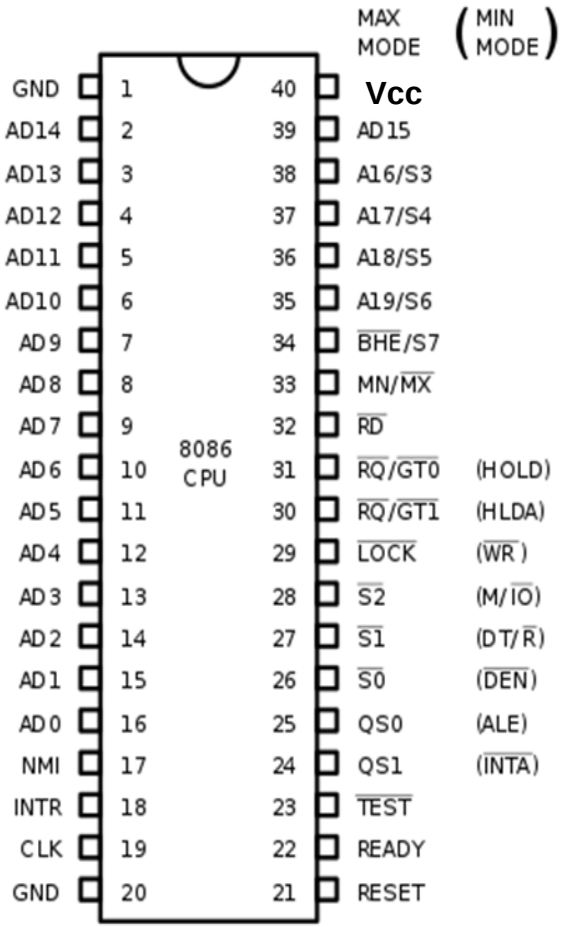
- **$\overline{\text{BHE}}$/S7** : (o) BHE stands for Bus High Enable. It is used to indicate the transfer of data using data bus D8-D15. S7 is always 1.
- **$\overline{\text{RD}}$:** (o) indicates the memory/IO read operation.
- **READY:** (i) It is an acknowledgement signal from I/O devices to indicate the completion of data transfer. If ready is low before the rising edge of T2, 8086 will insert wait states between T3 and T4.
- **INTR**: (i) Maskable interrupt request (level triggered)
- **$\overline{\text{TEST}}$** : (i) This pin is examined by WAIT instruction. If it is 1, 8086 will wait until it become 0.
- **NMI:** (i) Non Maskable Interrupt.
- **RESET**: (i)If it is 1, 8086 terminates current activity and starts executions from FFFF0. It must be 1 for at least 4 clock cycles to detect as a valid reset.
- **CLK**: (i) clock input
- **MN/$\overline{\text{MX}}$:** (i) If it is 1, 8086 works in minimum mode. If 0, works in maximum mode.



Pin details of 8086

Minimum mode signals

- **M/$\overline{\text{IO}}$** : (o) This signal is used to distinguish between memory and I/O operations. If it is high -> memory operation, else IO operation.
- **$\overline{\text{INTA}}$:** (o) Interrupt acknowledgement.
- **ALE:** (o) It stands for address latch enable. A high in this pin indicates the availability of a valid address on the address/data lines. It is used to enable external address latches.
- **DT/$\overline{\text{R}}$**: (o) Data Transmit/Receive signal. It indicates the direction of data flow through the transreceiver. When it is high, data is transmitted out from 8086 and vice-a-versa.
- **$\overline{\text{DEN}}$** : (o) Data Enable - This pin indicates the availability of valid data on AD0-AD15. It is used to enable data bus transceiver 8286.
- **HOLD:** (i) Bus request from other devices like DMA.
- **HLDA**: (o) Hold Acknowledgement. This signal acknowledges the HOLD signal..

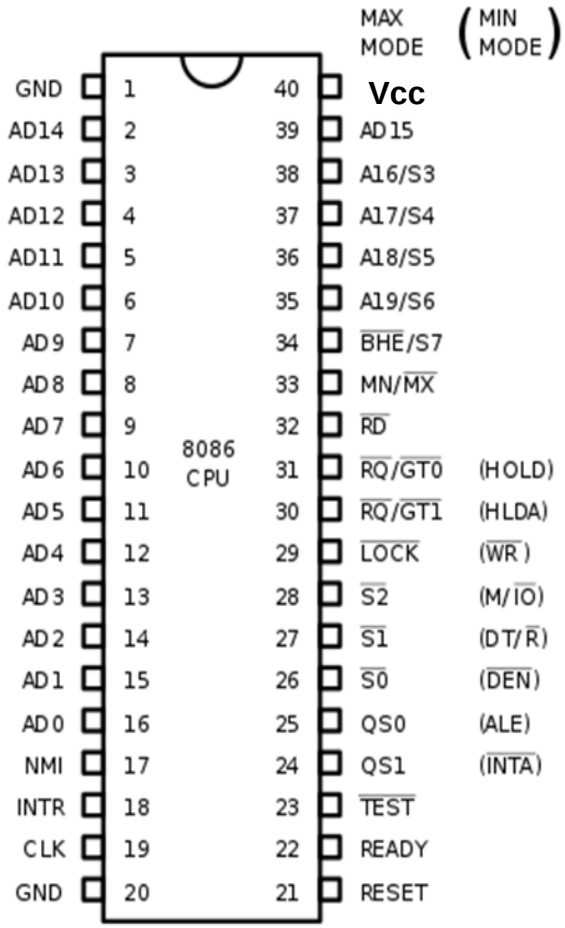


Pin details of 8086

Maximum mode signals

- $\overline{S2}, \overline{S1}$ **and** $\overline{S0}$: (o) These are the status signals that provide the status of operation, which is used by the bus controller 8288 to generate memory & I/O control signals.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Instruction fetch (Code access)
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive (no bus cycle)



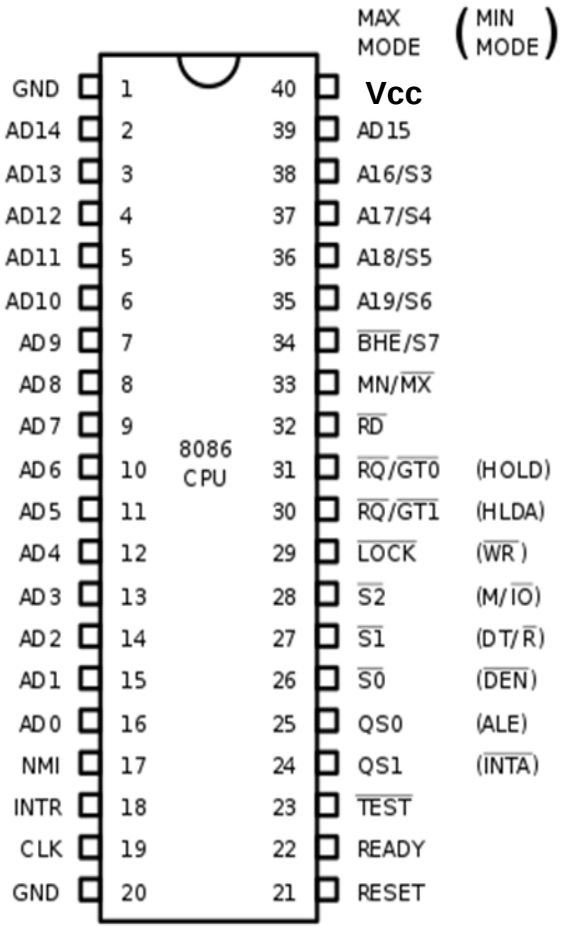
Pin details of 8086

- $\overline{\mathbf{LOCK}}$: (o) if this pin = 0, bus masters will be prevented from gaining the system bus. It is activated using the LOCK prefix on any instruction.

- **QS1, QS0**: (o) These queue status signals provide the status of instruction queue.

QS1	QS0	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty queue
1	1	Subsequent byte from the queue

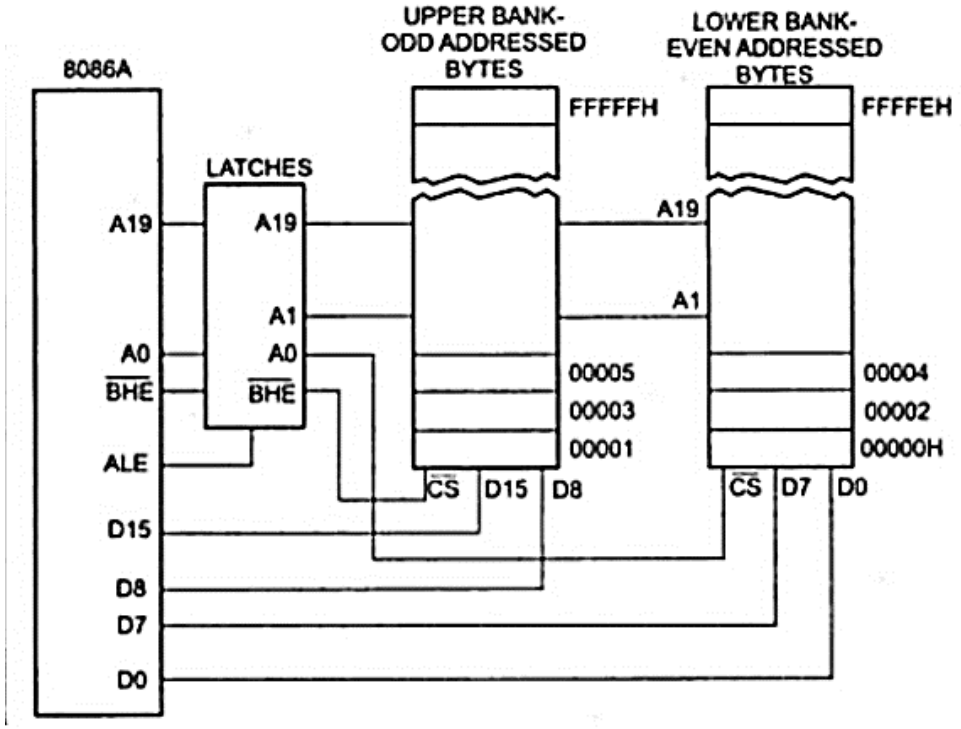
- $\overline{\mathbf{RQ}}$ / $\overline{\mathbf{GT0}}$, $\overline{\mathbf{RQ}}$ / $\overline{\mathbf{GT1}}$: (b) These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. $\overline{\mathbf{RQ}}$ / $\overline{\mathbf{GT0}}$ has a higher priority than $\overline{\mathbf{RQ}}$ / $\overline{\mathbf{GT1}}$.



Memory organization of 8086

To make it possible to read or write a word (16 bits) with one machine cycle, the memory of 8086 is set up as two banks.

- **Odd bank (512K)**
- **Even bank (512K)**



Operation	$\overline{BHE}$	A0	Bus cycles	Data lines used
R/W word from/to even address(Eg:MOV [0000], AX)	0	0	One	D0 - D15
R/W byte from/to odd address (Eg: MOV [0001], AL)	0	1	One	D8 – D15
R/W byte from/to even address(Eg: MOV [0000], AL)	1	0	One	D0 – D7
R/W word from/to odd address (Eg: MOV [0001], AX)	0	1	First	D8 – D15
	1	0	Second	D0 – D7

Differences between 8086 and 8088

8086	8088
16 bit data bus, 16 bit ALU	8 bit data bus, 16 bit ALU
6 byte instruction prefetch queue	4 byte instruction prefetch queue
8086 BIU will fetch new bytes into the pipelining queue when 2 bytes of the queue are empty.	8088 BIU will fetch a new byte into the pipelining queue when 1 byte of the queue is empty.
Odd/even memory bank organization to transfer 16-bit data at a time.	No odd/even bank arrangements
8086 has **M/$\overline{\text{IO}}$** pin to differentiate between memory and I/O operations.	8088 has **IO/$\overline{\text{M}}$** (active low is for M) pin to differentiate between memory and I/O operations.

References

- Doughlas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH, 2012.

Thank you