## COURSE: UCS1502 - MICROPROCESSORS AND INTERFACING

# Introduction to Microprocessor 8086

Dr. K. R. Sarath Chandran
Assistant Professor, Dept. of CSE

**This presentation covers**

• the basics of microprocessor 8086

**Learning Outcome of this Module**

• To understand the architecture of 8086

# Do you know ??

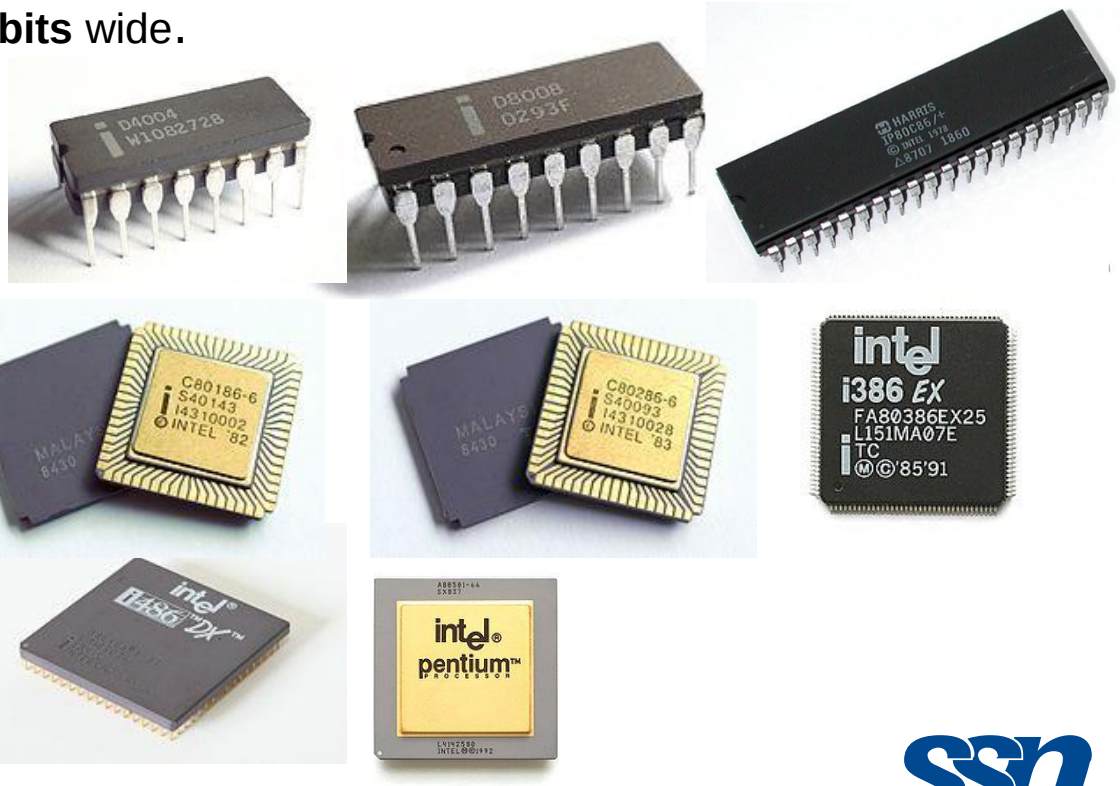
- What is a microprocessor ?
- Internal modules of a microprocessor
- n bit microprocessor – what is this “n” ?
- 8086 - Intel’s 16 bit processor

# Microprocessor

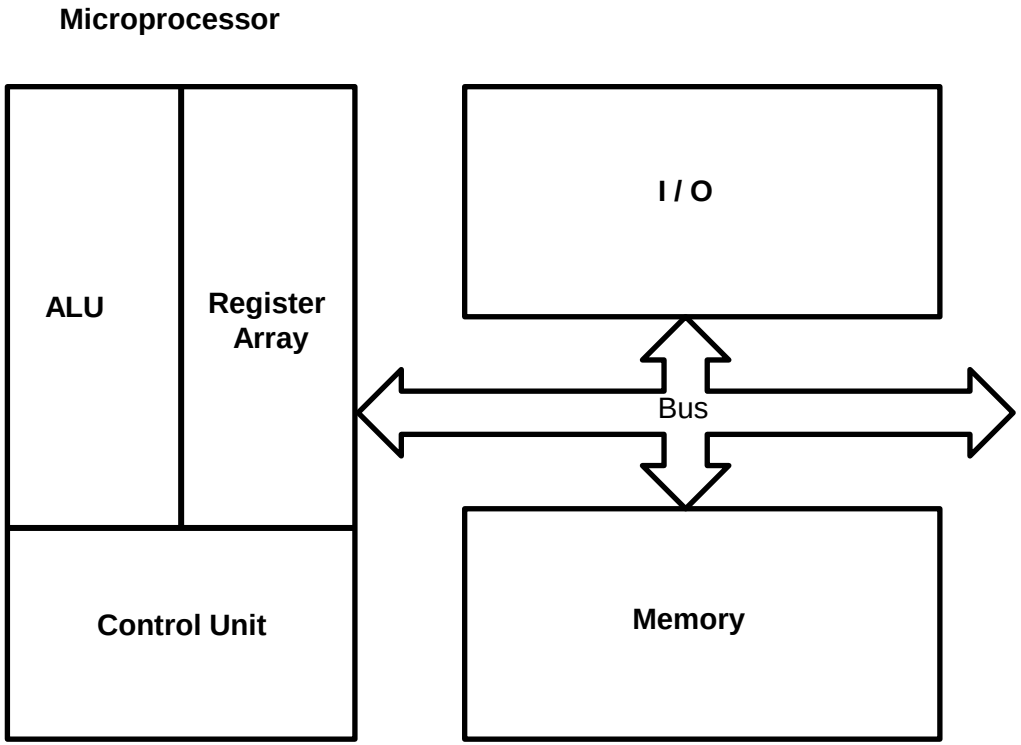
A multi-purpose programmable device that reads binary information from memory, accepting binary data as input and processes data according to those instructions.

| Intel's Processors | Bit size |
|---|---|
| 4004 | 4 |
| 8008 | 8 |
| 8080 | 8 |
| 8085 | 8 |
| 8086 | 16 |
| 8088 | 16 |
| 80186 | 16 |
| 80286 | 16 |
| 80386 | 32 |
| 80486 | 32 |
| Pentium … | 32 .. |

An **n-bit processor** is one in which the data registers, arithmetic Logic Units, and internal data paths, are **n bits** wide.



# Basic system structure




- **ALU**:
  Arithmetic and Logic Unit
- **Register array**:
  To store data temporarily during execution
- **Control unit**:
  Gives proper timing and control signals to all operations

**Basic operations**

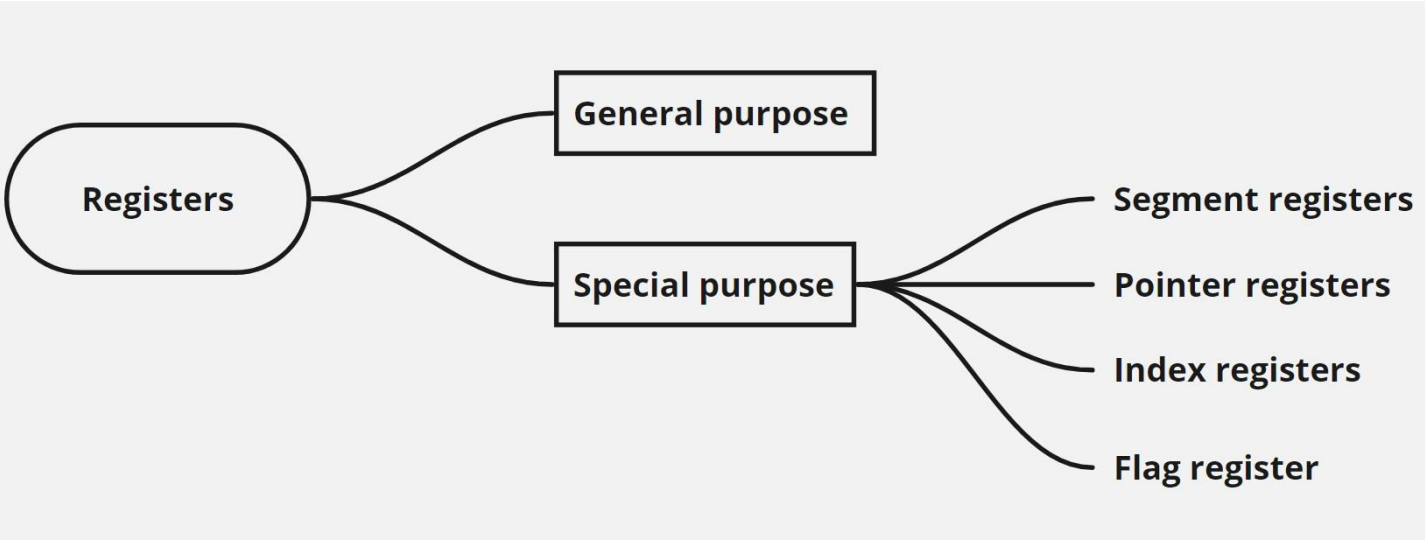
- Fetch
- Decode
- Execute

# Intel’s 8086 processor

- Intel’s first 16 bit processor
- Released in 1978
- Powerful instruction set compared to 8085
- All peripherals of 8085 are compatible with 8086
- 40 pin DIP
- Data bus width – 16 bit
- Address bus width – 20 bit
- Clock frequency range of different versions - 5, 8, 10 MHz
- Direct addressing capability – 1 MB of memory

# Register organization of 8086

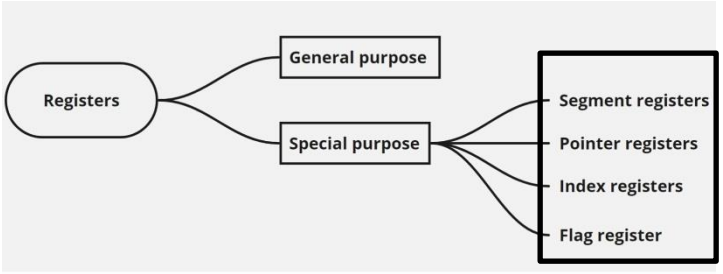
Register set

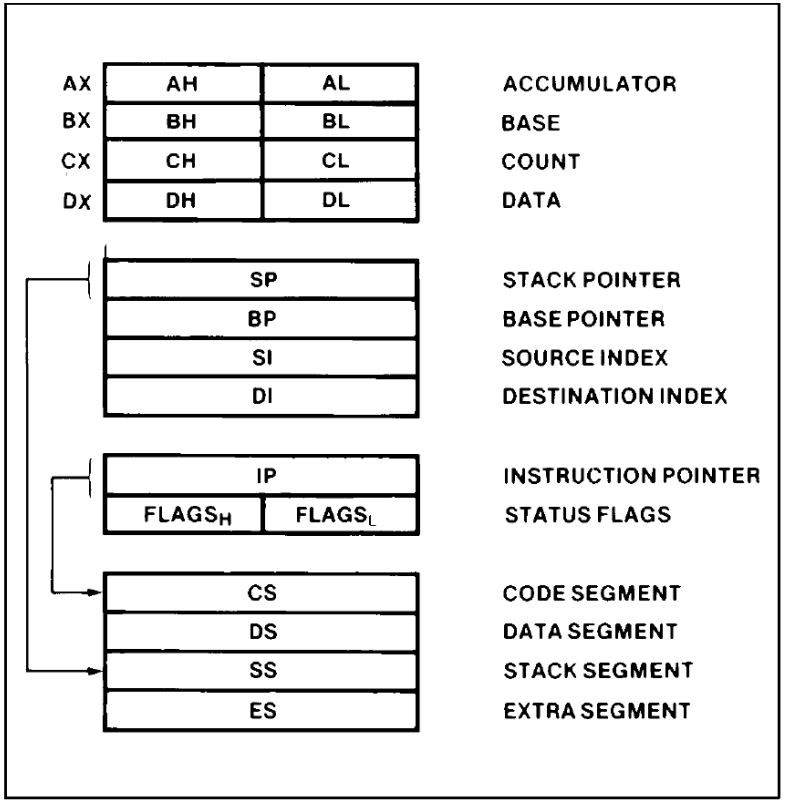



**General purpose registers :**

- AX, BX, CX, DX (16 bit registers)
- Each can also be used as 8 bit registers (AH, AL, BH, BL, CH, CL)

# Register organization of 8086




**Special purpose registers**

**Segment registers**

- 8086 supports segmented memory management
- CS, DS, SS, ES (16 bit segment base registers)

**Pointer registers**

- SP, BP, IP

**Index registers**

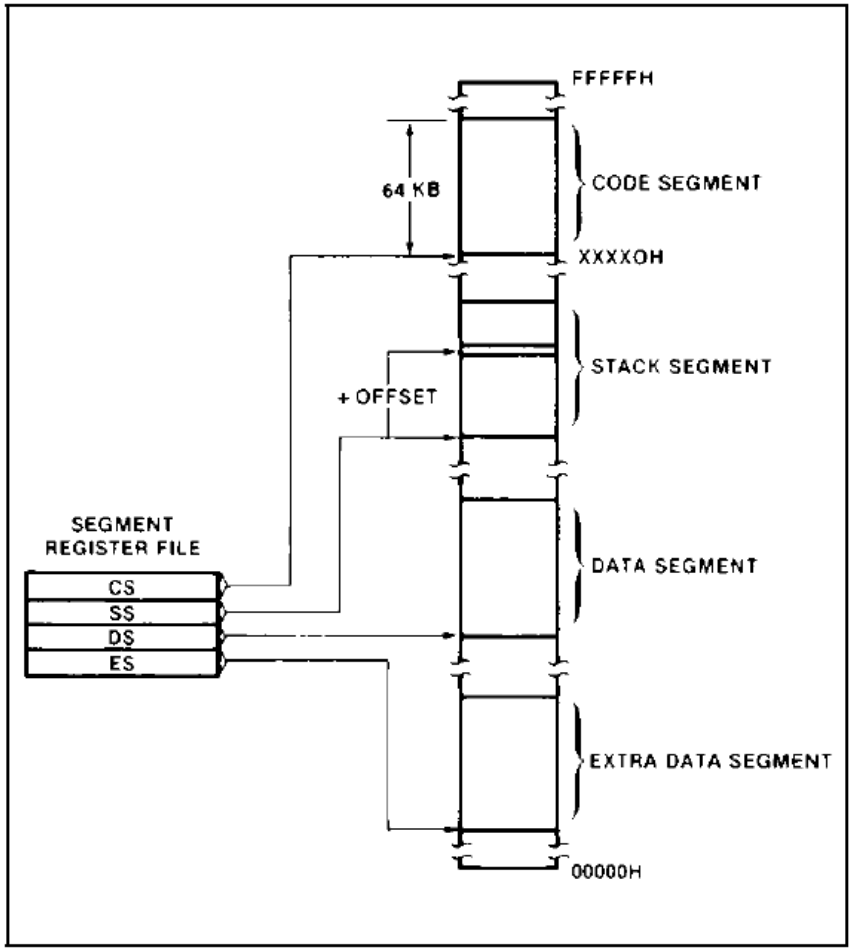
- SI, DI

**Flag register (16 bit)**

- Can also be accessed in 8 bits (FH, FL)

# Memory organization - Segments

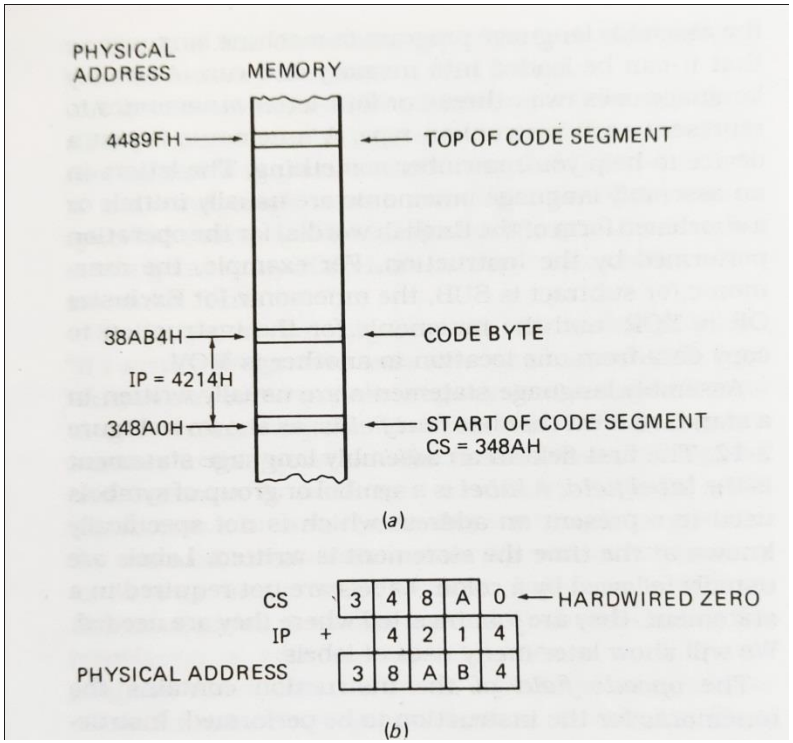
- The processor provides a 20-bit address to memory which locates the byte being referenced
- The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H).
- The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries.
- At load time: segment base register will be loaded with xxxx.
- During access:




20 bit address = segment register value << 4 + offset register value

# Memory organization - Segments

20 bit address = segment register value << 4 + offset register value




Source: D. V. Hall

# Internal architecture of 8086

- Architecture of 8086 has 2 functional units:

  **BIU** (Bus Interface Unit) and **EU** (Execution Unit).

---

- **BIU** takes care of sending addresses, fetching instructions from the memory, reading data from the ports and the memory as well as writing data to the ports and the memory.

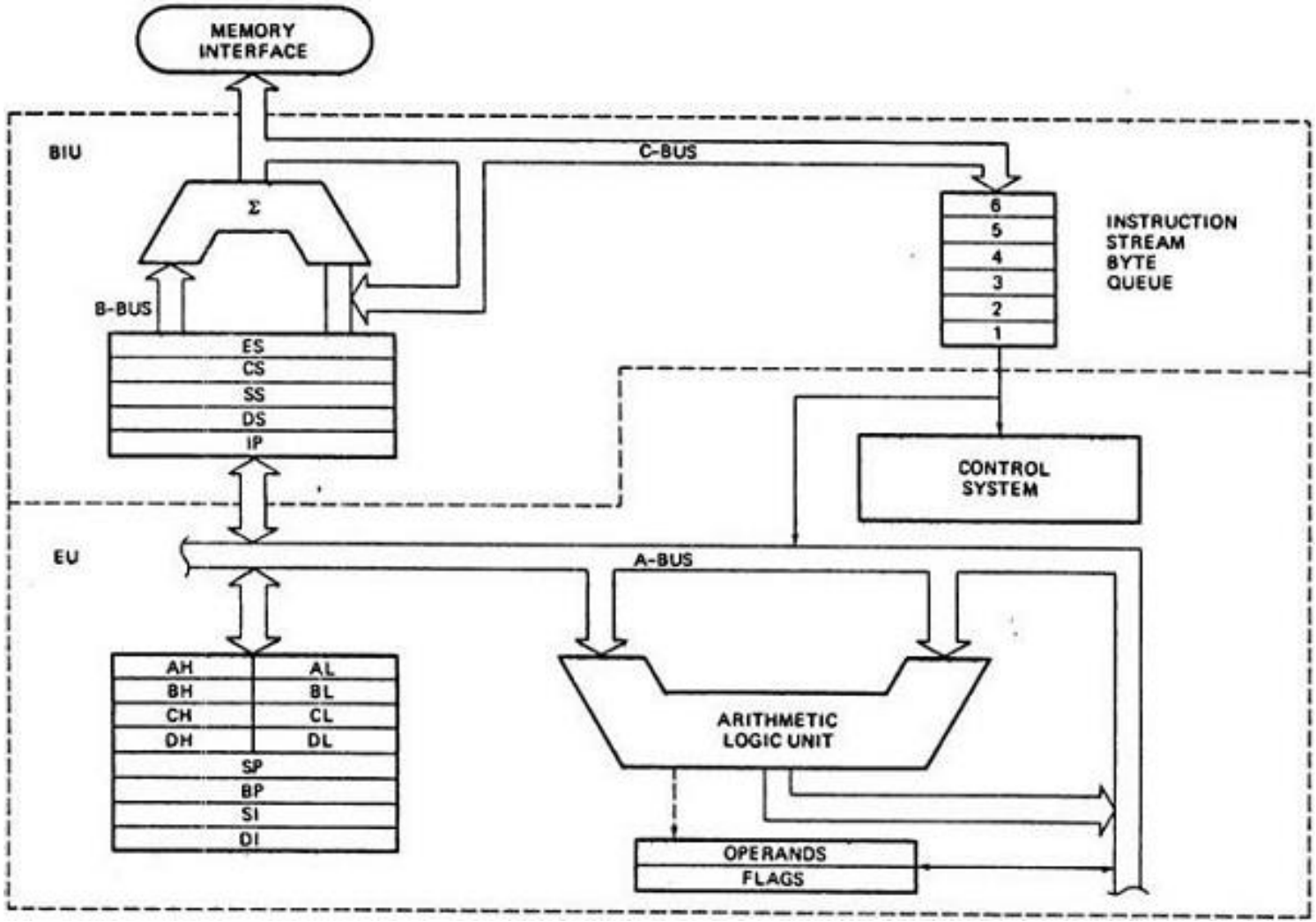
- **Instruction queue**
- **Segment register**
- **Instruction pointer**
- **Address generator**

---

- **Execution Unit** gives instructions to BIU stating from where to fetch the data and then decode and execute those instructions. Its function is to control operations on data using the instruction decoder & ALU.

- **ALU**
- **Flag Register**
- **General purpose registers, Index registers and other pointer registers**

# Internal architecture of 8086



# Summary

- 8086 is a 16 bit processor with ALU size of 16 bit and address bus size of 20 bit.
- It supports segmented memory management with the help of base and offset registers.
- 2 sections in its architecture – BIU and EU.

# References


- Doughlas V. Hall, “Microprocessors and Interfacing, Programming and Hardware”, Second Edition, TMH, 2012.

# Thank you