8086 – Instruction Set

Processor Control & Flag Control Instructions

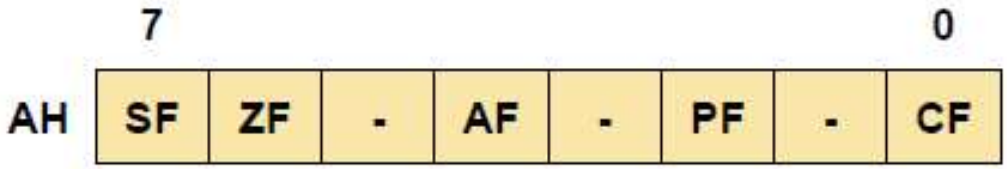
Learning Objective

We will be learning about the Flag Control & Processor Control Instructions:

- ✓ CLC / CMC / STC
- ✓ CLD / STD
- ✓ CLI / STI
- ✓ LAHF / SAHF
- ✓ HLT
- ✓ WAIT
- ✓ ESC
- ✓ LOCK
- ✓ Interrupt Operations

Flag Control Instructions

Mnemonic	Meaning	Operation	Flags affected
LAHF	Load AH from flags	(AH)←(Flags)	None
SAHF	Store AH into flags	(Flags)←(AH)	SF,ZF,AF,PF,CF
CLC	Clear carry flag	(CF)←0	CF
STC	Set carry flag	(CF)←1	CF
CMC	Complement carry flag	(CF)←NOT (CF)	CF
CLI	Clear interrupt flag	(IF)←0	IF
STI	Set interrupt flag	(IF)←1	IF



SF = Sign flag
ZF = Zero flag
AF = Auxiliary
PF = Parity flag
CF = Carry flag
- = Undefined (do not use)

Flag Control Instructions
Load Flag and Store Flag

LAHF	**LAHF** (no operands) Load AH from flags			**Flags** O D I T S Z A P C
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	4	—	1	LAHF

SAHF	**SAHF** (no operands) Store AH into flags			**Flags** O D I T S Z A P C R R R R R
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	4	—	1	SAHF

Flag Control Instructions – Carry Flag

CLC	CLC (no operands) Clear carry flag			Flags O D I T S Z A P C 0
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	CLC

CMC	CMC (no operands) Complement carry flag			Flags O D I T S Z A P C X
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	CMC

STC	STC (no operands) Set carry flag			Flags O D I T S Z A P C 1
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	STC

Flag Control Instructions – Direction Flag

Mnemonic	Meaning	Format	Operation	Flags affected
CLD	Clear DF	CLD	(DF)←0	DF
STD	Set DF	STD	(DF)←1	DF

CLD	**CLD** (no operands) Clear direction flag			**Flags** O D I T S Z A P C 0
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	CLD

STD	**STD** (no operands) Set direction flag			**Flags** O D I T S Z A P C 1
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	STD

Flag Control Instructions – Interrupt Flag

CLI	**CLI** (no operands) Clear interrupt flag			**Flags** O D I T S Z A P C 0
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	CLI

STI	**STI** (no operands) Set interrupt enable flag			**Flags** O D I T S Z A P C 1
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	STI

Processor Control Instructions – HLT

HLT	HLT (no operands) Halt			Flags O D I T S Z A P C
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	HLT

HLT

Halt

O	D	I	S	Z	A	P	C

Stops the CPU until a hardware interrupt occurs. (*Note:* The Interrupt flag must be set with the STI instruction before hardware interrupts can occur.)

Instruction format:

HLT

Processor Control Instructions – WAIT

WAIT	WAIT (no operands) Wait while TEST pin not asserted			Flags O D I T S Z A P C
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	3 + 5n	—	1	WAIT

WAIT — Wait for Coprocessor

O	D	I	S	Z	A	P	C

Suspends CPU execution until the coprocessor finishes the current instruction.
Instruction format:

```
WAIT
```

Processor Control Instructions – ESC

ESC	**ESC** external-opcode,source Escape			**Flags** O D I T S Z A P C
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
immediate, memory immediate, register	8 + EA 2	1 —	2-4 2	ESC 6,ARRAY [SI] ESC 20,AL

LOCK	**LOCK** (no operands) Lock bus			**Flags** O D I T S Z A P C
Operands	**Clocks**	**Transfers***	**Bytes**	**Coding Example**
(no operands)	2	—	1	LOCK XCHG FLAG,AL

Interrupt Instructions

Mnemonic	Meaning	Format	Operation	Flags affected
CLI	Clear interrupt flag	CLI	0 → (IF)	IF
STI	Set interrupt flag	STI	1 → (IF)	IF
INT n	Type n software interrupt	INT n	(Flags) → ((SP)-2) 0 → TF, IF (CS) → ((SP) – 4) (2+4xn) → (CS) (IP) → ((SP) – 6) (4xn) → (IP)	TF, IF
IRET	Interrupt return	IRET	((SP)) → (IP) ((SP)+2) →(CS) ((SP)+4) →(Flags) (SP) + 6 → (SP)	All
INTO	Interrupt on overflow	INTO	INT 4 steps	TF, IF

Summary

We have learnt about the Processor Control Instructions:

- ✓ CLC / CMC / STC
- ✓ CLD / STD
- ✓ CLI / STI
- ✓ LAHF / SAHF
- ✓ HLT
- ✓ WAIT
- ✓ ESC
- ✓ LOCK
- ✓ Interrupt Operations