Single LIF Neuron:

Diagram, schematic

Description automatically generated

Figure 1.

Op-amp U4 amplifies output voltage signal to activate NMOS M2 which drains the input voltage to the resting voltage of 60mV. An inductor L2 is placed at the gate of the NMOS to sustain the applied gate voltage, thereby inducing a “refractory” period. The oscillations should not be of concern due to the hysteresis mechanism of the Schmitt trigger.

Input Current and Input Voltage:

Chart, histogram

Description automatically generated

Figure 2.

Refractory Period

Output Spike (same input spike pattern as fig 2):

Chart, histogram

Description automatically generated

Figure 3.

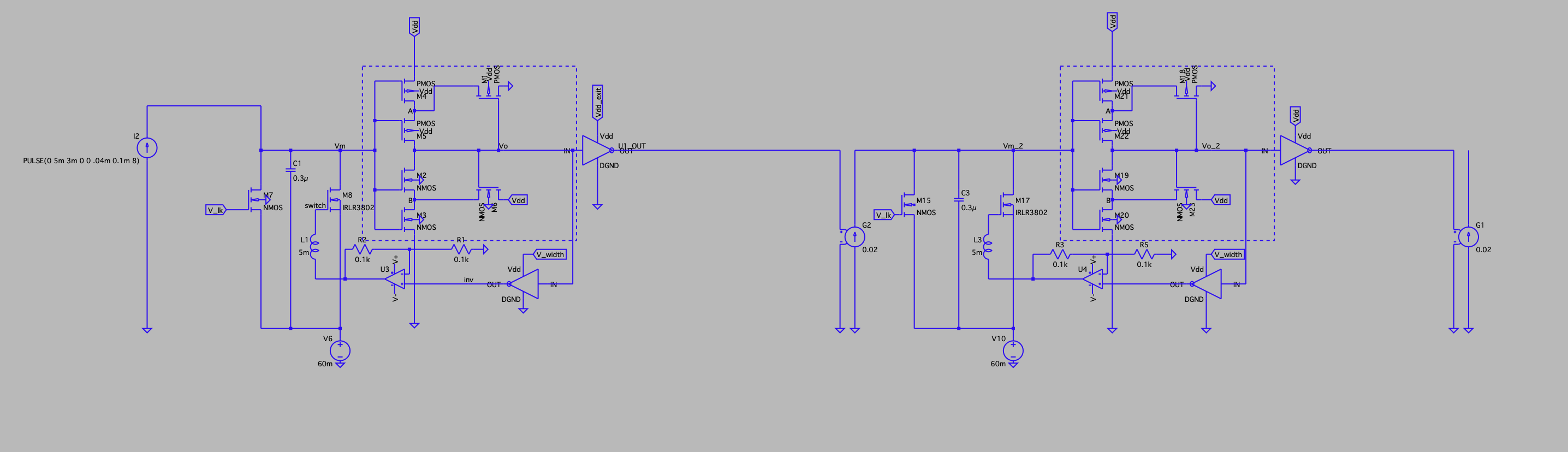
Problem: How to change width of output current spike. Looking into sample and hold circuit.

TWO NEURON NETWORK:

Diagram, schematic

Description automatically generated

N2Diagram, schematic

Description automatically generated

N1Diagram, schematic

Description automatically generatedDiagram, schematic

Description automatically generated

Figure 4.

Input voltage and output current spike of N1

Chart, histogram

Description automatically generated

Figure 5.

Input voltage and output current spike of N2:

Chart

Description automatically generated

Figure 6.

Input and output current spike of N2:

Chart

Description automatically generated

Figure 7.

Note that the output spike of N2 is larger than N1’s current spike. This can be overcome by changing the gain value of the voltage-controlled-current source.

THREE NEURON NETWORK:

Diagram, schematic

Description automatically generated

Figure 8.