



Phani Jayanth Jonnalagedda

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EDUCATION

- ◆ **Indian Institute of Technology Madras (IITM)** Chennai, India
- ◇ B. Tech (Honours) in Electrical Engineering and Minor in Computing: **CGPA 9.1/10** (July 2019 - June 2023)

PUBLICATIONS

- ◆ S. Mittal, S. Srivastava, and J. P. Jayanth, "A Survey of Deep Learning Techniques for Underwater Image Classification," in IEEE Transactions on Neural Networks and Learning Systems, DOI: 10.1109/TNNLS.2022.3143887 [\[Link\]](#)

SKILLS

- ◆ **Languages:** Bluespec Verilog, Verilog HDL, Python, C/C++
- ◆ **Frameworks:** PyTorch, ROS, CocoTb, Tensorflow
- ◆ **Tools:** Gem5, Spike, ChampSim, LTSpice, Electric, Eagle EDA
- ◆ **Others:** Git, Docker, LaTeX, Arduino, ESP32, RPi

PROJECTS

- ◆ **Extending Vector Support to SHAKTI C-Class Processor** ◆ **Prof. Kamakoti V** (Nov 2022 - Present)
 - ◇ Engineering configurable **Vector Functional Units** to add RISC-V Vector ISA support in SHAKTI C-Class Microprocessor.
- ◆ **Extending RISC-V ISA with Matrix-Multiply Support** ◆ **Prof. Sparsh Mittal** (Sep 2022 - Present)
 - ◇ Augmenting **Matrix-Multiply Extensions** to RISC-V ISA for accelerating AI-related Workloads (similar to Intel's AMX).
 - ◇ Aiming to achieve higher performance than RISC-V ISA's Scalar and Vector-based Matrix-Multiply implementations.
- ◆ **In-Memory Computing (IMC) Engine** ◆ **Prof. Janakiraman V** (Apr 2022 - Jun 2022)
 - ◇ Implemented an SRAM-based IMC Engine that can perform Multiply and Accumulate (**MAC**) with a **MAC** range of 128.
 - ◇ Constructed intricately-sized Charge-based and Current-based SRAM Cells with Decoupled Read and Write on Electric.
 - ◇ Achieved **98%** accuracy with the IMC Engine tuned on MNIST Dataset by employing 8-bit fixed-point inputs & weights.
- ◆ **Hardware Implementation of Discrete Cosine Transform (DCT)** ◆ **Prof. Kamakoti V** (Mar 2022 - May 2022)
 - ◇ Programmed **Butterfly Architecture-based fast DCT** algorithm in Bluespec Verilog for H.264 Module in SHAKTI C-Class.
 - ◇ Pipelined the design for maximum throughput, achieving **97.64%** Average Accuracy with minimal MSE Loss of **2.41**.
- ◆ **Accelerating Mandelbrot Fractal Image Generation** ◆ **Prof. Nitin Chandrachoodan** (Apr 2022 - May 2022)
 - ◇ Attained **3X** Performance Speedup by accelerating the Mandelbrot Fractal Generation on an FPGA using **HLS C**.
 - ◇ Analyzed several **HLS pragmas** and hardware parameters like word lengths, data I/O to optimize the implementation.
 - ◇ Utilized PYNQ framework to interface PYNQ-Z1 FPGA | Implemented AXI4 Stream Protocol to provide I/O to IP Block.
- ◆ **Pipelined RISC-V 32-bit Processor** ◆ **Personal Project (Group of 2)** (Sep 2021 - Oct 2021)
 - ◇ Built a 5-Stage Pipelined RISC-V 32-bit Processor with **Hazard Detection** and **Data Forwarding** Units, coded in **Verilog**.

PROFESSIONAL EXPERIENCE

- ◆ **Qualcomm India Private Limited** ◆ **Hardware Engineering Intern** Bengaluru, India (May 2022 - Aug 2022)
 - ◇ Developed a robust Python framework to perform exhaustive **retention register list analysis** for power optimization.
 - ◇ Identified 3658 potential redundancies (out of 7890 flops in camera sub-module) using Synopsys PrimeTime (PX).

POSITIONS OF RESPONSIBILITY

- ◆ **Core Member, Electronics Club, CFI¹, IITM** (Apr 2020 - Apr 2022)
 - ◇ Spearheaded a team of **50+** electronics enthusiasts working on **10+** projects | Managed club sessions and activities.
 - ◇ Designed a custom development board around **ESP-WROOM-32** SoC with built-in WiFi and Bluetooth functionalities.
 - ◇ **Project Head** for the Mountable Heads-up Display for Helmets project that assists bikers' navigation through traffic.
 - ◇ Taught **40+** participants about Parallel Programming, Multi-Threading (OpenMP), CUDA, and RTOS at Shaastra² 2022.

SCHOLASTIC & CO-CURRICULAR ACHIEVEMENTS

- ◇ Won **Gold** in DRDO's DRGE Autonomous Vision-based Obstacle Avoidance Drone Challenge in Inter IIT Tech Meet 9.0.
- ◇ Secured AIR³ **546** in JEE* Mains and AIR **685** in JEE* Advanced | Awarded the KVPY⁴ Fellowship in SA and SX Streams.