Phani Jayanth Jonnalagedda

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My research interests lie in **Computer Architecture**, **Parallel Processing**, and **Deep Learning**, specifically in robust and energy-efficient hardware accelerator architectures, Vector Processing, and In-Memory Computing techniques

EDUCATION

Indian Institute of Technology Madras (IITM)   Chennai, India
B. Tech (Honours) in Electrical Engineering and Minor in Computing: **CGPA 9.1/10**   (Jul 2019 - Jun 2023)

PUBLICATION

S. Mittal, S. Srivastava, and **J. P. Jayanth**, "A Survey of Deep Learning Techniques for Underwater Image   (Feb 2022)
Classification," in IEEE Transactions on Neural Networks and Learning Systems, DOI

SKILLS

Languages: Bluespec Verilog, Verilog HDL, Python, C/C++   **Frameworks:** PyTorch, ROS, CocoTb, Tensorflow, SciPy
Tools: Gem5, Spike, ChampSim, LTSpice, GNU Electric   **Others:** Git, Docker, LaTeX, AWS, Arduino, ESP32, RPi

RESEARCH PROJECTS

RISCV Vector ISA Support in SHAKTI C-Class, *Undergraduate Thesis, Prof. Kamakoti V, IITM*   (Nov 2022 - Present)
- Augmenting the SHAKTI C-Class Microprocessor with RISCV Vector ISA Support.
- Engineering configurable Vector Functional Units in Bluespec System Verilog.

Matrix-Multiply Support in RISCV ISA, *Prof. Sparsh Mittal, CANDLE Lab, IIT Roorkee*   (Sep 2022 - Present)
- Adding Matrix-Multiply Extensions and Approximate Instructions to RISCV ISA for accelerating AI Workloads.
- Benchmarking against RISCV Scalar and Vector-based implementations using Gem5 and Spike Simulators.

In-Memory Computing (IMC) Engine, *Prof. Janakiraman V, IITM*   (Apr 2022 - Jun 2022)
- Designed an SRAM-based IMC Engine that performs Multiply and Accumulate (MAC) with a MAC range of 128.
- Constructed Charge-based and Current-based SRAM Cells (with Decoupled Read-Write), Flash and Column ADCs, and Sense Amplifier on GNU Electric.
- Evaluated the Bitline Saturation Effect and the Energy-Delay Product (EDP) per MAC computation.
- Achieved 98% accuracy on simulating the IMC Engine tuned with MNIST dataset using 8-bit fixed-point inputs and weights in LTSpice.

Discrete Cosine Transform (DCT) in Hardware, *Prof. Kamakoti V, SHAKTI Lab, IITM*   [Report] (Mar 2022 - May 2022)
- Implemented 8-point DCT algorithm in Bluespec Verilog for the H.264 Video Codec Module of SHAKTI C-Class.
- Reduced the computational latency by employing Butterfly architecture-based Fast DCT Algorithm by 2.5X.
- Accelerated the execution by using a cosine look-up table and fixed-point operations instead of full-precision floating-point computations, incurring a minimal MSE Loss of 2.41.
- Pipelined the design for increased throughput and achieved an average accuracy of 97.64% on 8-point DCT.

TECHNICAL PROJECTS & COURSEWORK

Computer Architecture (CS6600), *Instructor: Prof. Madhu Mutyam, IITM*   [Report] (Nov 2022 - Dec 2022)
- Designed a hybrid Branch Predictor on ChampSim, combining the TAGE and Hashed Perceptron Predictors.
- Implemented predictor selection with a 4-bit Counter Table indexed using PC and Branch History Length of 13.
- Achieved 0.2% and 0.6% reduction in MPKI over the TAGE and Hashed Perceptron Predictors, respectively.
- Developed a hybrid LLC Replacement Policy on ChampSim, combining the Hawkeye and SHiP++ policies.

Secure Processor Microarchitecture (CS6630), *Instructor: Prof. Chester Rebeiro, IITM*   [Report] (Sep 2022 - Nov 2022)
- Performed Correlation and Differential Power Analysis attacks to obtain round keys from the CLEFIA Cipher.
- Executed the 8th Round Fault Injection attack on AES T-Table implementation for gleaning the AES round keys.
- Implemented Time-Driven and Evict+Time Cache Side-Channel attacks to extract the first round key of AES.

Acceleration of Mandelbrot Fractal Generation, *Prof. Nitin Chandrachoodan, Course: EE5332*　　(Apr 2022 - May 2022)
- Accelerated Static Mandelbrot Fractal Image Generation on an FPGA using HLS C, with advanced visual features like fractal coloring, panning, and zooming.
- Attained 3X speedup in performance over C-based software implementation of Mandelbrot Fractal Generation.
- Analyzed several HLS Pragmas and hardware parameters like arithmetic word lengths, memory types, and data I/O to optimize hardware design efficiently.
- Utilized PYNQ framework to interface PYNQ-Z1 FPGA and AXI4 Stream Protocol for data I/O to the IP Block.

Advanced Encryption Standard (AES) Algorithm Acceleration, *Prof. Nitin Chandrachoodan, Course: EE2003*　(Dec 2021)
- Accelerated standard and two security-enhanced versions of the AES algorithm on Artix 7 FPGA using Verilog.
- Interfaced the design with Microblaze Soft IP Core on Xilinx Vivado, providing I/O through C code using Vitis IDE.
- Achieved a 2X speedup in performance over C-based software implementation of the standard AES algorithm.
- Generated GDSII layout of the design for ASIC-based flow using the open-source silicon compiler OpenLane.

8-bit Signed Carry Save Multiplier (CSM), *Prof. Janakiraman V, Course: EE5311*　　　[Report] (Nov 2021 - Dec 2021)
- Designed the Schematic and Layout of an 8-bit Signed CSM, with and without pipelining on GNU Electric.
- Studied the design with multiple types of Full Adders (CSA, CLA) in the Vector Merge Stage of the Signed CSM.
- Simulated and Validated the DRC & LVS clean design using LTSpice and performed RC Extraction on the layout.

Pipelined RISCV 32-bit Processor, *Personal Project (Team of 2)*　　　　　　　　　　　　　　　(Sep 2021)
- Built a 5-Stage Pipelined RISCV ISA-based 32-bit Processor using Verilog HDL.
- Studied ways to detect and handle hazards in pipeline-based designs and ideated on Hazard Detection Unit and Data Forwarding Unit implementation in the processor.

PROFESSIONAL EXPERIENCE

Qualcomm, *Hardware Engineering Intern, GPU Design Team*　　　　　Bengaluru, India (May 2022 - Aug 2022)
- Developed a Python-based framework that uses design files to perform automated retention register list analysis to identify possible redundant retention registers in the design for power curtailment.
- Identified 3658 potential redundancies (out of 7890 retention registers in the Camera sub-module) utilizing PrimeTime(PX) STA and Power Analysis Tools from Synopsys.

LEADERSHIP & TEACHING EXPERIENCE

Core Member, Electronics Club, CFI, IITM　　　　　　　　　　　　　　　　(Apr 2020 - Apr 2022)
- Spearheaded a 3-Tier Team of 50+ electronics enthusiasts and managed club sessions and events on campus.
- Project Head for the Mountable Heads-Up Display for Helmets project that assists bikers in hassle-free navigation through traffic. Co-mentored the research-oriented study of Digital Design using FPGAs in the club.
- Designed a Development Board around ESP-WROOM-32 SoC with built-in WiFi and Bluetooth capabilities.

Workshop Trainer, Shaastra, IITM　　　　　　　　　　　　　　　　　　(Jan 2021 & Jan 2022)
- Taught 50+ participants the concepts of Parallel Programming (OpenMP), CUDA, and RTOS at Shaastra 2022.
- Instructed 100+ participants in Robotics and the Robot Operating System (ROS) framework at Shaastra 2021.

SCHOLASTIC & EXTRA-CURRICULAR ACHIEVEMENTS

- Won Gold in DRDO's DRGE Vision-based Obstacle Avoidance Drone Challenge in Inter IIT Tech Meet 9.0 of 2021.
- Secured an All-India Rank of 546 (of 1.2M+) in JEE Mains and 685 (of 170K+) in JEE Advanced Exams of 2019.
- Awarded the KVPY National Fellowship by the Indian Institute of Science (IISc) in both SA and SX Streams.

HOBBIES & INTERESTS

- Proficient in multiple drawing and painting mediums - Oils, Acrylic, Watercolours, Charcoal, and Pastels.
- Avid Reader of Fiction and Fantasy Thrillers. Writing Enthusiast.

SHAKTI - India's first Indigenous RISC-V Microprocessor developed at IITM, CFI - Centre for Innovation (India's Largest Student-Run Research Lab at IITM), Shaastra - Annual Tech Fest of IITM
JEE - Joint Entrance Examination for entry into Engineering Colleges in India, KVPY - Kishore Vaigyanik Protsahan Yojana Fellowship in Sciences offered by Indian Institute of Science (IISc)