Phani Jayanth Jonnalagedda

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EDUCATION

✦ **Indian Institute of Technology Madras (IITM)** Chennai, India

✧ B. Tech (Honours) in Electrical Engineering and Minor in Computing: **CGPA 9.1/10** (July 2019 - June 2023)

RESEARCH INTERESTS

✦ Computer Architecture, Hardware Accelerators, Parallel Processing, In-Memory Computing, Deep Learning

PUBLICATIONS

✦ S. Mittal, S. Srivastava, and **J. P. Jayanth**, "A Survey of Deep Learning Techniques for Underwater Image Classification," in IEEE Transactions on Neural Networks and Learning Systems, DOI

SKILLS

✦ **Languages:** Bluespec Verilog, Verilog HDL, Python, C/C++

✦ **Frameworks:** PyTorch, ROS, CocoTb, Tensorflow

✦ **Tools:** Gem5, Spike, ChampSim, LTSpice, Electric, Eagle EDA

✦ **Others:** Git, Docker, LaTeX, Arduino, ESP32, RPi

RESEARCH EXPERIENCE

✦ **Extending Vector Support to SHAKTI@ C-Class Processor** ✦ **Prof. Kamakoti V** (Nov 2022 - Present)

✧ Currently engineering configurable **Vector Functional Units** to add RISC-V Vector ISA support in SHAKTI C-Class.

✦ **Extending RISC-V ISA with Matrix-Multiply Support** ✦ **Prof. Sparsh Mittal** (Sep 2022 - Present)

✧ Augmenting **Matrix-Multiply Extensions** to RISC-V ISA for accelerating AI-related Workloads (like Intel's AMX).

✧ Aiming to achieve higher performance than RISC-V Scalar and Vector-based Matrix-Multiply implementations.

✦ **In-Memory Computing (IMC) Engine** ✦ **Prof. Janakiraman V** (Apr 2022 - Jun 2022)

✧ Designed an **SRAM-based** IMC Engine that performs Multiply and Accumulate (**MAC**) with a **MAC** range of 128.

✧ Constructed intricately-sized **Charge-based** and **Current-based** SRAM Cells (with Decoupled Read-Write), Flash and Column ADCs, and Sense Amplifier on the **Electric** software.

✧ Evaluated the **Bitline Saturation Effect** and the **Energy-Delay Product** per MAC computation.

✧ Achieved **98%** accuracy on simulating the IMC Engine tuned with MNIST Dataset by employing 8-bit fixed-point inputs & weights.

✦ **Hardware Implementation of Discrete Cosine Transform (DCT)** ✦ **Prof. Kamakoti V** (Mar 2022 - May 2022)

✧ Implemented 8-point DCT algorithm in **Bluespec Verilog** for the H.264 Video Codec Module in SHAKTI C-Class.

✧ Reduced the time complexity from $O(n^2)$ to O(nlogn) through **Butterfly architecture**-based **fast DCT** algorithm.

✧ Employed a cosine look-up table and fixed-point operations to accelerate the execution while meeting the design requirements, incurring a minimal MSE loss of **2.41**.

✧ Pipelined the design for maximum throughput and achieved an overall average accuracy of **97.64%**.

RELEVANT COURSE PROJECTS

✦ **Accelerating Mandelbrot Fractal Image Generation** ✦ **Prof. Nitin Chandrachoodan** (Apr 2022 - May 2022)

✧ Accelerated the static Mandelbrot Fractal Generation on an FPGA using **HLS C**, with advanced visual features of fractal coloring, panning, and zooming and attained **3X** Speedup over C-based software implementation.

✧ Analyzed several **HLS Pragmas** and hardware parameters like arithmetic word lengths, memory types, and data I/O to optimize the performance of the hardware design.

✧ Utilized **PYNQ** framework to interface PYNQ-Z1 FPGA and **AXI4** Stream Protocol for data I/O to the IP Block.

✦ **Accelerating the Advanced Encryption Standard (AES) Algorithm** ✦ **Prof. Nitin Chandrachoodan** (Dec 2021)

✧ Accelerated the standard and two modified versions of the AES algorithm on an Artix 7 FPGA using **Verilog** HDL.
✧ Interfaced the design with Microblaze Soft IP Core on **Xilinx Vivado**, providing I/O through C code on **Vitis IDE**.
✧ Achieved a **2X** Performance Speedup over C-based software implementation of AES.
✧ Analyzed the security aspects (**Avalanche Effect**) of the standard and modified versions of the AES algorithm.
✧ Generated **GDSII** layout of the design for ASIC-based flow using the open-source silicon compiler **OpenLane**.

✦ **Designing an 8-bit Signed Carry Save Multiplier (CSM)** ✦ **Prof. Janakiraman V** (Nov 2021 - Dec 2021)

✧ Designed the Schematic and Layout of an 8-bit Signed CSM, with and without pipelining using **Electric** software.
✧ Studied the design utilizing multiple types of Full Adders (**CSA**, **CLA**) in the **Vector Merge** Stage of the CSM.
✧ Simulated and Validated the DRC & LVS clean design using **LTSpice** and performed **RC Extraction** on the layout.

OTHER PROJECTS

✦ **Pipelined RISCV 32-bit Processor** ✦ **Personal Project (Team of 2)** (Sep 2021)

✧ Built a **5-Stage Pipelined** RISCV ISA-based 32-bit Processor, with pipeline stages and modules coded in **Verilog**.
✧ Studied ways to handle hazards in pipeline-based designs and ideated on **Hazard Detection** Unit and **Data Forwarding Unit** implementation in the processor.

✦ **Electronics Club Development Board** ✦ **Electronics Club, CFI[ǂ], IITM** (Jan 2021 - Feb 2021)

✧ Designed a development board around **ESP-WROOM-32 SoC** with built-in WiFi and Bluetooth capabilities.
✧ Developed the layout on the EasyEDA platform adhering to the **PCB design** rules. The board was fabricated by JLCPCB (China) and deployed for use in our club projects and electronics teaching sessions across campus.

PROFESSIONAL EXPERIENCE

✦ **Qualcomm India Private Limited** ✦ **Hardware Engineering Intern** Bengaluru, India (May 2022 - Aug 2022)

✧ Worked on power optimization in the GPU subsystems (Camera and Video modules) in the **GPU Design Team**.
✧ Developed a robust Python-based framework that uses design files to perform exhaustive **retention register list analysis** to identify possible redundant registers in the design for power curtailment.
✧ Identified 3658 potential redundancies (out of 7890 registers in the camera sub-module) using **PrimeTime PX** STA and Power Analysis Tool from **Synopsys**.

POSITIONS OF RESPONSIBILITY

✦ **Core Member, Electronics Club, CFI[ǂ], IITM** (Apr 2020 - Apr 2022)

✧ Spearheaded a 3-Tier Team of **50+** electronics enthusiasts, managing club sessions and activities on campus.
✧ **Project Head** for the Mountable Heads-up Display (HUD) for Helmets project that assists bikers in hassle-free navigation through traffic. **Co-mentored** research-oriented study of **Digital Design using FPGAs** in the club.

✦ **Workshop Trainer, Shaastra[♯], IITM** (Jan 2022)

✧ Taught **40+** participants the concepts of Parallel Programming (on OpenMP), CUDA, and RTOS at Shaastra[♯].

SCHOLASTIC & EXTRA-CURRICULAR ACHIEVEMENTS

✧ Won **Gold** in DRDO's DRGE Vision-based Obstacle Avoidance Drone Challenge in Inter IIT Tech Meet 9.0 of 2021.
✧ Secured an All-India Rank of **546** (of 1.2M+) in JEE* Mains and **685** (of 170K+) in JEE* Advanced Exams of 2019.
✧ Awarded the **KVPY[$]** National Fellowship by the Indian Institute of Science (IISc) in both SA and SX Streams.

HOBBIES & INTERESTS

✧ Proficient in multiple drawing and painting mediums - Oils, Acrylic, Watercolours, Charcoal, and Pastels.
✧ Avid reader of fiction and fantasy thrillers. Writing enthusiast.

@SHAKTI - India's first Indigenous RISC-V Microprocessor developed at IITM
ǂCentre for Innovation (Student-Run Research Lab at IITM) ♯Annual Tech Fest of IITM *Joint Entrance Examination $Kishore Vaigyanik Protsahan Yojana