INDIAN INSTITUTE OF TECHNOLOGY ROPAR

CP301: Development Engineering Project

DIGITAL FREQUENCY LOCKED LOOP FOR HEAVILY DISTORTED GRID SYSTEMS

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ABSTRACT

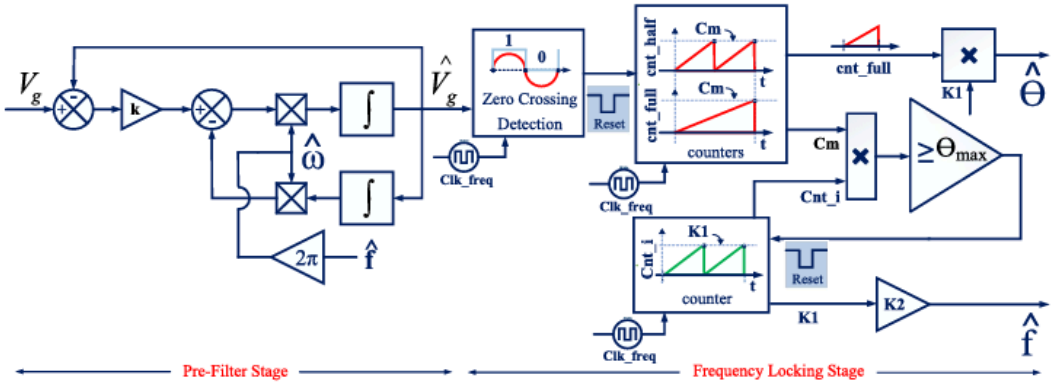
Grid-connected converters require grid frequency and phase information for controlling the power injections into the grid. This information is achieved by a phase-locked loop (PLL) or frequency-locked loop (FLL) algorithms. The accuracy, reliability, and ease of implementation of the PLL/FLL algorithms in all grid conditions dictate the performance of the grid-connected converters. This article proposes a digital FLL for single-phase grid-connected systems. The proposed FLL tracks the frequency accurately, even in heavily distorted grid conditions. It uses a second-order generalized integrator (SOGI) as a pre-filter and a digital counter, based on the zero-crossing detection (ZCD) logic for estimating the grid frequency and phase angle. It does not require complex filters and tuning of multiple parameters. The implementation of the proposed FLL is simple and has less computational overhead. The ability of the proposed FLL to track the frequency and phase under various steady-state (dc-offset and harmonics) and transient (voltage sag, frequency drift, and phase jump) grid disturbances is tested in simulation using MATLAB/SIMULINK, and the results are reported. The experimental validation is done using a field programmable gate array (FPGA) controller in the laboratory. The proposed algorithm is able to track the estimates within 1.2 cycles of the grid voltage when tested under a heavy-distorted grid having 26.4% total harmonic distortion (THD). The measurement uncertainties and results of single-phase grid-connected inverter (GCI) using the proposed FLL are also presented

INTRODUCTION

GRID-CONNECTED inverters (GCIs) have received considerable attention in recent years because of their widespread use in renewable energy generation, active power filters, and uninterrupted power supply . For safe and reliable operation of GCIs under adverse grid conditions, precise, smooth, and rapid estimate of grid frequency and phase is critical. It is accomplished by the use of synchronizing techniques. In single-phase and three-phase power generation, synchronization is achieved using two popular methods, categorized as FLL and phase-locked loop (PLL). FLL techniques provide benefits of fast synchronization, simple structure, and PI-less control eliminating bandwidth-related issues. However, they have performance limitations during abnormal grid conditions such as dc offset and harmonics . FLL-based techniques also face difficulty in the design of filters for suppressing harmonics and dc-offset present in the grid voltage. Conventional FLL techniques such as DFT -based recursive methods and Kalman filters are available but they involve complex calculations, the need of prior knowledge about covariance matrix, and issues related to spectral leakage. In literature, researchers have proposed various techniques to resolve these issues. The SOGI-FLL is presented in . It is based on a gradient descent algorithm to obtain frequency and phase accurately. But, due to the low-pass filter nature of the orthogonal component in SOGI, the SOGI-FLL requires additional filters for removing the dc component. To address this drawback, an offset estimation and rejection loop are presented in]. However, if the dc-gain is not exact to the offset value, it can lead to errors. However, each SOGI stage corresponds to a particular harmonic. Hence, it is difficult to eliminate the ever-changing harmonics during off nominal frequencies. In , the SOGI-FLL structure is used along with a prefilter or in-loop filter stage obtained using another SOGI to eliminate the unwanted components from the sensed grid voltage. However, the in-loop filter stage limits the dynamics of FLL in achieving synchronization, whereas the pre-filter is showing effective results but with a reduction in phase margin. In , the prefilter-based SOGI-FLL is proposed to reject the dc offset and attenuate the harmonics. It is effective but at the cost of complexity and computational burden on the system. A prefilter-based frequency and phase estimation is proposed in . The frequency required for the prefilter is obtained by an additional frequency estimation technique. In , a fixed delay length-based adaptive FLL with a fast dynamic response is proposed. However, it requires huge memory and higher sampling frequencies. A complex bandpass filter (CBFs) is proposed to filter harmonics. However, the estimates have steady-state oscillations even for fourth-order systems. Multiple CBF stages similar to M-SOGI are used to eliminate the harmonics. However, the slow transient response with the computational burden on the processor is inevitable. A circular limit cycle oscillator (CLO) and multi-CLO-FLL has been proposed as a robust FLL but it has poor performance with dc offset in the grid and requires pre-filter stages to gain harmonic suppression ability. The cascaded delayed signal cancellation (CDSC) FLL is proposed in . The dc offset and harmonics in the grid are properly handled by this FLL. However, CDSC-FLL provides poor harmonic filtering during off-nominal frequencies. It also requires more memory and computations. In higher order FLLs are proposed to estimate the frequency and phase accurately. However, they have brought more nonlinearity, complex calculations, demand for additional memory, and require controllers with high processing speed.

MODEL

BLOCK DIAGRAM:



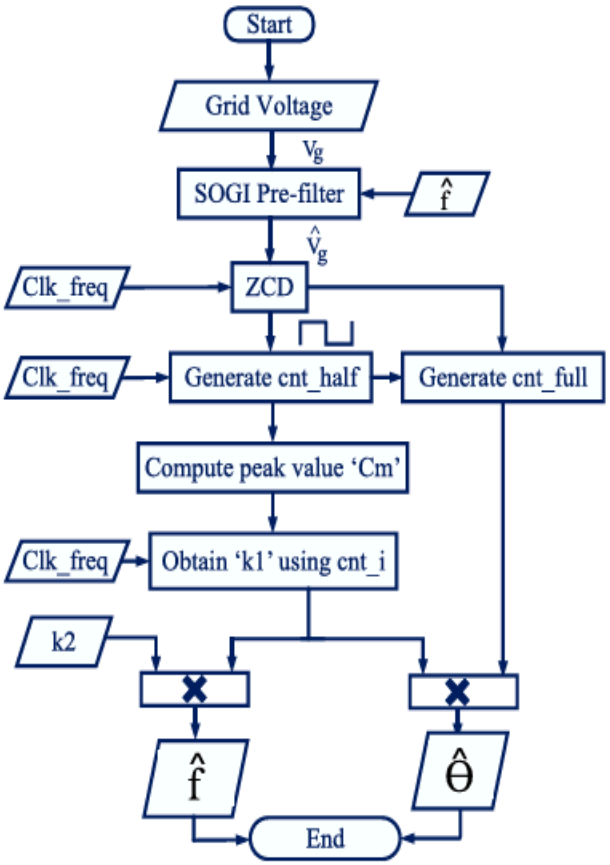


Fig. 2. Flowchart of the proposed algorithm.

THEORY

A. Pre-Filter Stage:

1) Selection of Pre-Filter: The proposed FLL requires dc offset elimination, high-frequency noise rejection, and some attenuation to harmonics from the pre-filter stage. This can be achieved if the pre-filter stage offers a bandpass characteristic to the grid voltage. Hence, SOGI which has bandpass proper ties to the in-phase component [5] is chosen as the pre-filter as shown in the block diagram

2) Design of Pre-Filter: The output to input transfer function of the SOGI pre-filter stage is given as

$$\frac{\hat{V}_g(s)}{V_g(s)} = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \qquad (1)$$

where ω is the frequency estimate in rad/s. This transfer function is plotted considering a grid frequency of 50 Hz for different values of damping coefficient "k". It is evident that the bandwidth of the SOGI-bandpass filter will alter for different values of "k." The bandwidth increases with an increase in "k" and vice versa. Choosing a smaller value of "k" provides more attenuation to the frequencies other than fundamental but this results in sluggish dynamic response of the system. Hence, the selection of "k" is a trade-off between filtering and the swift dynamic response of the system. As mentioned earlier, complete/more attenuation to harmonics is not required from the pre-filter stage. Hence, a reasonable bandwidth is chosen (k = 3) in this work to give improved dynamic response.

3) Digital Implementation of Pre-Filter: Digital implementation of the SOGI pre-filter stage with the designed parameters is carried out following. The Euler backward method is used for implementing SOGI-based pre-filter stages digitally. The prefilter stage is represented as the "SOGI Pre-filter" block in the flowchart

B. Frequency Locking Stage

Frequency locking stage deals with the precise and rapid estimation of the two quantities for synchronization, viz. frequency and phase. This stage is divided into three parts namely ZCD, estimation of grid frequency, and phase angle.

1) Zero Crossing Detection: The basic idea of using ZCD is to estimate the fundamental frequency by utilizing zero crossing instants. Initially, the filtered grid voltage ˆ Vg (free from dc-offset and noise) is compared with zero to obtain a 1-b square wave having logic 1 in a positive half cycle and logic 0 in the negative half cycle of input. From the square wave, the positive and negative zero crossings are obtained from 0 to 1 transition and 1 to 0 transition, respectively. This stage is represented as "ZCD" block in the flowchart

2) Estimation of Grid Frequency (f): Frequency is estimated using a digital counter (cnt_half) that increments using a predefined high-frequency digital clock (of the order of few kHz) and resets to zero at every zero crossing instant given by the ZCD. This part is represented by the "Generate cnt_half" block in the flowchart . The peak value of the counter Cm is saved to a register when it is reset by ZCD as shown by the "Compute peak value Cm" block in the flowchart. It can be observed that the counter cnt_half resets to zero for every half cycle of the input signal (grid voltage). Therefore, the relation between the estimated grid frequency (f)and the digital clock frequency (Clk_freq) is given as

$$\frac{1}{2\hat{f}} = \frac{C_m}{\text{Clk\_freq}} \Rightarrow \hat{f} = \frac{\text{Clk\_freq}}{2C_m}. \qquad (2)$$

3) Estimation of Grid Phase Angle (ˆ θ): The grid phase angle ˆ θ is obtained in a different manner using the already available counter cnt_half to minimize the number of computations. This method of estimation also helps to obtain the grid frequency from (2) without the use of division operation. For the grid phase angle, a counter with full-cycle reset is required. For this purpose, a full-cycle counter cnt_full is created using the available half-cycle counter cnt_half. It is given as follows.

After 0 to 1 transition of ZCD square wave

$$\texttt{cnt\_full} = \frac{\texttt{cnt\_half}}{2}. \qquad (3)$$

After 1 to 0 transition of ZCD square wave

$$\texttt{cnt\_full} = \frac{\texttt{cnt\_half} + C_m}{2}. \qquad (4)$$

The number of bits required in cnt_half and cnt_full is maintained the same. A half-cycle counter is used for full-cycle generation so that the frequency and phase changes, if any, will be updated in a half-cycle time period. This improves the dynamic response of the proposed FLL to grid disturbances. The grid phase angle (ˆ θ) which increments from 0 to θmax (corresponding to 360◦ or 2π radians) for one cycle can be obtained from cnt_full with appropriate scaling. The scaling factor required to generate ˆ θ from cnt_full varying from 0 to Cm is given as

$$\hat{\theta} = \theta_{\max} \times \frac{\texttt{cnt\_full}}{C_m} = \text{K1} \times \texttt{cnt\_full} \qquad (5)$$

Where

$$\text{K1} = \theta_{\max}/C_m. \qquad (6)$$

a) Calculation of K1: It can be observed from (6) that θmax is a constant and Cm is a variable quantity that changes with grid frequency. Therefore, the value of K1 is obtained iteratively using a counter cnt_i as follows.

1) Initialize cnt_i to zero.
2) Compute cnt_i × Cm.
3) If cnt_i × Cm <θmax, increment cnt_i and go to Step 2.
4) Else, K1 = cnt_i and exit.

This part of the algorithm where K1 is obtained using cnt_i is represented as the “Obtain ‘K1’ using cnt_i” block in the flowchart. For faster convergence, these iterations can be performed at a high frequency using the same digital clock used to increment cnt_half.OnceK1 is obtained,the phase angle is estimated using (5) as shown in Fig. 2. The grid frequency estimate is also derived using K1 and (2) as follows:

$$\hat{f} = \frac{\text{Clk\_freq}}{2\theta_{\max}} \times \text{K1} = \text{K2} \times \text{K1} \qquad (7)$$

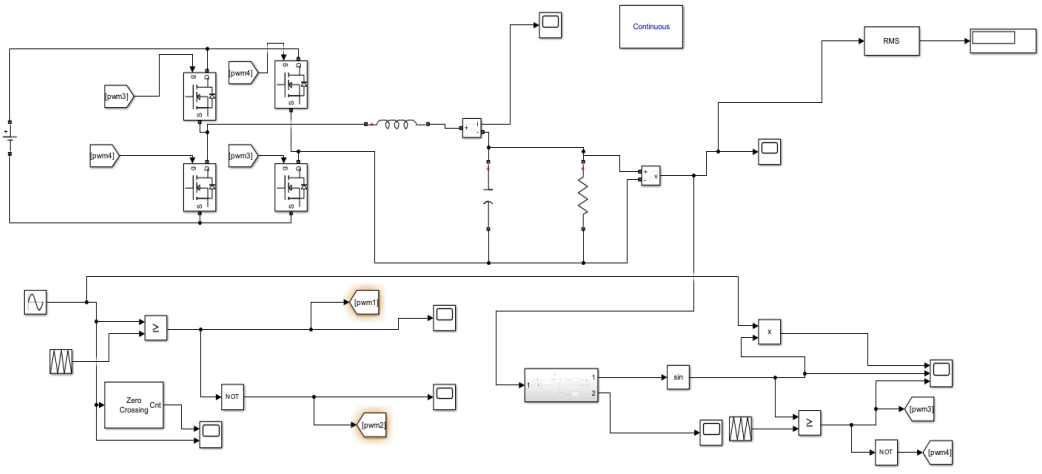
where K2 is a constant given by

$$\text{K2} = \frac{\text{Clk\_freq}}{2\theta_{\max}}. \qquad (8)$$

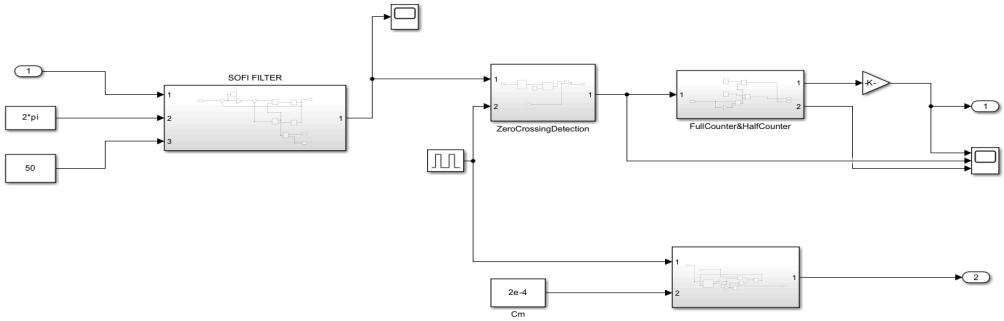
TABLE I

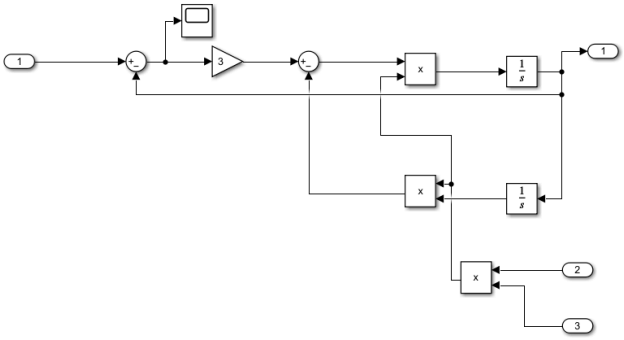
DIGITAL IMPLEMENTATION SPECIFICATIONS

Variable name	Bit-width	Format	Specification
Nominal frequency/Worst case frequency			50 Hz/47 Hz
100% Grid Voltage in RMS			230 V
Digital clock frequency, Clk_freq			3.125 MHz
C_m, cnt_half, cnt_full, cnt_i, K1, K2	16	16.0	
θ_{max}, $\hat{f}$, $\hat{\theta}$	32	8.24	

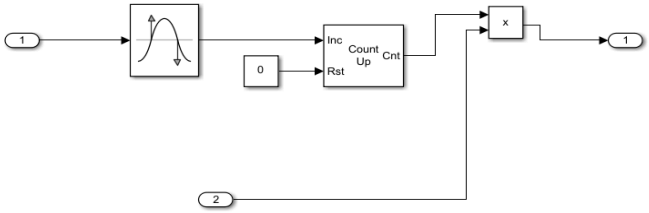


Simulated Single phase grid with sine PWM

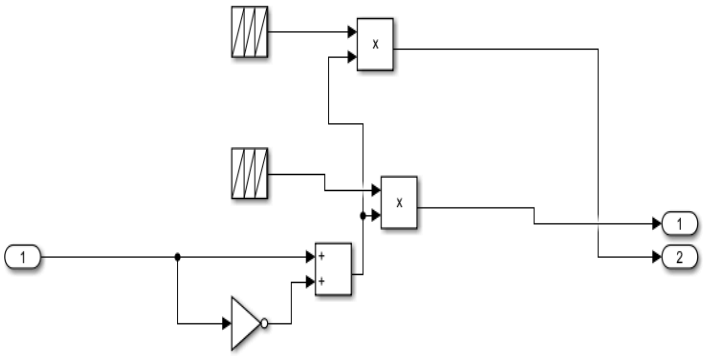

1
2*pi
50
SOFI FILTER
ZeroCrossingDetection
FullCounter&HalfCounter
K-
1
2
2e-4
Cm


1
3
x
1
s
2
3

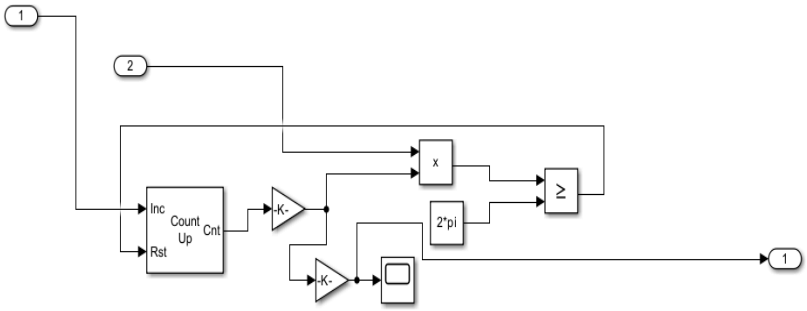
SOGI FILTER



ZERO CROSSING DETECTOR

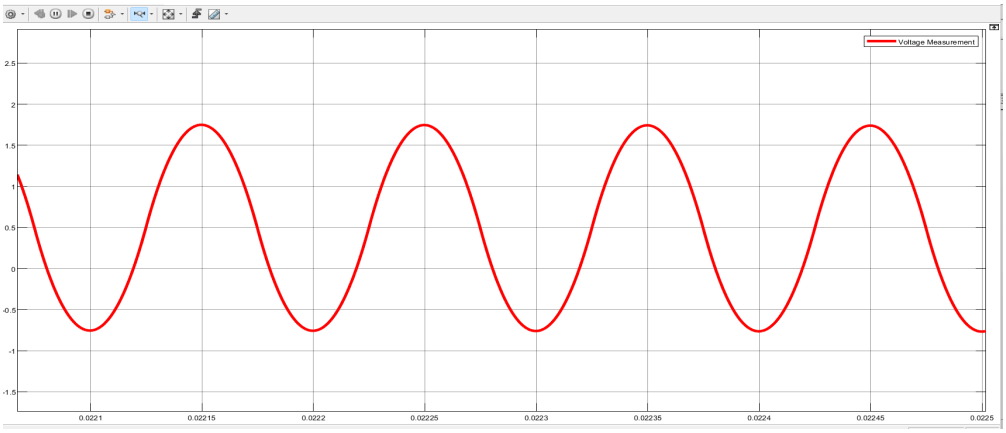


Full and half Counters

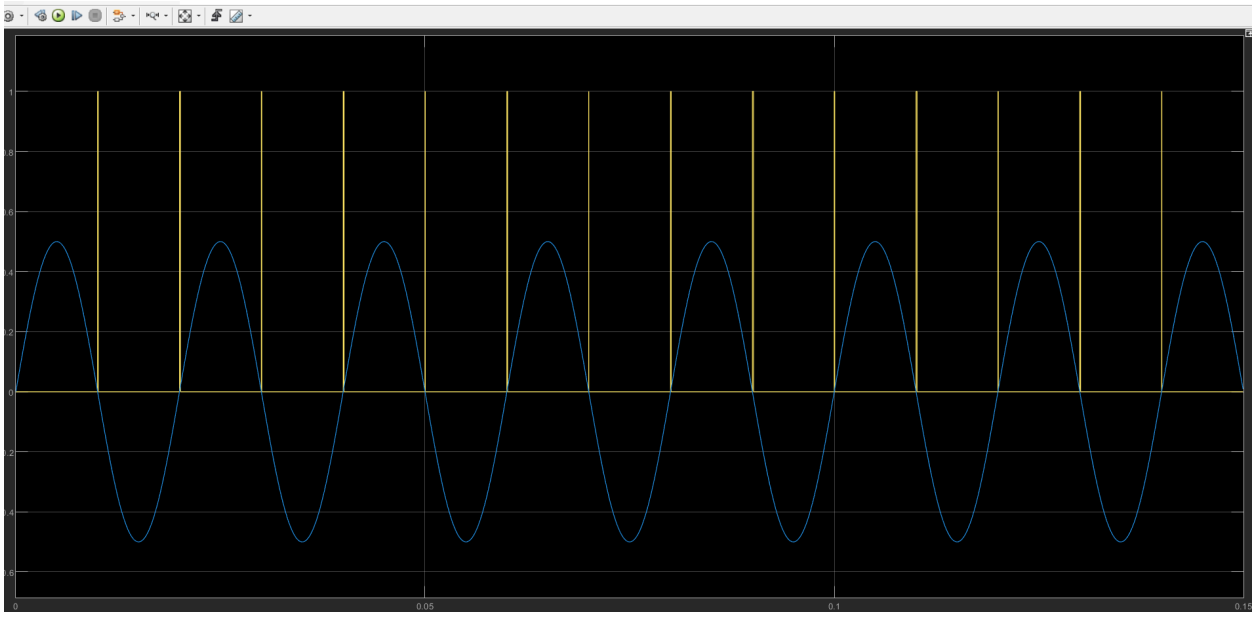


Counter Cnt_i

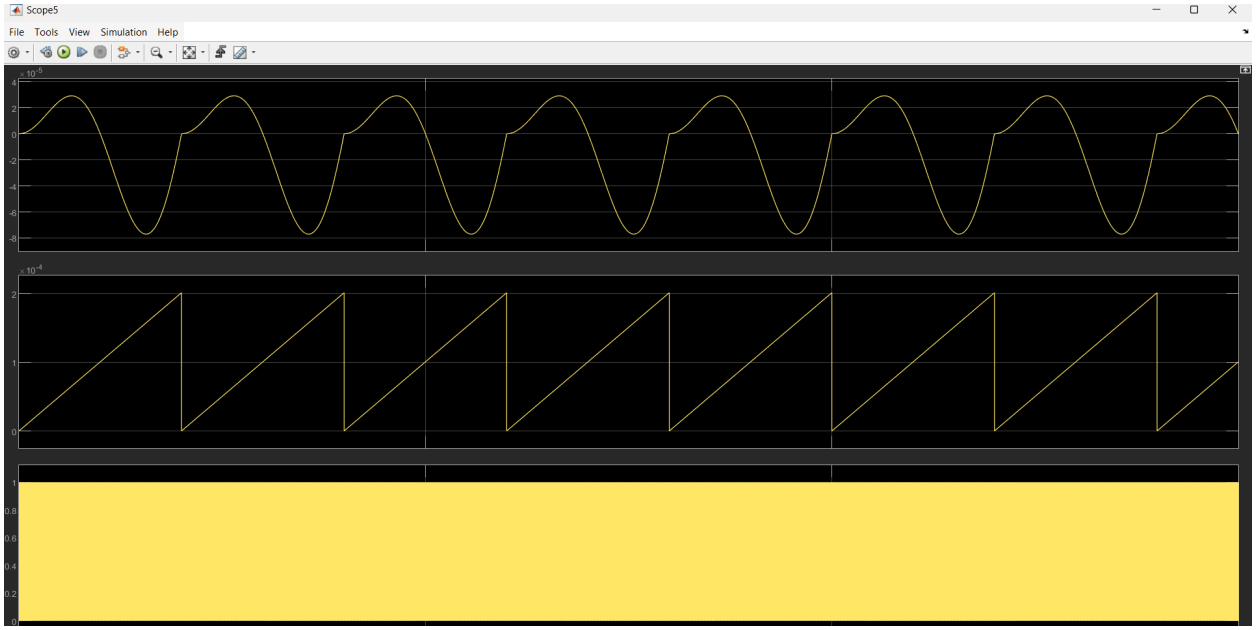
OBSERVATIONS



Grid voltage



Output of ZCD



Final Voltage Waveform Obtained from The process

LIMITATIONS AND FUTURE WORK

Limitations:

1. Accuracy Under Extreme Conditions: While the proposed FLL performs well under heavily distorted grid conditions with 26.4% THD, its performance under even more extreme conditions (higher THD levels or other types of disturbances) is not discussed. Limitations may arise when facing such extreme conditions.

2. Limited Validation:Although experimental validation is mentioned using an FPGA controller in the laboratory, the extent of this validation is not fully detailed. Further validation across a range of real-world scenarios and grid conditions may be necessary to assess its robustness.

3. Applicability to Three-Phase Systems:The abstract specifically mentions single-phase grid-connected systems. Extending the proposed FLL to three-phase systems may introduce additional challenges and complexities that need to be addressed.

4. Computational Resources:While the implementation is said to have less computational overhead, the specific computational resources required, especially in terms of hardware or

processor capabilities, are not specified. This could be a limitation, especially for resource-constrained applications.

Future Aspects:

1. Enhanced Robustness: Future work could focus on further enhancing the robustness of the FLL algorithm to handle a wider range of grid disturbances and conditions. This could involve refining the algorithm to improve accuracy and reliability under various scenarios.

2. Adaptability and Flexibility: Developing adaptive or self-tuning features within the FLL algorithm could enable it to automatically adjust its parameters based on the prevailing grid conditions. This would enhance its adaptability and performance in dynamic grid environments.

3. Extension to Three-Phase Systems: Investigating methods to extend the proposed FLL algorithm to three-phase grid-connected systems would broaden its applicability and usefulness in practical applications.

4. Real-World Deployment: Further research could focus on the practical deployment of the proposed FLL algorithm in real-world grid-connected systems. This would involve testing and validation in diverse grid environments to ensure its effectiveness and reliability in actual operating conditions.

5. Integration with Control Strategies: Integrating the FLL algorithm with advanced control strategies for grid-connected converters could lead to more efficient and intelligent power management solutions. This could involve incorporating predictive control or advanced filtering techniques to further enhance performance.

6. Standardization and Industry Adoption: Standardizing the implementation and performance criteria of FLL algorithms could facilitate their widespread adoption in the industry. Collaborations with standardization bodies and industry stakeholders could help establish guidelines and best practices for the deployment of FLL algorithms in grid-connected systems.