IEEE 2015-2016 PROJECT CAPTION –VLSI

Sl.No	PROJECT CAPTION
TNIVI1	A Mixed Decimation MDF Architecture For Radix-2k Parallel FFT
TNIVI2	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based On Multi Level Conditional Probability
TNIVI3	Comment on "High Speed Parallel Decimal Multiplication With Redundant Internal Encoding
TNIVI4	Low-Power Pulse-Triggered Flip-Flop Design Based on A Signal Feed-Through Scheme
TNIVI5	Adaptive Iterative Decoding for Expending the Convergence of Unary Error Correction Code
TNIVI6	Cost-Effective Robustness in Clock Networks Using Near Tree Structures
TNIVI7	Low Delay Single Symbol Error Correction Based on Reed Solomon Codes
TNIVI8	Stopping Set Elimination by Parity–Check Matrix Extension Via Integer Linear Programming
TNIVI9	Design of A High-Throughput QC-LDPC Decoder With TDMP Scheduling
TNIVI10	Resonator Voltage Predication in Microwave Band Pass Filter
TNIVI11	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability
TNIVI12	Design Flow for Flip-Flop Grouping in Data-Driven Clock Gating
TNIVI13	A Low Power Linear Phase Programmable Long Delay Circuit
TNIVI14	VLSI Implementation of an Adaptive Edge-Enhanced Color Interpolation Processor for Real-Time Video Applications
TNIVI15	Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation
TNIVI16	Efficient FPGA and ASIC Realizations of DA-Based Reconfigurable FIR Digital Filter

TNIVI17	An Efficient VLSI Architecture of A Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi Standard DUC
TNIVI18	Low Power FSK Receiver Using an Oscillator-Based Injection-Locked Frequency Divider
TNIVI19	Low-Power High-Throughput LDPC Decoder Using Non-Refresh Embedded DRAM
TNIVI20	SIFT Hardware Implementation for Real-Time Image Features Extraction
TNIVI21	An Efficient Denoising Architecture for Removal of Impulse Noise in Image
TNIVI22	Modeling, Control and Implementation of DC-DC Converter for Variable Frequency Operation
TNIVI23	An FPGA-Based Fully Synchronized Design of a bilateral Filter for Real-Time Image Denoising
TNIVI24	Modified Gradient Search for Level Set Based Image Segmentation FPGA Implementation of Pipelined Architecture for SPIHT Algorithm
TNIVI25	Shadow Removal for Background Subtraction Using Illumination Invariant Measures
TNIVI26	Segmentation and Location of Abnormality in Brain MR Images Using Distributed Estimation
TNIVI27	Background Subtraction Based on Threshold Detection Using Modified K-Means Algorithm
TNIVI28	16 Bit Microprocessors Design and Simulation in VHDL
TNIVI29	Real Time Background Generation and Foreground Object Segmentation for High Definition Color Video Stream in FPGA Device
TNIVI30	VLSI Implementation of A Low-Cost High Quality Image Scaling Processor
TNIVI31	VLSI Implementation of an Adaptive Edge-Enhanced Image Scalar for Real-Time Multimedia Applications
TNIVI32	A Pipeline VLSI Architecture for Fast Computation of 2D Discrete Wavelet Transform
TNIVI33	Design and Implementation of A Pipelined Data Path for High-Speed Face Detection Using FPGA