

No E-Mail submissions will be accepted.  
Submission formats and file naming:

File name: firstName\_lastName\_lab\_2

File format: pdf or MS Word format

e.g. Jim\_Carrey\_lab\_2.pdf

**1.** What are the two main functions of an operating system?

**2.** Which of the following instructions should be allowed only in kernel mode (select 3 items)?

(a) Disable all interrupts.

(b) Read the time-of-day clock.

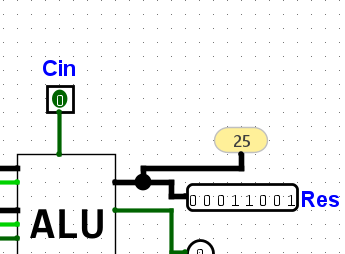
(c) Set the time-of-day clock.

(d) Change the memory map.

**3.** Obtain the number of cache lines and cache sets for the **L1I** Cache given below?

****

**4.** Assuming A = 12 and B= 15, and considering the control signals, given in the following table, obtain the output (function) of ALU for each case (attach a screenshot of your Logisim file for each case) e.g.



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **ALU (list of operations)** | | | | | | | |
| **F0** | **F1** | **ENA** | **ENB** | **INVA** | **INC** | **Output(Function)** | **Screenshot** |
| **1** | **1** | **1** | **1** | **1** | **1** |  |  |
| **1** | **1** | **1** | **0** | **1** | **1** |  |  |
| **1** | **1** | **0** | **0** | **1** | **0** |  |  |

**5.** Given the following information:

|  |  |
| --- | --- |
| Memory | 4 GiB |
| L3 cache | 8 MiB |
| Cache line size | 128 B |
| Method | Direct mapping |
| Addressing mode | Byte addressable |

Answer the following question:

1) How many bits are used for addressing each byte of memory?

2) How many bits are used for addressing each byte of the L3 cache?

3) How many bits are required to address each byte within a cache line?

4) How many cache lines are present in the memory?

5) How many cache lines are present in the L3 cache?

Complete the following table

|  |  |  |  |
| --- | --- | --- | --- |
|  | Provide the result in hexadecimal format | | |
| Memory Address | Tag | Memory Index (MI) | Cache Index (CI) |
| 0xA0B12FC0 |  |  |  |
| 0x100EEFF0 |  |  |  |

1 KiB = 210

1 MiB = 220

1 GiB = 230