ECGR 3131 Project 1: Common Emitter amplifier

Joshua Ayers

Abstract -

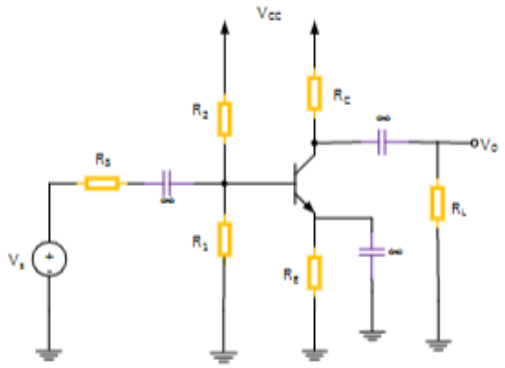
The purpose of this project is to design, simulate and implement a common emitter amplifier That matches a predefined set of operating parameters. The mathematical model for this emitter has been derived from sets of equations, The simulation will be made in Multisim and will provide theoretical operating performance and a real common emitter amplifier will be created on a breadboard using a fairchild Q2N3904 bipolar junction transistor and various other basic circuit elements.

I. Introduction

This common emitter amplifier must have a gain of 150 $\frac{V}{V}$. A minimum of 12 volts peak to peak output and no more than 200 milliwatts overall power draw. We are required to have a V_CC of 18V. We need a load resistor of 5kΩ

The standard model of common emitter amplifier is shown below:

Common emitter amplifier:



II. DC modeling

- □:

The first Step of the project was to determine □ using the information provided in the 2N3904 data sheet however the information that was required to was not included on the data sheet thus is assumed to be 100.

-Other assumed values

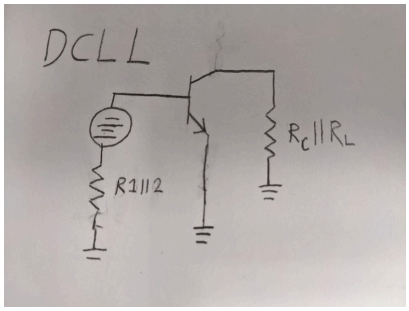
Similar assumptions were made for V_T where $V_T = 25mV$ and I_B << relative to I_C and I_E. V_{be} is assumed to be 0.7 volts.

-Finding the DC load line

The first Step in determining DCLL is finding the DC equivalent circuit. To do this the capacitors are removed and by connection the AC voltage source The load resistor (R_L) and the lead to ground on the emitter side are removed

from the circuit. Second The voltage V_{BB} is calculated by transforming the DC rail and base side ground into a resistor whose impedance is the combination of R_1 and R_2 in parallel and single DC voltage source That is equal to The voltage across R_1 in the original circuit.

$$V_{BB} = V_{CC} * \frac{R_1}{R_1+R_2}$$



From first principles It is known that $I_E = I_C + I_B$. Because I_B is known to be very small It was assumed that $I_E \approx I_C$.

-DC Q points:

III. AC modeling

To determine the characteristic AC behavior The common emitter amplifier was modeled using the pie model. In this model the capacitors were replaced with shorts and the DC voltage sources were replaced with grounds. The bipolar junction transistor was replaced with a pair of parallel grounded branches as shown in the figure below:

Epi in the figure is equivalent to The impedance of the thermally induced voltage of the line and is represented by the equation VT which is assumed to be 25 millivolts divided by the I_{CQ} which was determined in DC analysis.

On the v outside of the separate parallel branches is a current dependent current source that is equivalent to beta times the current across Rpi

-Determining Gain

Because voltage drop is the same across resistors in parallel it is deduced that:

$V_{in} = i_b * r_\pi$

$r_\pi = \frac{25mV}{18mA}$

Thus

$i_b = \frac{V_{in}}{r_\pi}$

Because $V_{out} = -i_b * \beta * R_L$

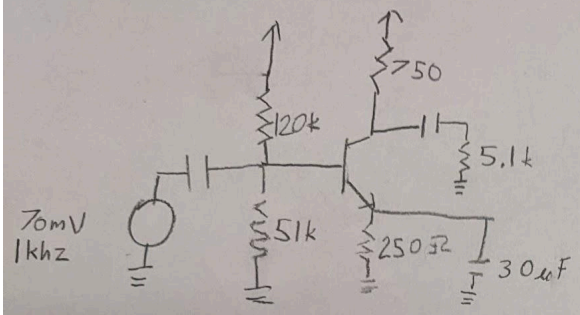
We can represent V_{out} in terms of V_{in}.

$V_{out} = -(\frac{V_{in}}{R_\pi}) * \beta * R_L$

$A_v = \frac{V_{out}}{V_{in}} = -\frac{\beta * R_L}{r_\pi} =$

$$I_C = I_B * gain$$

$$V_{BB} = 18 \cdot \frac{51k}{171k} = 5.36844$$

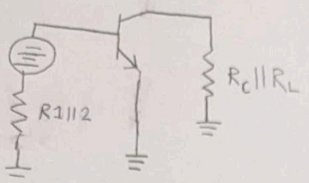


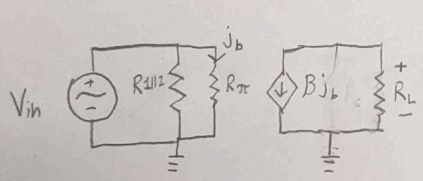
$$V_{cc} = I_c(R_c + R_E) + V_{CE}$$

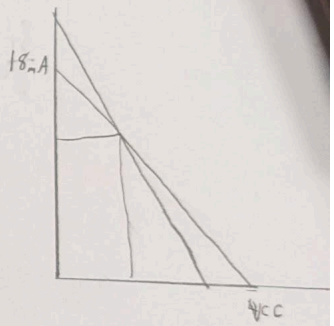
$$I_{CQ} = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta} + R_E} = \frac{4.6684V}{\frac{R_B}{100} + 250} \approx 18.7$$

V

DCLL



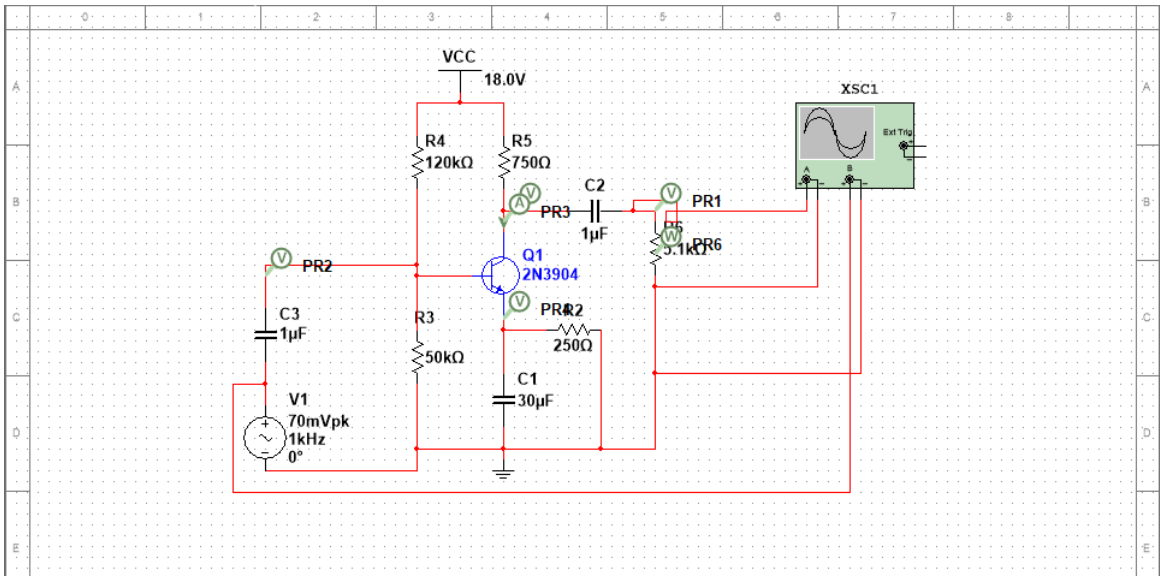




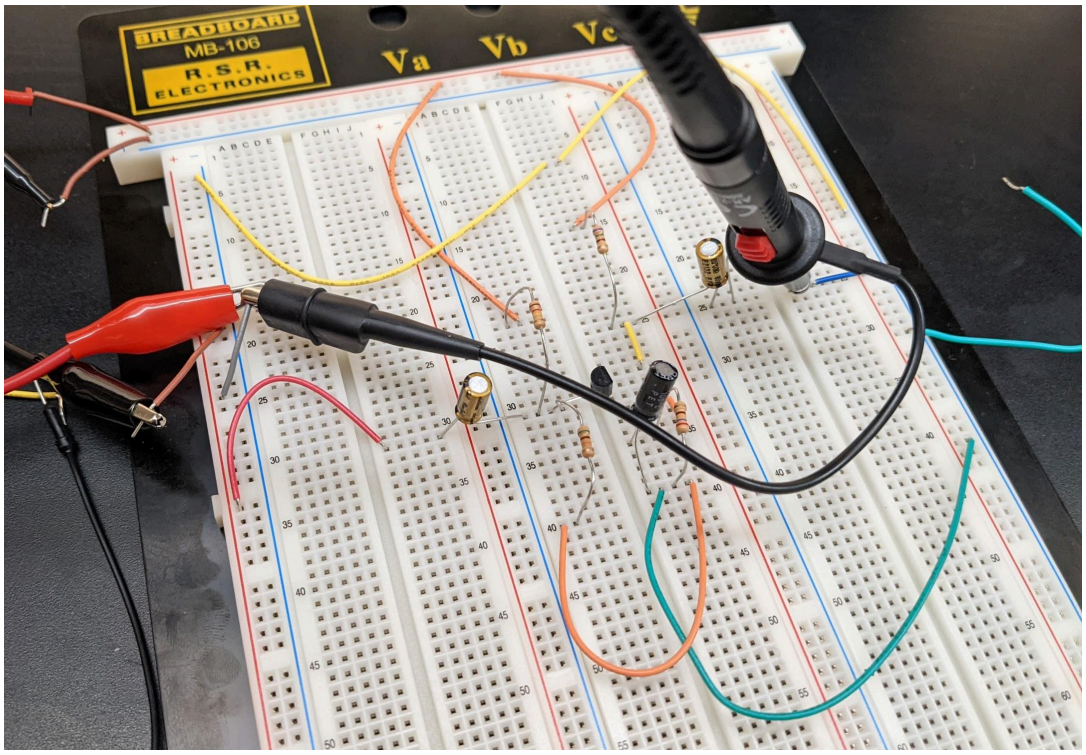
Step 2 - simulation

-Building the model

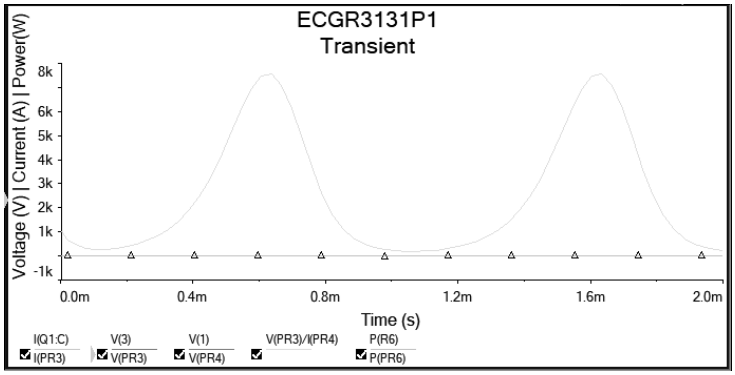
Model was constructed in Multisim



While clipping was expected with such high values for R4 and R3 this did not prove to be an issue.



Below a graph of the simulations transient response.



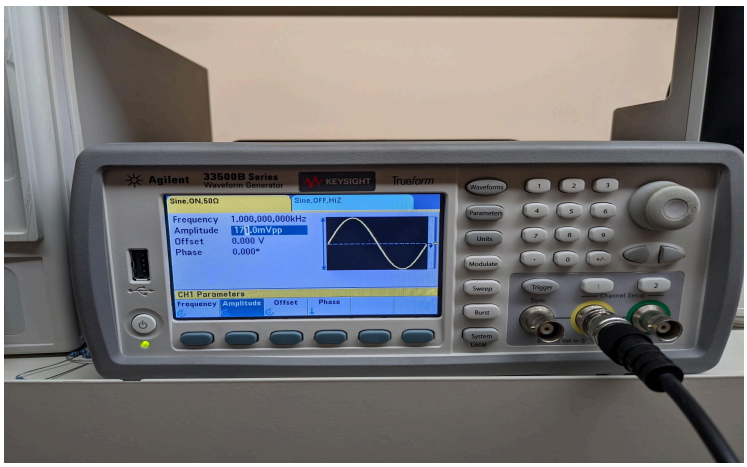
Step 3 - implementation

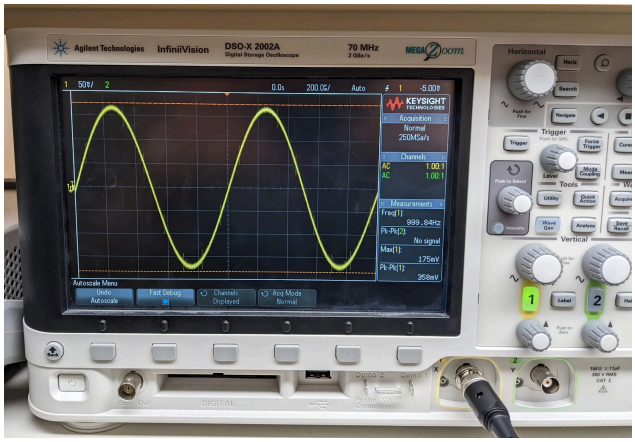
Constricting the circuit

The circuit below was constructed using a 2 1μF capacitors,

Testing the circuit:

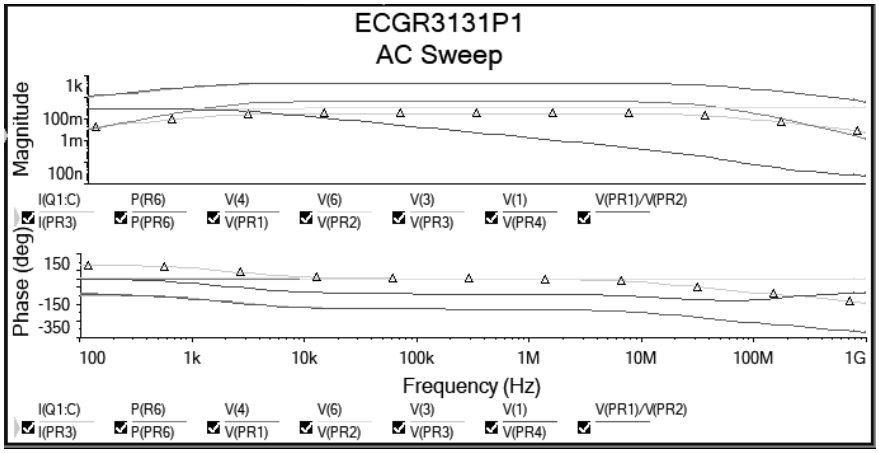
The below oscilloscope





Results:

Note: the Multisim model was produced before the hand calculations were performed this ment that there was practically no error between the hand calculations and the



Bandwidth:

Areas of improvement:

The circuit could be improved a number of ways notably the actual function of the physical amplifier. The amplifier provided a gain of approximately 3 rather than the intended gain of 150. This issue probably could have been resolved by a rebuild of the circuit if there was more time.

Conclusion

What value does the swing
Things that can be improved

References

4. Results to Include

The plots and tables previously asked for during the tutorial should be included in the results section. Discussion about what is happening with the plot or table should be included. The following about the frequency response should also be included in the results section for both simulated and measured.

Range of frequency of operation: _____ Hz to _____ Hz
3dB Bandwidth of the circuit: _____ Hz
Peak Gain Frequency: _____ Hz

5. Conclusion

A discussion of the circuit and how it performed should be included in the conclusion. The following questions should also be addressed:

Why is there a difference between the hand calculated gain, the simulated gain, and the measured gain?

At what value does the swing become unsymmetrical and why is that?

How did you approach solving this design problem (remember to write in passive voice)?