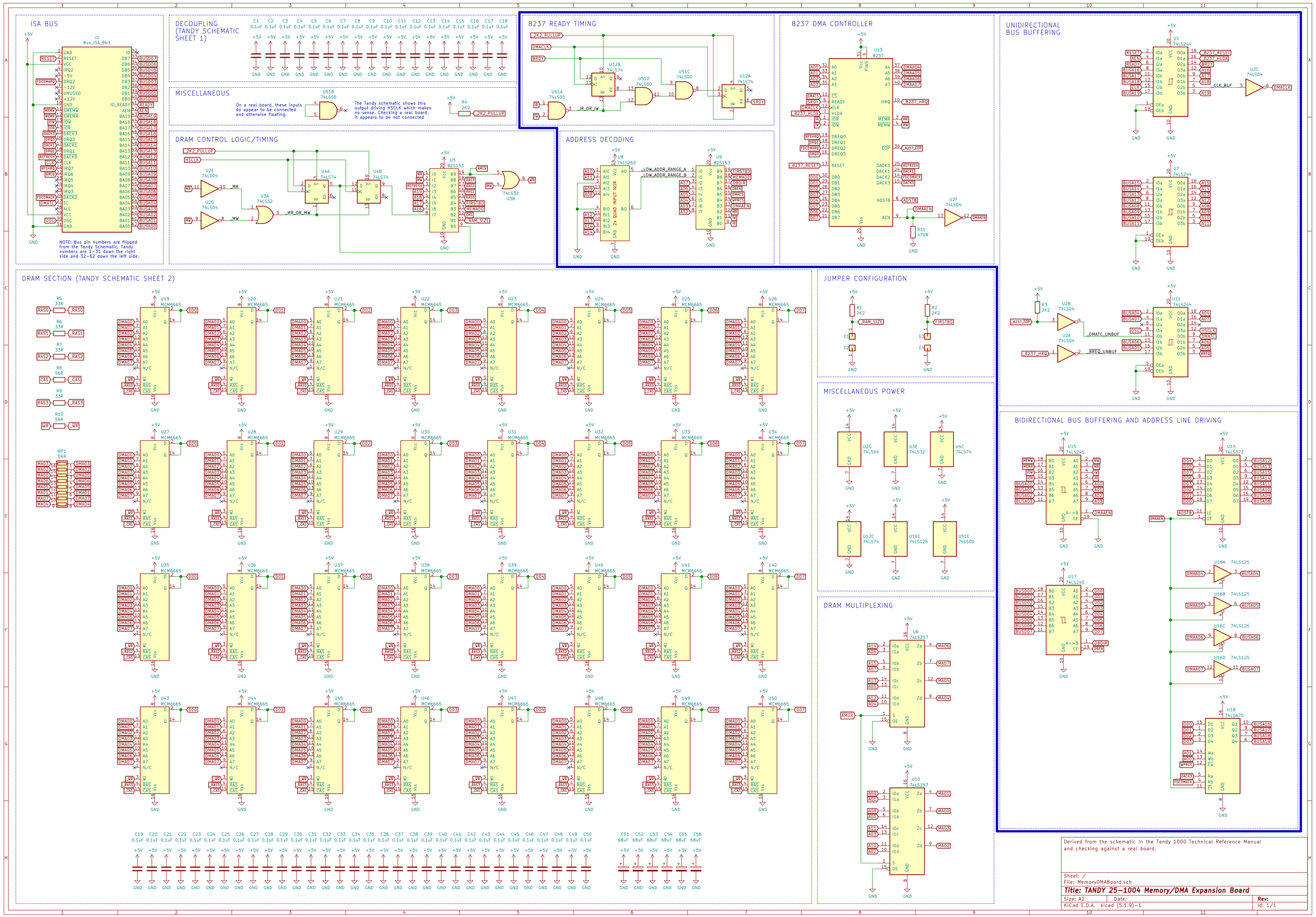
ISA BUS
J1
Bus_ISA_8bit
NOTE: Bus pin numbers are flipped from the Tandy Schematic. Tandy numbers are 1–31 down the right side and 32–62 down the left side.
DECOUPLING (TANDY SCHEMATIC SHEET 1)
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
0.1uF
MISCELLANEOUS
U51B 74LS00
On a real board, these inputs do appear to be connected and otherwise floating.
The Tandy schematic shows this output driving HSCLK which makes no sense. Checking a real board, it appears to be not connected
R4 2K2
_2K2_PULLUP
DRAM CONTROL LOGIC/TIMING
U2E 74LS04
U2D 74LS04
U3A 74LS32
U4A 74LS74
U4B 74LS74
U5 825153
74LS32 U3B
_MR
_MW
_MR_OR_MW
_RAS3
_RAS2
_RAS1
_RAS0
_FIRSTBD
_MEMADD
_RAM_SIZE
_AMUX
8237 READY TIMING
U12B 74LS74
U51D 74LS00
U51A 74LS00
U12A 74LS74
_IR_OR_IW
_SRDY
8237 DMA CONTROLLER
U13 8237
_DMAAD4
_DMAAD5
_DMAAD6
_DMAAD7
_8237_HRQ
_8237_EOP
_DMAAEN
R11 470R
ADDRESS DECODING
U8 74LS260
2x QUAD INPUT NOR
U9 825153
_LOW_ADDR_RANGE_A
_LOW_ADDR_RANGE_B
_DBDIR
_DBEN
UNIDIRECTIONAL BUS BUFFERING
U1 74LS244
U2C 74LS04
_CLK_BUF
U7 74LS244
U2F 74LS04
U11 74LS244
U2B 74LS04
U2A 74LS04
_DMATC_UNBUF
_BREQ_UNBUF
DRAM SECTION (TANDY SCHEMATIC SHEET 2)
MCM6665
JUMPER CONFIGURATION
R1 2K2
R2 2K2
MISCELLANEOUS POWER
U2G 74LS04
U3E 74LS32
U4C 74LS74
U12C 74LS74
U16E 74LS125
U51E 74LS00
DRAM MULTIPLEXING
U6 74LS257
U10 74LS257
BIDIRECTIONAL BUS BUFFERING AND ADDRESS LINE DRIVING
U15 74LS245
U14 74LS373
U17 74LS245
U16A 74LS125
U16B 74LS125
U16C 74LS125
U16D 74LS125
U18 74LS670
Derived from the schematic in the Tandy 1000 Technical Reference Manual and checking against a real board.
Sheet: /
File: MemoryDMABoard.sch
Title: TANDY 25-1004 Memory/DMA Expansion Board
Size: A2
Date:
Rev:
KiCad E.D.A. kicad (5.1.9)-1
Id: 1/1