SCL/VDG/VDG/Readme_PDK_SCLV3/2023/12/22

README DOCUMENT
OF
SCL 180nm PDK
VERSION 3.0
(SCLPDK_V3.0)

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सेमी-कंडक्टर लेबोरेटरी
सेक्टर 72, एस.ए.एस. नगर
चंडीगढ़, पंजाब-160071
Semi-Conductor Laboratory
Sector 72, S.A.S. Nagar
Chandigarh, Punjab-160071

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1. Introduction

This document covers all the deliverables present in SCL 180 nm PDK, SCLPDK_V3.0. The deliverables inside this database consists of Process Design Kit (PDK), Standard cell library, IO library and memory cuts and various related documents. This document explains various aspects of PDK usage like installation of PDK, list of legal devices available, illegal combinations of devices which should not be used together, recommended design flow and related aspects.

It is strongly recommended to go through this Readme document and other Important documents (Refer to Section 4.6) thoroughly before starting your design and submitting GDSII to SCL foundry.

2. List of Legal Devices

User to make sure that only Legal devices with valid legal combinations must be used in their design.
Note: DR Manual contains information on extra devices which are not part of legal device list and these devices need to be ignored.

S. No	Device Name	Type	Device Description	SPICE Name	P-cell	LVS
1	MOSFETs	1.8V,Svt	1.8V SVt NMOS Transistor	n18	nmos_18	N
2	MOSFETs	1.8V,Svt	1.8V SVt PMOS Transistor	p18	pmos_18	P
3	MOSFETs	1.8V,Svt	1.8V SVt NMOS Transistor in IPW	n18	nmos_18_iso	N_ISO
4	MOSFETs	1.8V,Hvt-Low Leakage	1.8V HVt NMOS transistor for Low Leakage	n18hvtb3	n18hvt	N18HVT
5	MOSFETs	1.8V,Hvt-Low Leakage	1.8V HVt PMOS transistor for Low leakage	p18hvtb3	p18hvt	P18HVT
6	MOSFETs	1.8V,Hvt-Low Leakage	1.8V HVt NMOS transistor for Low leakage in IPW	n18hvtb3	n18hvt_iso	N18HVT_ISO
7	MOSFETs	1.8V,Native	1.8V NMOS Native Transistor	natlv	nmos_native	NA
8	MOSFETs	3.3V,Svt	3.3V SVt NMOS Transistor	nhv	nmos_33	NH
9	MOSFETs	3.3V,Svt	3.3V SVt PMOS Transistor	phv	pmos_33	PH
10	MOSFETs	3.3V,Svt	3.3V SVt NMOS Transistor in IPW	nhv	nmos_33_iso	NH_ISO

11	MOSFETs	3.3V,Native	3.3V NMOS Native Transistor	nathv	nmos_native_33	NB
12	MOSFETs	5VSvt	5V SVt NMOS transistor	n5v	nmos_5V	N5
13	MOSFETs	5VSvt	5V SVt PMOS transistor	p5v	pmos_5V	P5
14	MOSFETs	5VSvt	5V SVt NMOS transistor in IPW	n5v	nmos_5V_iso	N5_ISO
15	MOSFETs	5V,Native	5V NMOS Native Transistor	nat5v	nmos_native_5	NB5
16	BJT	1.8V, BJT	1.8V Vertical PNP 10um x 10um BJT	vd10	vpnp18_10	VD10
17	BJT	1.8V, BJT	1.8V Vertical PNP 5um x 5um BJT	vd5	vpnp18_5	VD5
18	BJT	1.8V, BJT	1.8V Vertical PNP 2um x 2um BJT	vd2	vpnp18_2	VD
19	BJT	1.8/3.3/5V, BJT	1.8/3.3/5V Vertical NPN 5um x 5um BJT	vdn5	vnpn18_5	VDN5
20	BJT	3.3/5V, BJT	3.3/5 Vertical PNP 10um x 10um BJT	vd10	vpnp33_10	VH10
21	BJT	3.3/5V, BJT	3.3/5 Vertical PNP 5um x 5um BJT	vd5	vpnp33_5	VH5
22	BJT	3.3/5V, BJT	3.3/5 Vertical PNP 2um x 2um BJT	vd2	vpnp33_2	VH
23	Capacitors	1.8V, Acc.Capacitor	1.8V Scalable Accumulation capacitor N+ Gate/ NW, 2 terminals	nwcap2t	cnwnmos_thn2t	CL
24	Capacitors	1.8V, Acc.Capacitor	1.8V Scalable Accumulation capacitor N+ Gate/NW)3 terminals	nwcap3t	cnwnmos_thn3t	CL3
25	Capacitors	3.3V, Acc.Capacitor	3.3V Scalable Accumulation capacitor, N+ Gate/NW,2 terminals)	nwcaph2t	cnwnmos_thk2t	CH
26	Capacitors	3.3V, Acc.Capacitor	3.3V Scalable Accumulation capacitor, N+ Gate/NW,3 terminals	nwcaph3t	cnwnmos_thk3t	CH3
27	Capacitors	5V, Acc.Capacitor	5V Accumulation capacitor, N+ Gate/NW.	ch53t	ch53t	CH53T
28	Capacitors	MIM cap	MIM Capacitor, 1fF/um2 capacitor	cmim_sq	cmim_sq	CB
29	Capacitors	MFC in USG	M15 USG 2T MFC	usgcm52t	usgcm52t	usgcm52t
30	Capacitors	MFC in USG	M13 USG 2T MFC	usgcm32t	usgcm32t	usgcm32t
31	Capacitors	MFC in USG	M15 USG 3T MFC	usgcm53t	usgcm53t	usgcm53t
32	Capacitors	MFC in USG	M13 USG 3T MFC	usgcm33t	usgcm33t	usgcm33t
33	Resistors	poly resistor	HIPO-1k High Ohmic P-type Poly w/o salicide 2 terminal resistor	rphpoly2t	rphpoly2t	RC
34	Resistors	poly resistor	HIPO-1k High Ohmic P-type Poly w/o salicide 3 terminal resistor	rphpoly3t	rphpoly3t	RC3

35	Resistors	poly resistor	2k High Ohmic P-type Poly w/o salicide 2 terminal resistor	mr22t	mr22t	MR22T
36	Resistors	poly resistor	2k High Ohmic P-type Poly w/o salicide 3 terminal resistor	mr23t	mr23t	MR23T
37	Resistors	poly resistor	NMOPO–N-type Poly w/o salicide 2 terminals resistor	rnmpoly2t	rnmpoly2t	RE
38	Resistors	poly resistor	NMOPO–N-type Poly w/o salicide 3 terminals resistor	rnmpoly3t	rnmpoly3t	RE3
39	Resistors	poly resistor	PMOPO–P-type Poly w/o salicide 2 terminals resistor	rpmpoly2t	rpmpoly2t	RD
40	Resistors	poly resistor	PMOPO–P-type Poly w/o salicide 3 terminals resistor	rpmpoly3t	rpmpoly3t	RD3
41	Resistors	poly resistor	N-poly salicide 2 terminals resistor	rnlpoly2t	rnlpoly2t	RH
42	Resistors	poly resistor	N-poly salicide 3 terminals resistor	rnlpoly3t	rnlpoly3t	RH3
43	Resistors	poly resistor	P-poly salicide 2 terminals resistor	rplpoly2t	rplpoly2t	RG
44	Resistors	poly resistor	P-poly salicide 3 terminals resistor	rplpoly3t	rplpoly3t	RG3
45	Resistors	diffusion resistor	N+ AA Diffusion w/o salicide 2 terminals resistor	rnplus2t	rnplus2t	RB
46	Resistors	diffusion resistor	N+ AA Diffusion w/o salicide 3 terminals resistor,	rnplus3t	rnplus3t	RB3
47	Resistors	diffusion resistor	P+ AA Diffusion w/o salicide 2 terminals resistor	rpplus2t	rpplus2t	RA
48	Resistors	diffusion resistor	P+ AA Diffusion w/o salicide 3 terminals resistor	rpplus3t	rpplus3t	RA3
49	Resistors	diffusion resistor	N+ AA Diffusion salicide 2 terminals resistor	nasr2t	rnplus_sal2t	RK
50	Resistors	diffusion resistor	N+ AA Diffusion salicide 3 terminals resistor	nasr3t	rnplus_sal3t	RK3
51	Resistors	diffusion resistor	P+ AA Diffusion salicide 2 terminals resistor	pasr2t	rpplus_sal2t	RM
52	Resistors	diffusion resistor	P+ AA Diffusion salicide 3 terminals resistor	pasr3t	rpplus_sal3t	RM3
53	Resistors	well resistor	N-Well under AA 2 terminals resistor	rnwellaa2t	rnwell_AA2t	RF
54	Resistors	well resistor	N-Well under AA 3 terminals resistor	rnwellaa3t	rnwell_AA3t	RF3

55	Resistors	well resistor	N-Well under STI 2 terminals resistor	rnwellsti2t	rnwell_STI2t	RW
56	Resistors	well resistor	N-Well under STI 3 terminals resistor	rnwellsti3t	rnwell_STI3t	RW3
57	Resistors	Metal resistor	M1 resistor	rm1	rm1	R1
58	Resistors	Metal resistor	M2 resistor	rm2	rm2	R2
59	Resistors	Metal resistor	M3 resistor	rm3	rm3	R3
60	Resistors	Metal resistor	M4 resistor	rm4	rm4	R4
61	Resistors	Metal resistor	M5 resistor	rm5	rm5	R5
62	Resistors	Metal resistor	ML resistor	rml	rmL	RL
63	Diodes	1.8V diode	1.8V N+ /Pwell Diode,	dn18	ndio_sal	DN
64	Diodes	1.8V diode	1.8V P+ /Nwell Diode	dp18	pdio_sal	DP
65	Diodes	diode	3.3/5V N+ /Pwell Diode	dnh	ndio_33	N3
66	Diodes	diode	3.3/5V P+ /Nwell Diode	dph	pdio_33	P3
67	Diodes	1.8V diode	1.8V Nwell/Psub Diode	dnwell	nwldio	DW
68	Diodes	diode	3.3/5V Nwell/Psub Diode	dnwell33	nwldio_33	W3
69	Diodes	diode	1.8/3.3/5V Deep-N-Well/Psub Diode	ddwnps18	ddwnps18	DDWNPS18
70	Diodes	diode	1.8/3.3/5V Isolated-P-Well / Deep N-Well diode	ddwnpw18	ddwnpw18	DDWNPW18
71	Diodes	diode	N+ in 5V Pwell diode	dn50	dn50	DN50
72	Diodes	diode	P+ in 5V Nwell diode	dp50	dp50	DP50

Table 2-1 List of Legal Devices

3. Illegal Combinations

Few available devices should not be used together and user must carefully choose the combination of devices being used in design. Table below describes the illegal combination of devices which should not be used.

Note: If any such combination of devices is found in design, it will lead to rejection of GDSII.

Combinations not allowed in the process:

1. 3.3V and 5V process options are mutually exclusive (allowed combinations are : 1.8V/3.3V, 1. 8V/5V,1.8V only, 3.3V only, 5V only)
2. Triple Vt combination for 1.8V transistors (SVt, HVt, LVt together) is not allowed. Only allowed combinations are (SVt +HVt) or (SVt +LVt) together.
3. Only one type of MIM device is allowed in single or stacked MIM option. Either 1fF, or 1.7fF, or 2.8fF can be used in one ASIC.
4. No two thick last metals allowed in the process. Only one Last Metal (either ML or MT or MT3) is allowed in ASIC. MT3 and MF terms are used interchangeably.
5. ML & MTOP are used interchangeably in the documentation.

Note: Only legal device list to be followed for selecting any process option and not to be confused with extra information provided in any of the documents.

Below figure represents the possible FEOL and BEOL combinations. To be chosen carefully for device and process compatibility. For any query, please consult SCL process/ design team focal for clarifications.

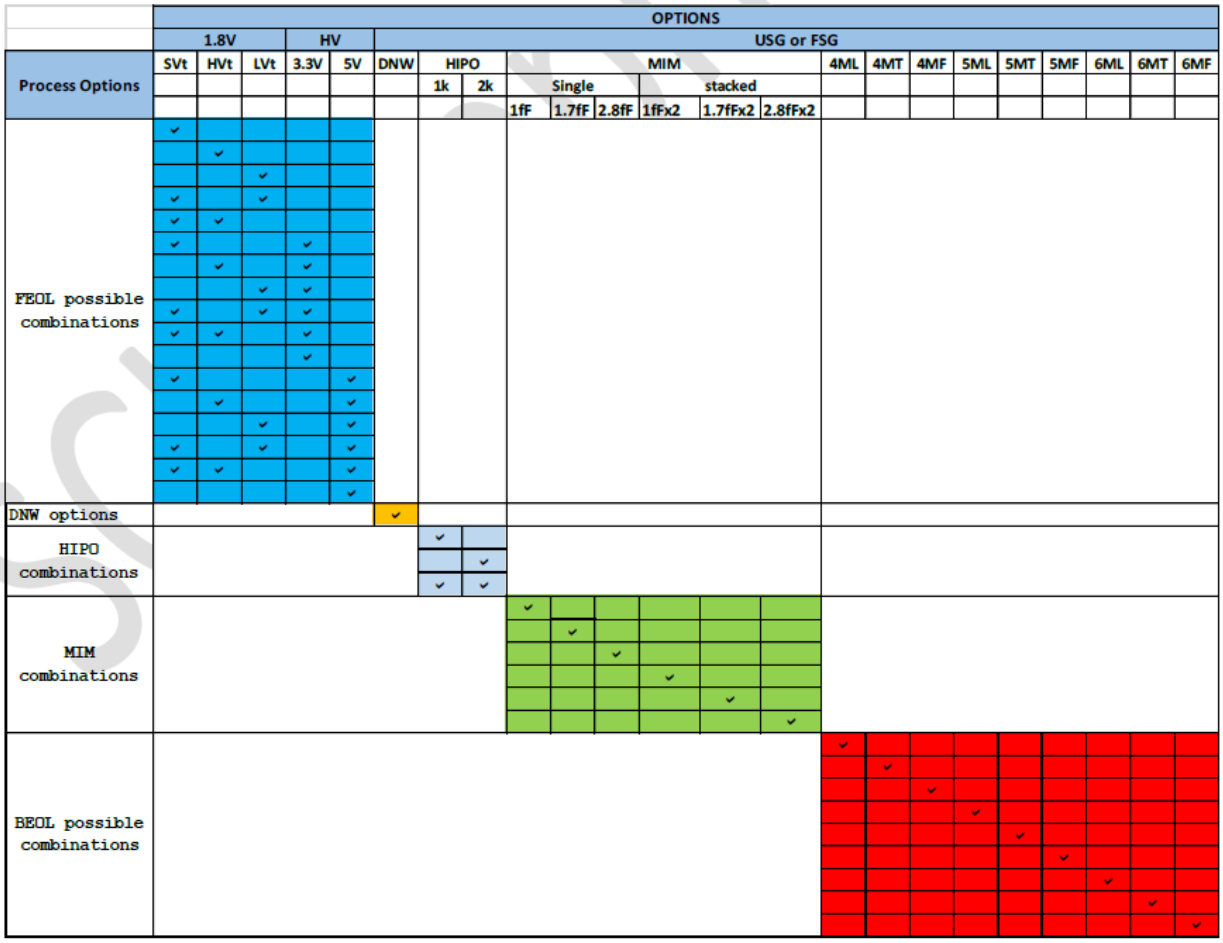

Figure 3-1 Illegal Combinations

4. SCL Process Design Kit (SCLPDK_V3.0) Deliverables

4.1 PDK

Home Directory path : ~/scl180/pdk/cdns/sclpdk_v3/HOTCODE

This folder contains PDK compatible with Cadence Virtuoso EDA tool.

Section 5 of this document contains PDK installation guide. Designer has to follow the instructions with proper selection of PDK flavor according to design requirement.

After installation, PDK will be enabled with respective Pcells, DRC, LVS,PEX getting automatically loaded in browser.

Model File Related :

Home Directory path :
~/scl180/pdk/cdns/sclpdk_v3/HOTCODE,models/ts18scl/v2.0/hspice

Note: Kindly make sure that all files under this directory are of .lib extension. If not please change the files to .lib extension.

1) The SPICE models for the following devices are provided in the model library file (ts18sl_scl.lib). This file contains-

- 1.8V NMOS/PMOS (Standard Vt only - n18,p18)
- 3.3V NMOS/PMOS (nhv,phv)
- Native Mosfets (1.8V NMOS and 3.3V NMOS - natlv,nathv)
- Diodes for 1.8V & 3.3V [dn18,dp18,dnh,dph,ddwnps18 (D-NWell/Psub), ddwnpw18 (I-Pwell/D-NWell) ,dnwell ,dnwell33]
- Resistors : [nasr2t, pasr2t, rm1, rm2, rm3, rm4, rm5, rml, rmt, rnmpoly2t, rnplus2t, rnwellaa2t, rnwellsti2t, rphpoly2t, rplpoly2t, rpmpoly2t, rpplus2t, rnlpoly2t]
  [nasr3t, pasr3t, rnlpoly3t, rnmpoly3t, rnplus3t, rnwellaa3t, rnwellsti3t, rphpoly3t, rplpoly3t, rpmpoly3t, rpplus3t]
- Accumulation Capacitors [nwcap2t, nwcap3t, nwcaph2t, nwcaph3t, ch53t] (Please note that 5V accumulation capacitors-'ch53t' has been added here itslef)
- MIM Capacitor [cmim_sq] (Only 1 type of MiM capacitor-1 fF/um2 density is being released by SCL in December 2022)

2) The SPICE models for the following devices are provided in the new model library file (ts18sl_scl_2019.lib). This file contains

- 1.8V High Vt NMOS/PMOS (n18hvtb3,p18hvtb3) -LOW LEAKAGE-
- 5V NMOS/PMOS (n5v,p5v)
- Native Mosfets (5V NMOS nath5v)
- BJTs (vd10,vd5,vd2,vdn5)
- Diodes for 5V- n&p type (dn50,dp50)
- Resistors (mr22t, mr23t) - 2k HIPO resistor only
- Metal Fringe Capacitors (usgcm32t,usgcm33t,usgcm52t,usgcm53t)

3) The files such as 'fet.lib' , 'fethv.lib' , 'bjt.lib' , 'accap.lib' ,'mimcap.lib' ,'mfc.lib' , 'res.lib' ,'diode.lib' , 'nat.lib' have been modified suitably to incorporate the above distribution of models in the two SPICE files- ts18sl_scl.lib & ts18sl_scl_2019.lib

4) The corner libraries for 5V NMOS, 5V PMOS, 5V Native NMOS, Accumulation capacitors, Diodes have been modified/renamed as per the above changes.

5) Designer can just include 'header.lib' and run the simulation.

6) For mismatch simulation of 1.8V and 3.3V MOSFETs, use the file 'ts18sl_scl_mat.lib'

4.2 IO Pad Library

Home Directory path : ~/scl180/iopad

CIO 150 Folder details: 1.8V Core and 1.8V IO

Sr No.	Folder Name	Contents in folder
1	**4M1L**	GDSII of I/O for 4Metal backend
	cdl	CDL Netlist of I/O pads for LVS
	Doc	Documents and application notes related to I/O pads
	lef	lef file
	liberty	Timing information of I/O
	milkyway	Milky way data base for ICC(Synosys) Tool
	Spc_netlist	Spice netlist with parasitcs
	symbol	Symbols of I/O pad
	Verilog	Verilog models for Simulation Library
2	**6M1L**	GDSII of I/O for 6Metal backend
	cdl	Netlist of I/O pads for LVS
	Doc	Documents and application notes related to I/O pads
	lef	lef file
	liberty	Timing information of I/O
	milkyway	Milky way data base for ICC(Synosys) Tool
	Spc_netlist	Spice netlist with parasitcs
	symbol	Symbols of I/O pad
	Verilog	Verilog models for Simulation Library

Table 4-1 CIO 150 Folder Details

CIO 250 Folder Details: 1.8VCore and 3.3V IO, 3.3VCore and 3.3V IO

Sr. No.	Folder Name	Contents in folder
1	**4M1L**	GDSII of I/O for 4Metal backend
	cdl	Netlist of I/O pads for LVS
	Doc	Documents and application notes related to I/O pads
	lef	lef file
	liberty	Timing information of I/O
	milkyway	Milky way data base for ICC(Synosys) Tool
	Spc_netlist	Spice netlist with parasitic
	symbol	Symbols of I/O pad
	Verilog	Verilog models for Simulation Library
2	**6M1L**	GDSII of I/O for 6Metal backend
	cdl	Netlist of I/O pads for LVS
	Doc	Documents and application notes related to I/O pads
	lef	lef file
	liberty	Timing information of I/O
	milkyway	Milky way data base for ICC(Synosys) Tool
	Spc_netlist	Spice netlist with parasitic
	symbol	Symbols of I/O pad
	Verilog	Verilog models for Simulation Library

Table 4-2 CIO 250 Folder Details

PIO520 Folder Details: 1.8V Core and 5V IO, 5V Core and 5V IO,
1.8V Core and 1.8V IO

Sr. No.	Folder Name	Contents in folder
1	**4M1L**	GDSII of I/O for 4 Metal backend
	cdl	Netlist of I/O pads for LVS
	lef	lef file
	doc	Documents and application notes related to I/O pads
	difi	Layout data of I/O pad
	spc	Spice netlist with parasitic
	Spc_simple	Spice netlist
	liberty	Liberty model of I/O Pad
	Verilog	Verilog models for Simulation Library
	db	.db files for 1.8V, 1.8V/5V and 5V only I/O
2	**6M1L**	**GDSII of I/O for 6 Metal backend**
	cdl	Netlist of I/O pads for LVS
	lef	lef file
	doc	Documents and application notes related to I/O pads
	difi	Layout data of I/O pad
	spc	Spice netlist with parasitic

	Spc_simple	Spice netlist
	liberty	Liberty model of I/O Pad
	Verilog	Verilog models for Simulation Library
	db	.db files for 1.8V, 1.8V/5V and 5V only I/O

Table 4-3 PIO 520 Folder Details

Summarized features of I/O library available at SCL

<table>
<tr><th></th><th>CIO150</th><th>CIO250</th><th>PIO520</th></tr>
<tr><td rowspan="3">Input /Output Voltage Range</td><td rowspan="3">1.65V to 1.95V IO and 1.62 to 1.98 Core side</td><td>2.7V to 3.6V
IO and core side</td><td>2.7V to 5.5V
IO and core side</td></tr>
<tr><td rowspan="2">2.7V to 3.6V
IO and 1.8V±10% core side ,
(1.8V/3.3V level shifter I/O pads Available)</td><td>2.7V to 5.5V
IO and 1.8V±10% core side
(1.8V/5.0V level shifter I/O pads Available)</td></tr>
<tr><td>1.8V±10%
I/O and core side</td></tr>
<tr><td>Maximum Bus Voltage swing support</td><td>0 to 1.98V</td><td>0 to 3.6V</td><td>0 to 5.5V</td></tr>
<tr><td>I/O size</td><td>Width=65um,
Height=250um</td><td>Width=65um,
Height=250um</td><td>Width=100um,
Height=310um</td></tr>
</table>

Table 4-4 Summarized Features of IO Library

Note 1: Following types of MOSFET combination (used in core and IO) is legal in this technology

a) 5V and 1.8V
b) 3.3V and 1.8V
c) 5V only
d) 3.3V only
e) 1.8V only

5V and 3.3 V is illegal combination of MOSFET devices for circuit design in this technology.

Note 2: Special supply cells supporting up to 9V and down to -5.5V are available, for details refer to library document PIO520SL.

Note 3: CIO250 and CIO150 can be used in combination, but PIO520 can not be used in combination with CIO250/CIO150 library because all IO available in CIO150/CIO250 contains 3.3V MOSFET at ESD circuit.

4.3 *Standard* Cell Library

Home Directory path : ~/scl180/stdcell/fs120

Contents	**4M1L**	**6M1L**
GDSII library	4M1L/gds	6M1L/gds
CDL Netlist (For LVS Purpose)	4M1L/cdl	6M1L/cdl
Extracted Netlist (SPICE format)	4M1L/spc	6M1L/spc
Technology LEF file directory	4M1L/lef	6M1L/lef
Standard cell LEF file directory	4M1L/lef	6M1L/lef
.lib files directory	4M1L/liberty	6M1L/liberty
Verilog model directory (For Simulation and ATPG Purpose)	4M1L/verilog	6M1L/verilog
P&R Milkyway directory	4M1L/milkyway	6M1IL/milkyway
DOC files(Datasheets)	4M1L/doc	6M1IL/doc

Table 4-5 Standard Cell Library

4.4 Digital PNR Kit for synopsys EDA tools

Home Directory path : ~scl180/digital_pnr_kit/snps/non_rh

Contents	**4M1L**	**6M1L**
Technology File	4M1L/SCL_4LM.tf	6M1L/SCL_6LM.tf
ICC GDS Out Map file	4M1L/icc_gds_out_4LM.map	6M1L/icc_gds_out_6LM.map
TLUPLUS Map file	4M1L/SCL_TLUPLUS_4M1L.map	6M1L/SCL_TLUPLUS_6M1L.map
TLUPLUS File	4M1L/SCL_TLUPLUS_4M1L_TYP.tlup	6M1L/SCL_TLUPLUS_6M1L_TYP.tlup

Table 4-6 Digital PNR Kit for Synopsys EDA tools

4.5 Memory

Home Directory path : ~/scl180/memory

SPRAM Folder Details:

Sr No.	Folder Name	Contents in folder
1	4M1L	Seventeen (17) Memory Cuts
2	6M1L	Twenty (20) Memory Cuts
3	SPRAM*/SP_SRAM*	cdl file, lef file, pmd/datasheet file, verilog file, liberty files(lib & db files), Milkyway database

Table 4-7 SPRAM

SPRAM*/SP_SRAM* - Folder names of Various Memory Cuts with each folder name w.r.t. memory configuration in terms of number of locations and number of data bits.

DPRAM Folder Details:

Sr No.	Folder Name	Contents in folder
1	4M1L	Twenty (20) Memory Cuts
2	6M1L	Twenty (20) Memory Cuts
3	DPRAM*	cdl file, lef file, pmd/datasheet file, verilog file, liberty files(lib & db files), Milkyway database

Table 4-8 DPRAM

DPRAM* - Folder names of Various Memory Cuts with each folder name w.r.t. memory configuration in terms of number of locations and number of data bits.

4.6 Important Documents

Home Directory path : ~/scl180/doc

- Read Me Document : Readme_SCLPDK_v3.pdf
- Design Rule Manual : DRM.pdf
- SPICE Document : DRS.pdf
- Chip finishing flow Document : chip_finishing.pdf
- IO Guidelines : io_guidelines.pdf
- Std Cell Guidelines : std_cell_guidelines.pdf
- Memory Cuts List : memory_cuts_scl.pdf
- External Structure Guidelines : Readme_PDK2020_06122023.pdf

4.7 External Structure - VPTG

Home Directory path : ~/scl180/ext_str

External structures like Silicon number, revision blockade required to be put in every individual chip design for chip identification, layer revision control. In addition to these there are other structures like seal ring and PADs which are to be used by designer to put at appropriate positions. For details please refer document “Readme_PDK2020_06122023.pdf” as mentioned in section 4.6

5. PDK Installation Guide

PDK can be installed by following set of steps. If setup is done properly, while using calibre, libraries/Headers will be set automatically. If not, please do setup again. Please find steps to install PDK in Annexure - I.

6. Metal Flavors available

S. No	Metal Flavor	Process Name (To be used in PDK installation)	Std. Cell lib availability	IO lib availability	External Structure availability
1	4M1L	SCLSL18_4M1L	Yes (1.8V svt only)	Yes (1.8V, 3.3V & 5 V)	Yes
2	6M1L	SCLSL18_6M1L	Yes (1.8V svt only)	Yes (1.8V, 3.3V & 5 V)	Yes

Table 6-1 Available Metal Flavors

7. Reference Design Flow & EDA Tool version

SCL design kit is qualified for these flows and it is recommended to use the same flow for any design.

7.1 Digital Design Flow

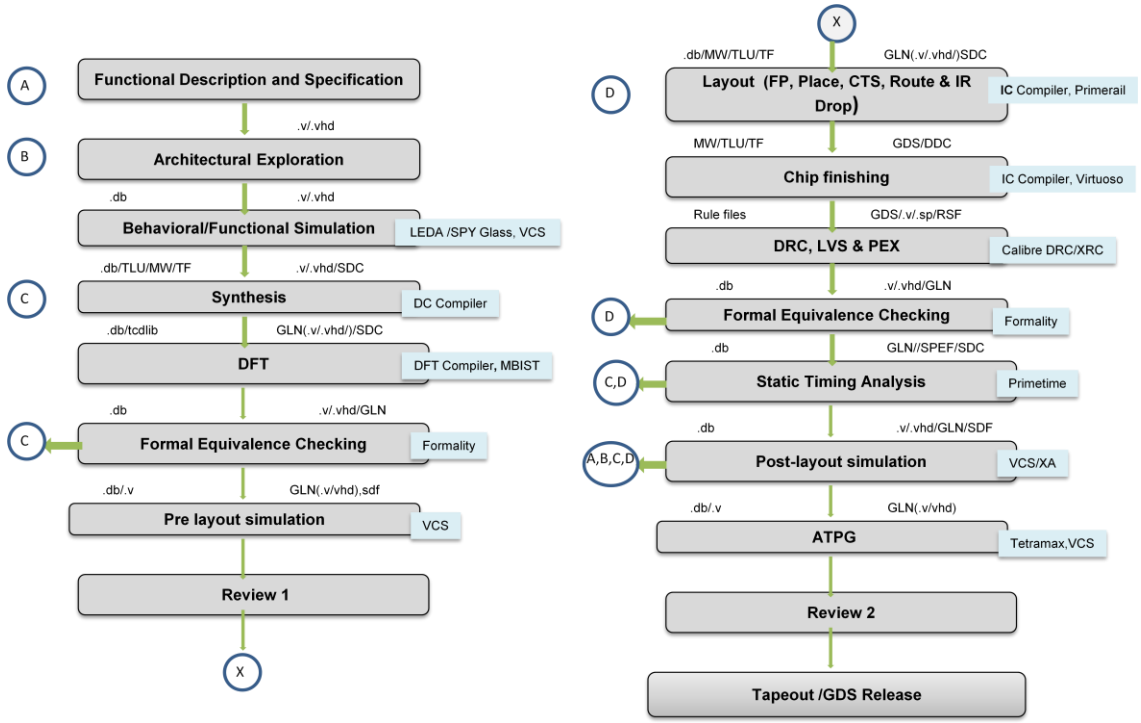

Figure 7-1 Digital Design Flow

7.2 Analog Design Flow

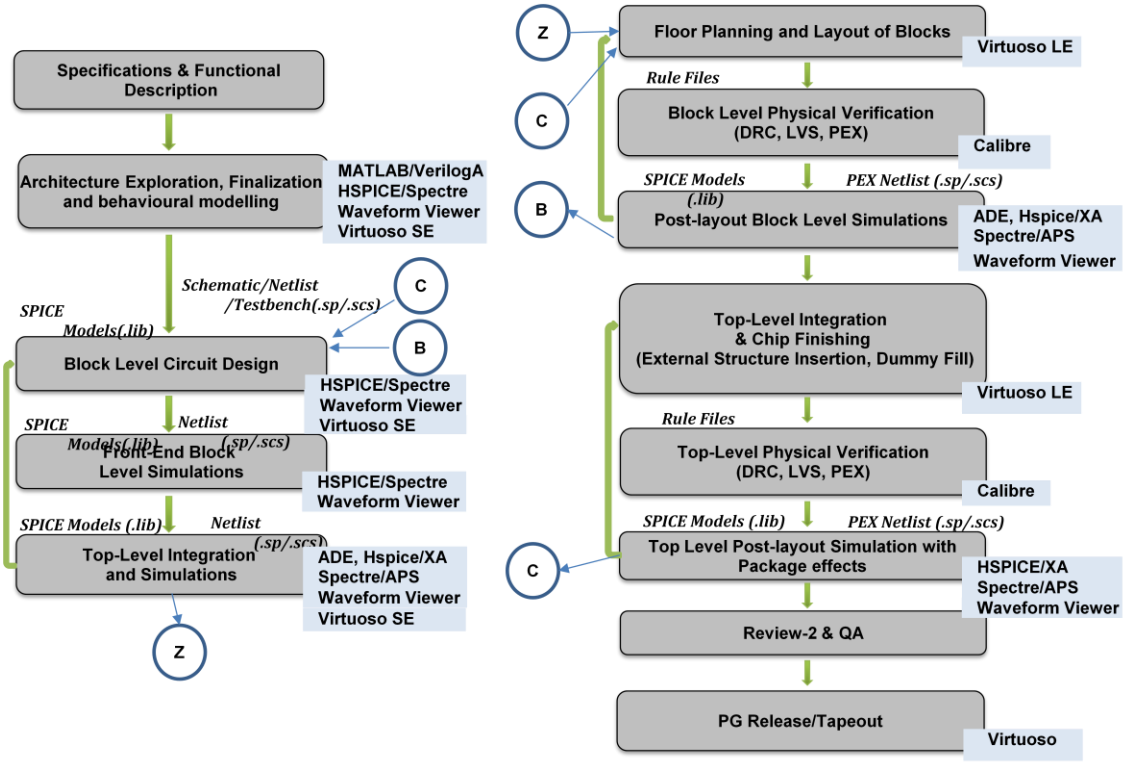

Figure 7-2 Analog Design Flow

7.3 AMS Design Flow

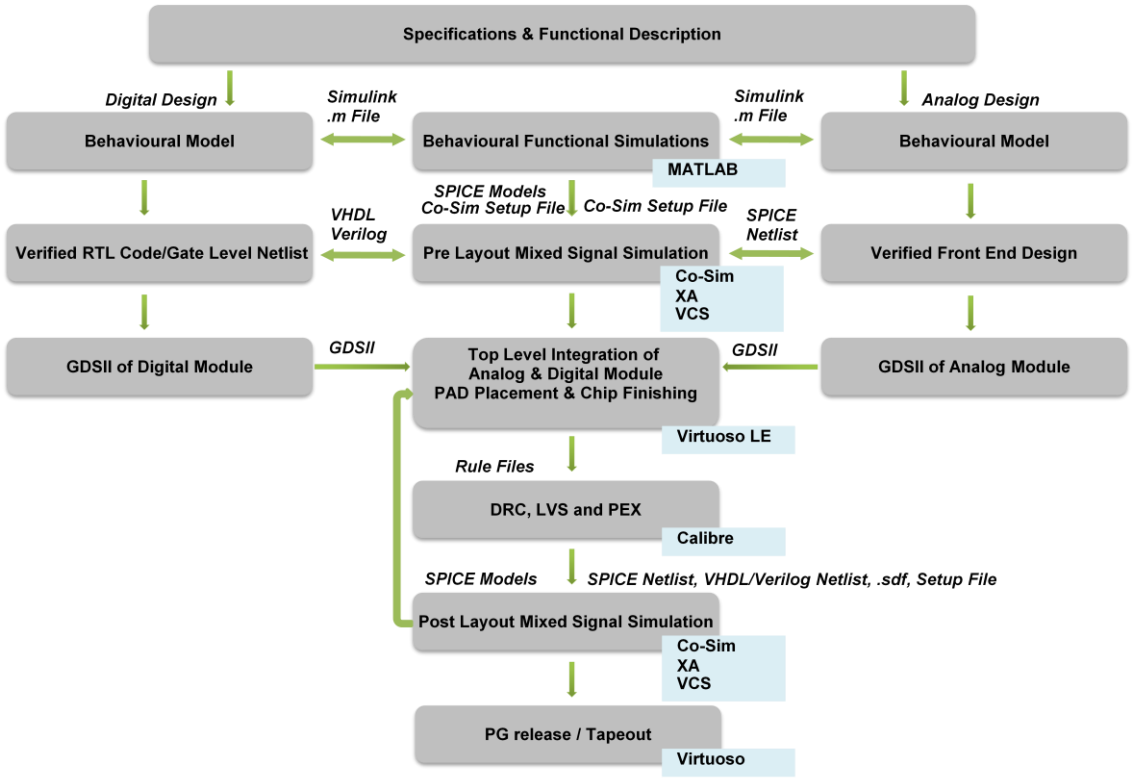

Figure 7-3 AMS Design Flow

7.4 EDA Tool Versions

Files in this design kit are verified against these versions of EDA tools as mentioned in above flows.

Sr. No	Tool	Tool Versions
1	LEDA	K-2015-09 and latest
2	SPYGLASS	R-2020.12 and latest
3	VCS	N-2017.12-1 and latest
4	DC Compiler	N-2017.09-SP2 and latest
5	DFT Compiler	N-2017.09-SP2 and latest
6	MBIST	2018.1 and latest
7	Formality	N-2017.09-SP2 and latest
8	VCS	N-2017.12-1 and latest
9	IC Compiler	N-2017.09-SP2 and latest
10	Primerail	M-2017.06-SP3 and latest
11	Virtuoso	IC6.1.7-64b.500.12 and latest
12	Calibre DRC/XRC	v2017.2_16.14 and latest
13	Calibre LVS	v2017.2_16.14 and latest
14	Calbire PEX	v2022.2_15.10 and latest
15	Primetime	N-2017.12 and latest
16	XA	N-2017.12 and latest
17	Tetramax	K-2015.06-SP5-2 and latest
18	Matlab	R2015b and latest
19	Co-Sim	2018.09 and latest
20	Hspice	J-2014.09 SP1 and latest

Table 7-1 EDA Tool Versions

Annexure – I : PDK Installation Guide

1) Create Installation Directory (<kit_dir_name>)

Create a directory for the design kit to be installed in that is accessible to all the users of the design kit.

% mkdir <kit_dir_name>

% cd <kit_dir_name>

*Here underlined <kit_dir_name> indicates the full path to this directory <kit_dir_name>.

* This step is required only if PDK is not preset in your system.

2) Copy "SCL_PDKV3.tar.gz" tar file in <kit_dir> directory and then untar it in <kit_dir_name> directory

*Please don't untar file in windows system.

*This step is required only if PDK is not preset in your system.

3) Create a root location (<projects>) for all of your projects in your login

Create a location for users design project. This can be any directory that is accessible to users and is outside the <kit_dir_name> directory. This <projects> directory will be the top- level and all projects started will be created below this directory. Need to use the full path for this directory.

% mkdir <projects>

4) Create and customize "pdk_flow_setup.csh" file

This file is used to set up the design kit environment. Each time user works with the design kit, it is required to source this file.

4.1) Update "pdk_flow_setup.csh" file.

Customize the below lines as per users working environment by replacing the items with underlines with a complete directory path. The order in which these commands are

executed is important.

#!/bin/csh -f
setenv KIT_DIR <kit_dir_name>/scl180/pdk/cdns/sclpdk_v3/
setenv RDS_ROOT $KIT_DIR/HOTCODE
setenv MGC_CALIBRE_CUSTOMIZATION_FILE
$RDS_ROOT/techs/generic/calibre/calibre_ts_drc.custom
setenv PERL5 [full path to perl executable]
source $RDS_ROOT/etc/RDS.cshrc
source $RDS_ROOT/etc/cdsDesKit.cshrc
source $RDS_ROOT/etc/cdsSystem.cshrc
setenv PROJ_ROOT <projects>

*Here underlined <projects> (i.e.,<projects>) indicates the full path to this directory <projects>.
*Here <kit_dir_name> is full path to folder where PDK is unzipped.
*In order to find out the full path for perl executable file then type the below command in linux terminal.
% which perl

5) Determine project name

Select a project name to be used for new project. Create a <project_name> folder inside <projects> directory. This name will be used in the instructions when <project_name> value is required. Now save the script file "pdk_flow_setup.csh" in this <project_name> folder and execute the below commands in the terminal:
% cd <projects>
% mkdir <project_name>
% cd <project_name>
% source ./pdk_flow_setup.csh

6) Create project user list

Create a user list for new project that contains each linux user login name with one user per line. Can use commands below, or can edit a file with text editor. The commands

mentioned below will create a file named "user_list" that lists the login name:
% echo <login_id> > user_list

*user_list must contain name of current login only.
For eg: if current login name is "test" then we will write linux command in terminal as:
echo test > user_list

7) Make project directory tree

Use the makeProjectTree command shown below to create the files and directory structure for the new project. User need to contact SCL PDK team for getting suitable flow name for your projects and use the same in below script.

% makeProjectTree <project_name> -flow <Flow name provided by pdk team for your project> -users user_list -flow_lib create -cds -attach -ver -assura -pvs

*Present flow names are: 1. for 4M1L : SCLSL18_4M1L
2. for 6M1L : SCLSL18_6M1L

8) Procedure to launch Cadence virtuoso:

8.1) Go to your <project_name>/work_libs/<login_name>/cds folder by using below linux command as:
% cd <project_name>/work_lib/<login_name>/cds

*Here underlined <project_name> (i.e.,<project_name>) indicates the full path to this directory <project_name>.

8.2) An alias cdsprj is defined when pdk_flow_setup.csh is sourced. This alias sources project specific cdsUsr.cshrc and changes working directory to be user- specific cds directory within users project. To begin working in Cadence, type the following:
% cdsprj <project_name>

8.3) Launch Virtuoso

*If setup is done properly, while using ADE or calibre, libraries/Headers will be set

automatically. If not, please do setup again.

9) Launching existing project

9.1) Go to <project_name> directory.
% cd <project_name>

*Here underlined <project_name> (i.e.,<project_name>) indicates the full path to this directory <project_name>.

9.2) Source "pdk_flow_setup.csh" file.
% source ./pdk_flow_setup.csh

9.3) Go to your <project_name>/work_libs/<login_name>/cds folder by using below linux command as:
% cd <project_name>/work_lib/<login_name>/cds

*Here underlined <project_name> (i.e.,<project_name>) indicates the full path to this directory <project_name>.

9.4) An alias cdsprj is defined when pdk_flow_setup.csh is sourced. This alias sources project specific cdsUsr.cshrc and changes working directory to be user- specific cds directory within users project. To begin working in Cadence, type the following:
% cdsprj <project_name>

9.5) Launch Virtuoso

*If setup is done properly, while using Calibre, libraries/Headers will be set automatically. If not, please do setup again.