General Information and Guidelines

On

IOPAD

0.18µm SCL18SL

Semiconductor Laboratory

Rev 2023.01 – December 2023

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General I/O library Information

There are three types of I/O libraries

1. CIO 150 (core 1.8V & I/O 1.8V)
2. CIO250 (core 1.8V & I/O 3.3V or core & I/O 3.3only)
3. PIO520 (core & I/O - 5VOnly, 5V/1.8V and 1.8V)

CIO 150: The CIO150 library is made up exclusively of low voltage chip interface circuits powered by a voltage in the range of 1.65V to 1.95V. This library has been designed to be used at a frequency up to 130MHz, on a maximum external load capacitance of 40pF and for a pin package inductance up to 20nH. This library uses a 3.15 mils pitch. The size of the IO is 65µm width and 162µm height without bonding pad. With bonding pad the height is 250µm. The usable filler cells are provided in this library. The library is designed to meet high performance, low power, and is compliant with industry standard ESD, Latch-Up and electrical guidelines.

CIO 250: CIO250 library is made up exclusively of low voltage chip interface circuits powered by a voltage in the range of 2.7V to 3.6V. The direct input pad is only 1.8V (VDD core, 1.62V up to 1.98V) tolerant if connected to core standard cells. This library supports 3.3V/1.8V containing all necessary digital, analog, power, ground and support cells. The CIO250 library has been designed to be used at a frequency up to 130MHz, on a maximum external load capacitance of 40pF and for a pin package inductance up to 20nH. This library uses a 3.15 mils pitch. The size of the IO is 65µm width and 162µ height without bonding pad. With bonding pad the height is 250µm. Using the bonding cell provided with this library the I/Os can be abutted. Customer bonding cell can be used for the I/O. The usable filler cells are provided in this library. The library is designed to meet high performance, low power, and is compliant with industry standard ESD, Latch-Up and electrical guidelines.

PIO520: PIO520 is an SCL`s IO library electrically and physically designed for SCL18SL process, offered with either Stack pad. This library supports 5V-Only, 5V/1.8V and 1.8V-Only, containing all necessary digital, analog, power, ground and support cells. The library is designed to meet high performance, low power, and is compliant with industry standard ESD, Latch-Up and electrical guidelines.

Table 1: Core, I/O voltages and Backend options in CIO150/CIO250/PIO520

		CIO 150	CIO250		PIO520		
Core Voltage		1.8V	1.8V	3.3 V	1.8V	1.8V	5V
I/O Voltage		1.8V	3.3V	3.3V	1.8V	5V	5V
Backend option	4LM	4M1L	4M1L	4M1L	4M1L	4M1L	4M1L
	6LM	6M1L	6M1L	6M1L	6M1L	6M1L	6M1L

1.1 Details of I/O pads For *CIO150/CIO250*

Different types of I/O pads are available in the *CIO150/CIO250* library. Commonly required power/ground pads are listed below. Generic I/O pad frame diagram is shown in figure1. Details and recommendations on the optimum use of power buses are described in the SSO guidelines document (an_ tsl18cio150.pdf) and Power Distribution Guidelines and power routing are provided in separate documents (PowerStrapping.pdf & Power_routing.pdf)

- pv0a (used for ground connection)
- pv0i (used for ground connection)
- pv0c (used for ground connection)
- pvda (used for power connection)
- pvdi (used for power connection)
- pvdc (used for power connection)

Guidelines for uses of these pads can be taken from **section 5.0 "System Design Considerations**" of document ds_tsl18cio250.pdf/ ds_tsl18cio150.pdf

1.2 I/O for Analog Circuit

PC3D00 cell is a direct input/output pad, without buffer, suitable for bringing analog signals or reference voltages onto the chip. The current function of this pad is to provide to the core an external chip signal without any gain. In this usage it is mandatory not apply to this pad greater voltage than allowed by the core cell connected to this pad. This I/O pad supports 3.3Vonly, 3.3V/1.8V and 1.8V only circuits. This I/O can also be used in digital circuit if non buffered pad is required. More details are available of this I/O pad in datasheet of cio250/cio150 and n_analog_io_flow.pdf

1.3 I/O pads for digital circuits

A large variety of I/O pads (CMOS, with pull-up resistor, different driving strength etc.) are available. More information can be obtained from following document available along with the process design kit (PDK) .

a) ds_tsl18cio250.pdf
b) ds_tsl18cio150.pdf
c) an_io_flow.pdf

1.4 I/O fillers and corner pads: I/O fillers required to fill the space between the I/O pads placed in the ring and to make the continuity of the ring. Corner pads are placed on the four corners of die layout as depicted in figure 1. Detail information of these is available in section 5.5 and 5.6 of document ds_tsl18cio250.pdf. There are two types of filler and corner pads (e.g., pfeed00010,.. & afeed00010…) of various widths are present in CIO150/CIO250, while the dummy corner cells information is available in Section 9.1.7 "Dummy Pad Rules" of DR2-0018_SL_4_2.pdf document supplied along the PDK.

1.5 3.3V only Analog design: CIO 250 supports 3.3V only design, to realize this design PC3D00 I/O should be used for input/output signals and PVDC for power and **PV0C(with modification – guidelines can be obtained from SCL)** for ground. VDDO and VDD has to be shorted at I/O ring at many places and VSSO and VSS to be shorted at I/O ring at many places. All other guidelines have to be followed as per guidelines document available with PDK.

1.6 ESD Performance of I/O Pad/SSO Guidelines: Documents namely an_tsl18cio150sso.pdf/ an_tsl18cio250sso.pdf are to help the IO library users to calculate the number of power pads to be used in their design. These documents give the basic guidelines for Simultaneously Switching Outputs (SSO), for currents density and for electrostatic discharge (ESD) issues, to allow optimizing the placement the power pads.

Table2: Documents available in CIO150

Document	Brief Purpose
PowerStrapping.pdf	Power distribution guidelines
Power_routing.pdf	Power routing guielines

An_analog_io_flow.pdf	Analog Staggered I/O library Usage
An_io_flow.pdf	Application Notes- I/O library Usage
An_tsl18cio150sso.pdf	Application Notes -SSO guidelines
Ds_tsl18cio150.pdf	Datasheet of I/O pad

Table3: Documents available in CIO250

Document	Brief Purpose
PowerStrapping.pdf	Power distribution guidelines
Power_routing.pdf	Power routing guielines
An_analog_io_flow.pdf	Analog Staggered I/O library Usage
An_io_flow.pdf	Application Notes- I/O library Usage
An_tsl18cio250sso.pdf	Application Notes -SSO guidelines
Ds_tsl18cio250.pdf	Datasheet of I/O pad

2.1 Details of I/O pads For *PIO520*

PIO 520 library has following features. Usage guidelines, maximum operation conditions, complete I/O cells list, filler cell, corner cells, ESD characteristics, digital/analog/power I/O cells and application optimized cells are explained in PIO520 document (ds_tsl18pio520sl.pdf). These I/O pads are using dnpwcpl, dnpwcpl5, dpnwcpl and dpnwcpl5 diodes in their cdl. To simulate these I/O cells, include the IO_pads_diode.lib model file.

Features

2.1.1 FULL CMOS OFFERING

- 5V-Only (single gate oxide)
- 5V/1.8V (dual gate oxide)
- 1.8V-Only (single gate oxide)

2.1.2 FLEXIBLE POWER SUPPLY OPTIONS

- 2.7-5.5V IO and Core sides
- 2.7-5.5V IO and 1.8V±10% Core sides
- 1.8V±10% IO and Core sides

2.1.3 VARIOUS METALLIZATION OPTIONS

- 4 & 6 metal layers with 9KÅ Aluminum Top Metal

2.14 APPLICATION OPTIMIZED

- Integrated Over Voltage Tolerant and Power-Off Protection in all data cells
- Special supply cells supporting up to 9V and down to -5.5V

2.1.5 ESD COMPLIANCE

- >2KV HBM

- >200V MM

2.1.6 LATCH-UP IMMUNITY

- >100 mA

2.2 Quick reference guide for I/O PAD CIO 150/250 library

Table4 : CMOS I/O Pad

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PC3B01	•			1x			1
PC3B02	•			2x			1
PC3B03	•			3x			1
PC3B04	•			4x			1
PC3B05	•			5x			1
PC3B01D	•			1x	•		1
PC3B02D	•			2x	•		1
PC3B03D	•			3x	•		1
PC3B03ED	•			3x	•		1
PC3B04D	•			4x	•		1
PC3B05D	•			5x	•		1
PC3B01U	•			1x		•	1
PC3B02U	•			2x		•	1
PC3B03U	•			3x		•	1
PC3B04U	•			4x		•	1
PC3B21EU	•			1x		•	1
PC3B25EU	•			5x		•	1
PC3B05U	•			5x		•	1
PC3O01		•		1x			1
PC3O01HV		•		1x			1
PC3O02		•		2x			1

CMOS Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PC3O03		•		3x			1
PC3O04		•		4x			1
PC3O05		•		5x			1
PC3T01			•	1x			1
PC3T02			•	2x			1
PC3T03			•	3x			1
PC3T04			•	4x			1
PC3T05			•	5x			1
PC3T01D			•	1x	•		1
PC3T02D			•	2x	•		1
PC3T03D			•	3x	•		1
PC3T04D			•	4x	•		1
PC3T05D			•	5x	•		1
PC3T01U			•	1x		•	1
PC3T02U			•	2x		•	1
PC3T03U			•	3x		•	1
PC3T04U			•	4x		•	1
PC3T05U			•	5x		•	1

Table5: TTL I/O Pads for CIO 250

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PT3B01	•			2mA			1
PT3B02	•			8mA			1
PT3B03	•			16mA			1
PT3B01D	•			2mA	•		1

PT3B02D	•			8mA	•		1
PT3B03D	•			16mA	•		1
PT3B01U	•			2mA		•	1
PT3B02U	•			8mA		•	1
PT3B03U	•			16mA		•	1
PT3O01		•		2mA			1
PT3O02		•		8mA			1
PT3O03		•		16mA			1
PT3T01			•	2mA			1
PT3T02			•	8mA			1
PT3T03			•	16mA			1
PT3T01D			•	2mA	•		1
PT3T02D			•	8mA	•		1
PT3T03D			•	16mA	•		1
PT3T01U			•	2mA		•	1
PT3T02U			•	8mA		•	1
PT3T03U			•	16mA		•	1

Table6: Analog I/O Pads

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pulldown Device	Pullup Device	Pad Sites Used
PC3D00	ANALOG		•				1

Table 7: CMOS Input Only Pads

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-Inverting	Inverting	Pulldown Device	Pullup Device	Pad Sites Used
APC3D01	CMOS		•				1
PC3D01	CMOS		•				1

PC3D01D	CMOS		•		•		1
PC3D01U	CMOS		•			•	1
PC3D11	CMOS			•			1
PC3D11D	CMOS			•	•		1
PC3D11U	CMOS			•		•	1
PC3D21	CMOS	•	•				1
PC3D21D	CMOS	•	•		•		1
PC3D21EU	CMOS	•	•			•	1
PC3D21U	CMOS	•	•			•	1
PC3D31	CMOS	•		•			1
PC3D31D	CMOS	•		•	•		1
PC3D31U	CMOS	•		•		•	1

Table8: Crystal Oscillator Pads

Cell Name	Frequency Category	Maximum Operating Frequency	Pad Sites Used
PC3X11	Low	10MHz	2
PC3X12	Intermediate	40MHz	2
PC3X13	High	100MHz	2

Table9: Core Driven Clock Buffer Pad

Cell Name	Drive Strength	Non-Inverting	Inverting	Pad Sites Used
PC3C01	1x	•		1
PC3C02	2x	•		1
PC3C03	3x	•		1
PC3C04	4x	•		1

Table 10: Power Pads

	Power Bus Connections								Pad Sites Used
	vssi	vsso	avssi	avsso	vddi	vddo	avddi	avddo	
PV0I	•								1
PV0A		•							1
PV0C									1 (**)
PV0F	•	•							1
APV0I			•						1
APV0A				•					1
PVDI					•				1
PVDA						•			1
PVDC									1 (**)
APVDI							•		1
APVDA								•	1

**) Note: PVDC/PV0C is used to supply VDD/VSS to core only then do not supply any I/O power ring.

Table 11: Cut Power Pads

	Cut Power Bus							
	vssi	vsso	avss	avsso	vddi	vddo	avdd	avddo
PVCF		•	•	•	•	•	•	•
PVCE	•	•	•	•		•	•	•
APFEEDENDRINGL		•	•	•	•	•	•	•
APFEEDENDRINGR		•	•	•	•	•	•	•

Table12: TTL I/O Pads for CIO 150

TTL Cell Name	3-State I/O	Output Only	3-State Output Only	Drive Strength	Pulldown Device	Pullup Device	Pad Sites Used
PT3B01	•			2mA			1
PT3B02	•			6mA			1
PT3B03	•			10mA			1
PT3B01D	•			2mA	•		1

PT3B02D	•			6mA	•		1
PT3B03D	•			10mA	•		1
PT3B01U	•			2mA		•	1
PT3B02U	•			6mA		•	1
PT3B03U	•			10mA		•	1
PT3O01		•		2mA			1
PT3O02		•		6mA			1
PT3O03		•		10mA			1
PT3T01			•	2mA			1
PT3T02			•	6mA			1
PT3T03			•	10mA			1
PT3T01D			•	2mA	•		1
PT3T02D			•	6mA	•		1
PT3T03D			•	10mA	•		1
PT3T01U			•	2mA		•	1
PT3T02U			•	6mA		•	1
PT3T03U			•	10mA		•	1

		Table 13 I/O Pad for PIO250 Library			
	I/O cell	Description	5V Only	5V/1.8V	1.8V-Only
	Digital IO Cells				
1	PIOH_50_50	Digital IO for IO Side	√		
2	PIOHO_50_50	Digital IO for IO Side with 9V tolerance	√		
3	PIOH_50_18	Digital IO for IO Side with 9V tolerance		√	
4	PIOHO_50_18	Digital IO for IO Side with 9V tolerance		√	
5	PIOL_NA_18	Digital IO for Core Side		√	√
6	PIOH_18_18	Digital IO for IO Side			√
	Analog IO Cells				
7	PAH_50_NA	Analog IO for IO Side	√	√	
8	PAN_50_NA	Negative Supply (-5.5V)	√	√	
9	PVPP_50_NA	High Voltage Supply (9V)	√	√	
10	PAL_NA_18	Analog IO for Core Side		√	√
11	PAH_18_NA	Analog IO for IO Side			√
	Power Cells				
12	PVDA_50_NA	Power Supply for IO Side and IC circuits	√	√	
13	PVDI_NA_50	Power Supply for Core Side and IC circuits	√	√	
14	PVDF_50_50	Power Supply for IO Side, Core Side and IC	√		
15	PVDC_NA_NA_50	Power Supply for IC circuits only	√	√	
16	PVDI_NA_18	Power Supply for Core Side and IC circuits		√	√
17	PVDA_18_NA	Power Supply for IO Side and IC circuits			√
18	PVDF_18_18	Power Supply for IO Side, Core Side and IC			√
19	PVDC_NA_NA_18	Power Supply for IC circuits only			√
	Ground Cells				
20	PV0A_50_50	Ground Supply for IO Side and IC circuits	√		
21	PV0I_50_50	Ground Supply for Core Side and IC circuits	√		
22	PV0F_50_50	Ground Supply for IO Side, Core Side and IC	√		
23	PV0C_50_50_50	Ground Supply for IC circuits only	√		
24	PV0A_50_18	Ground Supply for IO Side and IC circuits		√	
25	PV0I_50_18	Ground Supply for Core Side and IC circuits		√	
26	PV0F_50_18	Ground Supply for IO Side, Core Side and IC		√	
27	PV0C_50_18_50	Ground Supply for IC circuits only		√	
28	PV0C_50_18_18	Ground Supply for IC circuits only			
29	PV0A_18_18	Ground Supply for IO Side and IC circuits			√
30	PV0I_18_18	Ground Supply for Core Side and IC circuits			√
31	PV0F_18_18	Ground Supply for IO Side, Core Side and IC			√
32	PV0C_18_18_18	Ground Supply for IC circuits only			√
	Cut Cells				
33	PCDA_50_NA	Cut of IO Side Power Supply	√	√	
34	PCDI_NA_50	Cut of Core Side Power Supply	√		
35	PC0A_50_NA	Cut of IO Side Ground Supply	√	√	
36	PC0I_NA_50	Cut of Core Side Ground Supply	√		
37	PCDI_NA_18	Cut of Core Side Power Supply		√	√
38	PC0I_NA_18	Cut of Core Side Ground Supply			√
39	PCDA_18_NA	Cut of IO Side Power Supply			√
40	PC0A_18_NA	Cut of IO Side Ground Supply		√	√
	Coupling (Diode) Cells				
41	PDDA_50_NA	Coupling of IO Side Power Supply	√	√	
42	PDDI_NA_50	Coupling of Core Side Power Supply	√	√	
43	PD0A_50_NA	Coupling of IO Side Ground Supply	√	√	
44	PD0I_NA_50	Coupling of Core Side Ground Supply	√	√	
45	PDDI_NA_18	Coupling of IO Side Power Supply			√
46	PD0I_NA_18	Coupling of Core Side Power Supply			√
47	PDDA_18_NA	Coupling of IO Side Ground Supply			√
48	PD0A_18_NA	Coupling of Core Side Ground Supply			√
	Service Cells				

49	POK_50_50	Power Detection for IO and Core Sides	√		
50	POK_50_18	Power Detection for IO and Core Sides		√	
51	POK_18_18	Power Detection for IO and Core Sides			√
	Filler Cells				
52	PFILL0001_NA_NA	Filler Cell	√	√	√
53	PFILL0010_NA_NA	Filler Cell	√	√	√
54	PCORNER_NA_NA	Corner Cell	√	√	√
55	PRENROC_NA_NA	Corner Cell	√	√	√

3.0 General Pad frame diagram

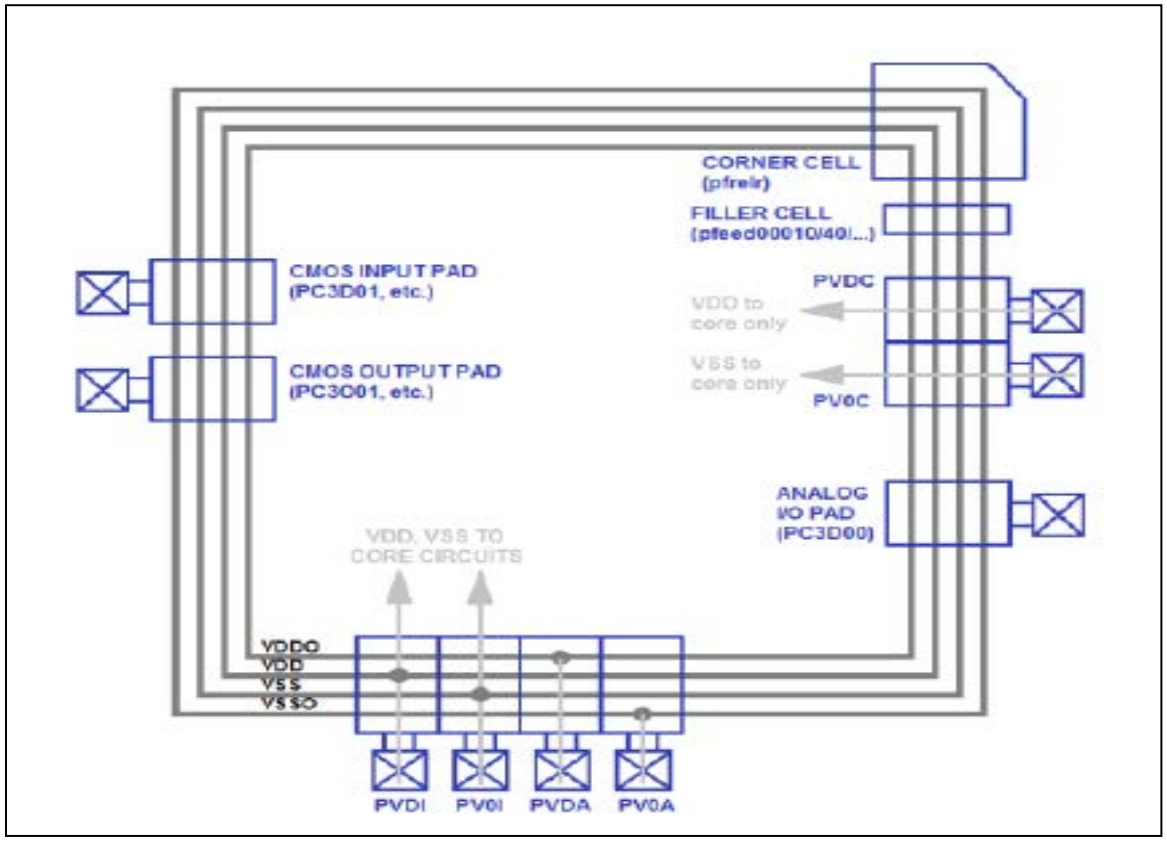

Figure1: Generic I/O pad frame