High speed and area efficient scalable N-bit digital comparator

Major Project Report

Submitted in partial fulfilment of the requirements for the degree of

MASTER OF TECHNOLOGY
in
VLSI Design

by

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Reg No.2120359
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NATIONAL INSTITUTE OF TECHNOLOGY,KARNATAKA
SURATHKAL, MANGALORE - 575025

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Under the guidance of

Dr. M S Bhat
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY,KARNATAKA
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November, 2022

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DECLARATION

by the M.Tech (Regular) Student

I hereby declare that the report of the P.G. Project Work entitled **High speed and area efficient scalable N-bit digital comparator** which is being submitted to the National Institute of Technology Karnataka Surathkal, in partial fulfilment of the requirements for the award of the Degree of **Master of Technology in VLSI Design** in the department of Electronics and Communication Engineering, is a bonafide report of the work carried out by me. The material contained in this report has not been submitted to any University or Institution for the award of any degree.

Rathod Jaypal Prakash
Roll No: 212VL016
Department of Electronics and Communication Engineering

Place: NITK, Surathkal
Date: November 21, 2022

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CERTIFICATE

This is to certify that the P.G Project Work Report entitled **High speed and area efficient scalable N-bit digital comparator** submitted by **Rathod Jaypal Prakash, (Roll No: 212VL016)** as the record of the work carried out by him, is accepted as the P.G Project Work Report submission in partial fulfilment of the requirements for the award of degree of **Master of Technology in VLSI Design** in the Department of Electronics and Communication Engineering, National Institute of Technology Karnataka Surathkal, during the academic year of 2021-2023.

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Place: NITK Surathkal
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Abstract

This project presents an area-efficient N-bit digital comparator with high operating speed and low power consumption.There are two distinct modules in the proposed comparator structure. The comparison evaluation module (CEM) is the first module, and the comparator final results is decided by the second module. Stages in CEM entail the regular structure of repeating logic cells needed to build parallel prefix tree structure, independent of the input operand bitwidths.The presence of highly large-scale integration topology on a regular basis in the designed structure enables the area to be calculated analytically in terms of the bitwidth and transistor count in the design. The total delay observed in input-output flow is a function of bitwidth of input operand. Spectre simulation results have been presented using 180 nm CMOS technology.

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ABBREVIATIONS

AEB	-	A is equal to B
AGB	-	A is greater than B
ALB	-	A is lesser than B
CEM	-	Comparison evaluation module
COMP	-	Complement function
FA	-	Full adder
FM	-	Final module

Chapter 1

Introduction

A digital comparator is the fundamental design element required in applications where the final results are dependent on the output of a calculation that includes comparison as an activity. The optimised comparator design is utilised as a major component in general purpose computer architecture. The extensive usage of comparator logic in many computation-based architectures needs area, power, and speed optimization.

1.1 Motivation

1. It is found that comparator design using novel Exor-nor cell method is more superior as compaired to design of comparator using dynamic logic.

2. The proposed structure's regular VLSI topology enables analytical derivation of area in terms of total number of transistors in the design and total delay encountered in input output flow as a function of input operand bitwidth.

1.2 Objective of the project

The goal of this project is to reduce the total number of transistors while maintaining high operating speed, low power dissipation, and a less effective area. For this proposed method of N-bit comparator is designed using Exor-nor cell. For speed enhancement and power consumption reduction, N-bit comparators based on pipelining and power-down techniques is implemented and analysed.

Chapter 2

Literature review

1. A parallel binary comparator in [4] has a normal digital hardware structure that is independent of input bitwidths, but it has a large area and power consumption.

2. Some comparator designs use dynamic logic to achieve low-power consumption, however the low-speed and low-noise margin requirements make the dynamic design fairly difficult. The designs in [3], [6], [7] and [8] employ subtractors in the form of flat adder components in conjunction with specialized logic circuits to implement comparison processes for broader bit operands, however these designs have a longer response time and occupy more space.

3. Some of the parallel prefix tree structure limiting characteristics, such as size and power consumption, can be improved by employing two input multiplexers at each level and generate-propagate logic at the first level [2].

4. This project is based on the work presented in [1], [5] & [7] for designing a scalable N-bit digital comparator that is fast and small in size.

Chapter 3

Workdone

3.1 Methodology of N-bit digital comparator design

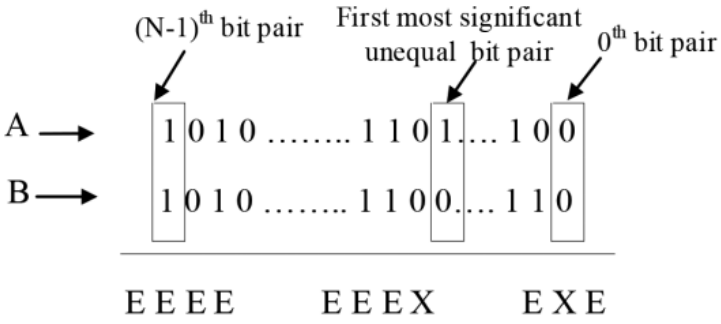

Figure 3.1: Comparing two N-bit operands [7]

The comparison process shown in Fig. 3.1 used to compare N-bit operands begins comparison from the (N-1)th (or MSB bit) and moves toward the comparison of the (N-2)th bit and so on. The unequal bit pair (X) and equal bit pair (E) are realised as

$$X = A\ Exor\ B; E = A\ Exnor\ B \tag{3.1}$$

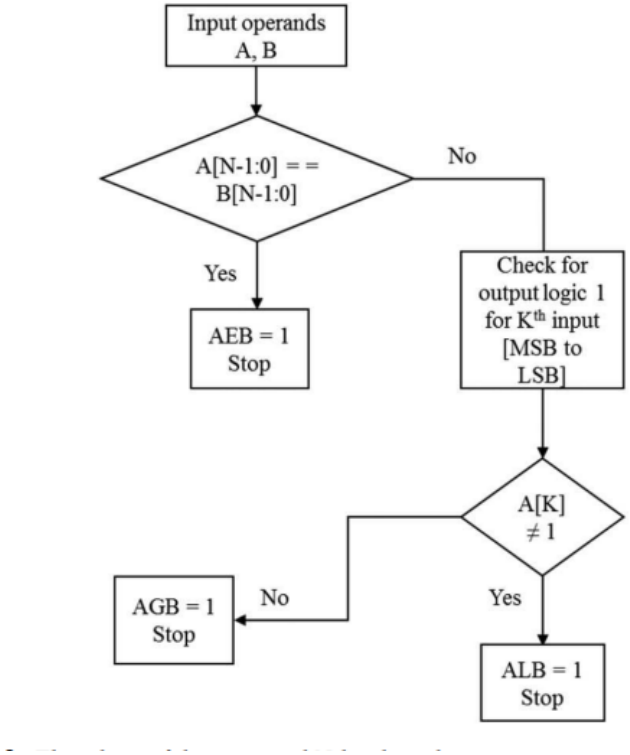

Figure 3.2: N-Bit digital comparator design flowchart [7]

The flowchart of the algorithm used for the implementation of the proposed N-bit digital binary comparator is shown in Fig.3.2. The two N-bit input operands A and B are selected for the comparison and are checked if the operands are equal or not equal by performing the bitwise comparison. If the result of comparison comes out as 'equal', then the proposed comparator drives the output logic AEB to logic 1. If the comparison result of the operands comes out as 'unequal', then the pre-encoder output bits are checked from MSB to LSB. The output logic AGB or ALB goes to logic 1 based on the results of pre-encoder.

3.2 Structure of N-bit digital comparator

The proposed structure is divided into the comparison evaluation module (CEM) and final module (FM). These modules serve as a high-level and low-level architectures for comparing two N-bit binary operands, as shown in Fig 3.3. To explore the regularity of the proposed comparator for arbitrary bitwidths, two operands A and B are applied into 4bit partitions as $A_{N1}A_{N-2}....A_0$ and $B_{N1}B_{N-2}....B_0$.

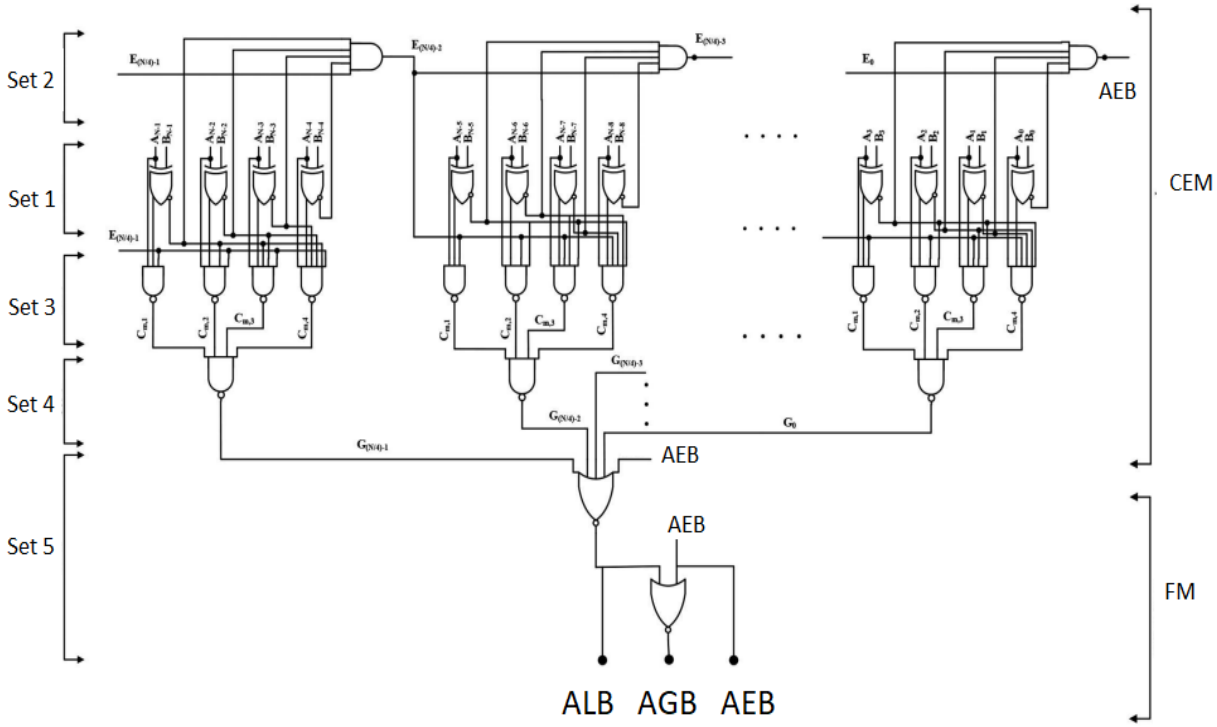

Figure 3.3: Novel proposed N-bit digital comparator [7]

1. The complete comparison procedure consists of five Sets; CEM has Sets 1-4 while FM contains Set 5. All the Sets in the design are arranged in five hierarchal prefix orders according to their functionality.

2. In Set 1, a novel Exor-nor cell shown in Fig 3.4, a bitwise comparison of two N-bit binary operands.

   (a) The termination and comparison bits required for Set 2 and 3 structure are output of novel Exor-nor cell.

   (b) Equation (3.2) shows how the novel Exor-nor cell functions.

$$T_k = A_k \; Exnor \; B_k; D_k = A_k \; Exor \; B_k \tag{3.2}$$

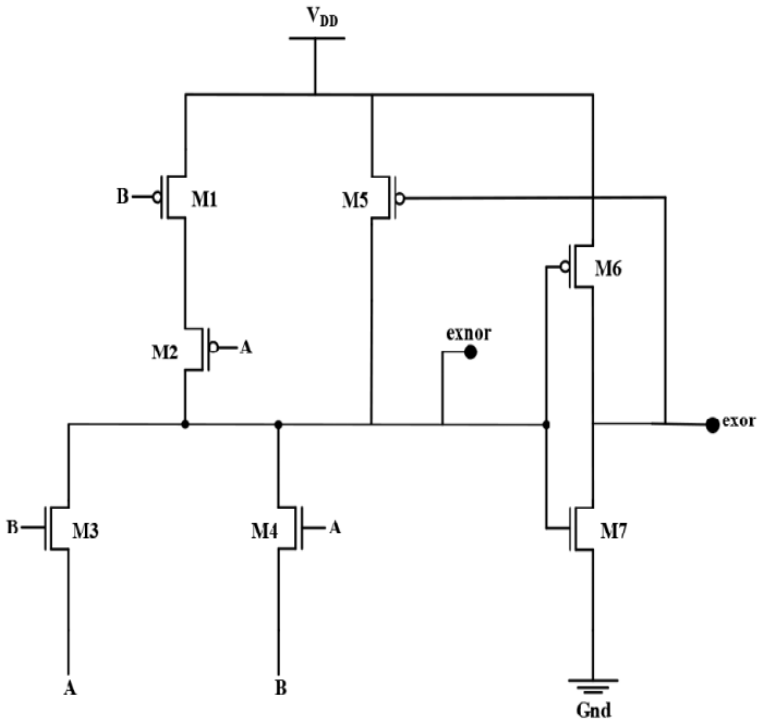

Figure 3.4: Novel Exor-nor cell [7]

where k is an integer that ranges from 0 to N–1.
T_k represents an equal bit pair, D_k represents an unequal bit pair of the operands A and B.

3. Set 2 consists of cells that use the termination bits from Set 1 to operate. The logic cells in Set 2 combine the outputs from the previous AND-type logic cells in the same level of Set 2 with the termination bits received from the nibble partitions in Set 1 to create a final output.

4. Cells in Set 3 combine the results from Set 1 and Set 2 output. The pre-encoder structure is made up of the architectures from Sets 1 and 3.

5. Set 4 inputs are received from NAND-type logic cells in Set 3, and Set 4 needs (N/4) cells to aggregate the outputs from each of Set 3 partitions.

6. Set 5 contains two NOR-type logic cells to decide the final results of the proposed digital comparator in terms of ALB and AGB. First NOR gate uses outputs of Set 4 and AEB as inputs to decide 'ALB', whereas second NOR gate uses the output of first NOR gate and 'AEB' as inputs to decide 'AGB'.

3.3 Proposed design & implementation

Fig. 3.5 shows symbolic representation of different input NAND, AND, NOR gate & Exor-nor cell implementation using cadence virtuoso 180 nm CMOS Technology by static CMOS Logic.

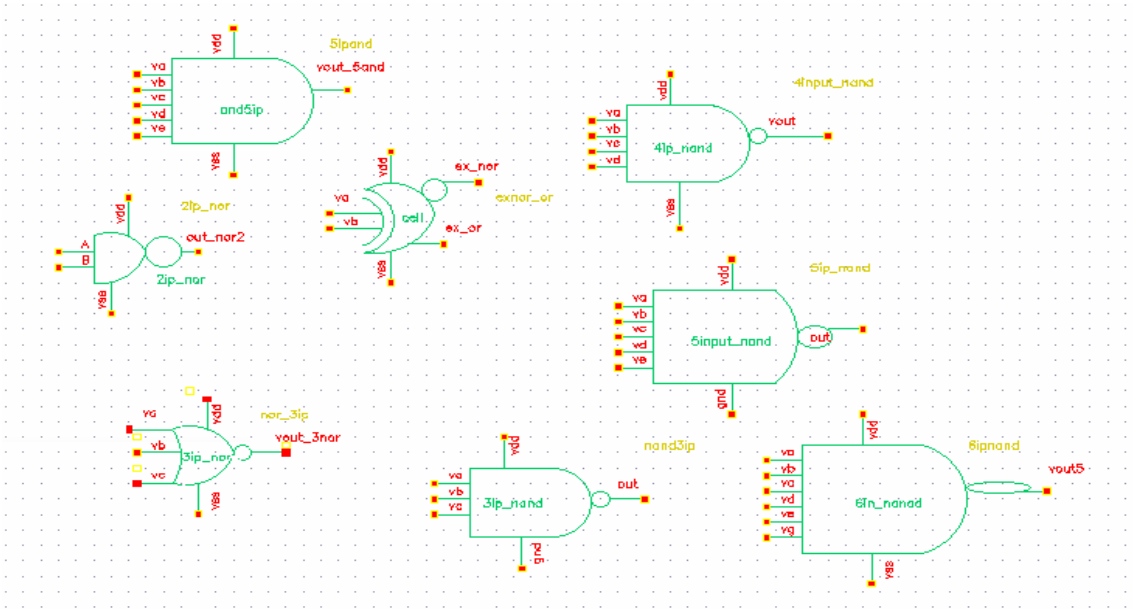

Figure 3.5: Symbolic representation of different input NAND, AND, NOR gate & Exor-nor cell implementation using static CMOS Logic

3.3.1 Novel Exor-nor cell implementation

Novel Exor-nor cell as shown in Fig. 3.5 is based on the pass transistor logic and CMOS logic. The novel structure uses a PMOS transistor in the feedback to maintain the logic level on the Exnor output terminal and the CMOS logic to boost up the output for achieving the full voltage swing on the Exor output terminal.

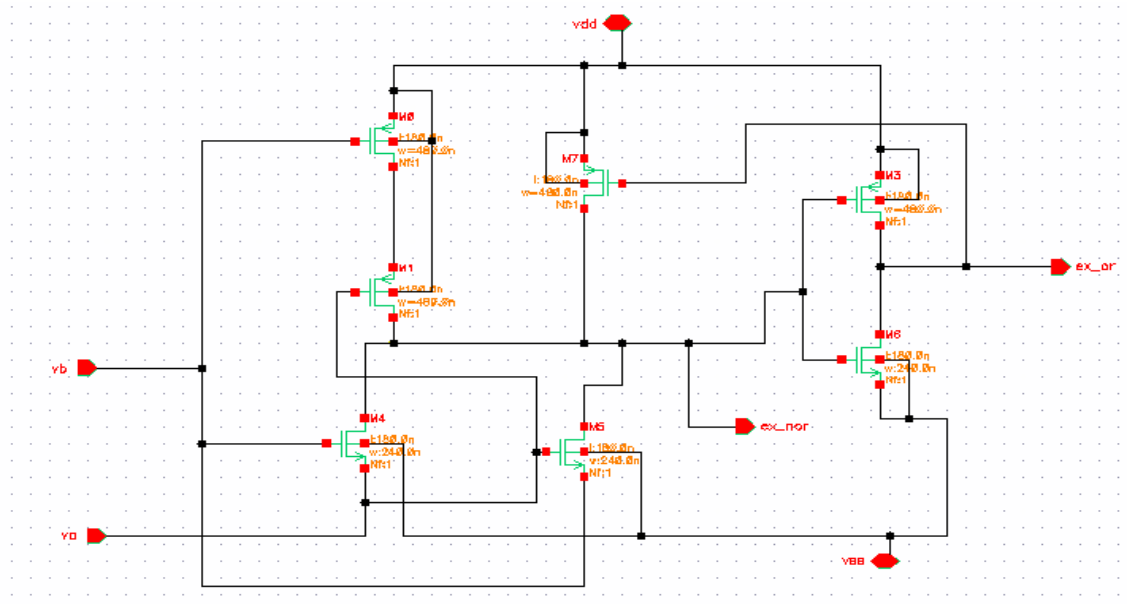

Figure 3.6: Novel Exor-nor cell design using cadence

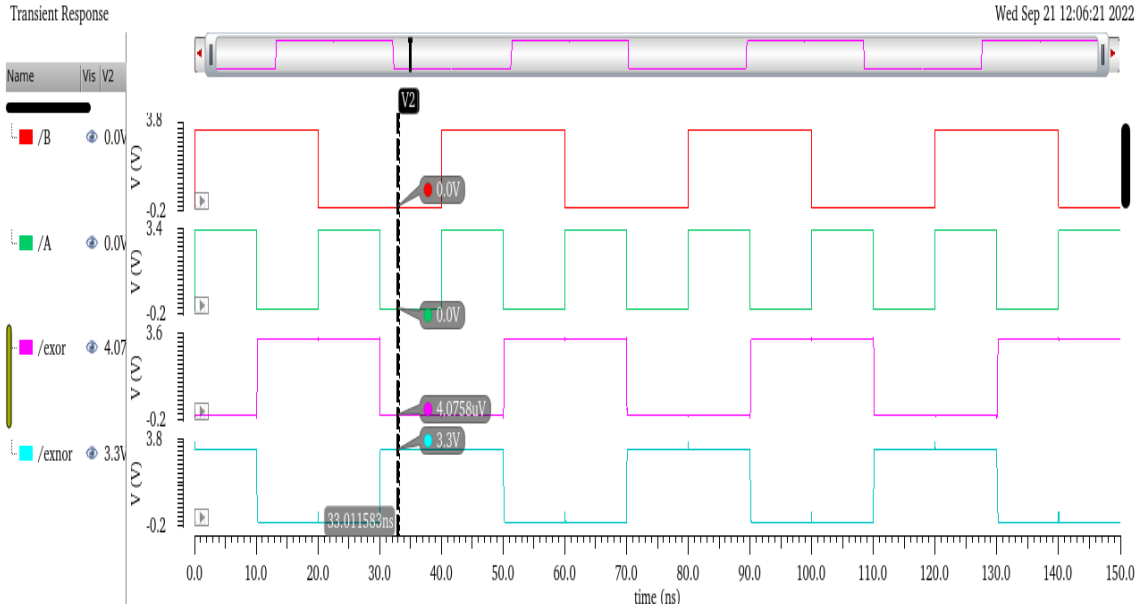

Figure 3.7: Output waveform of Exor-nor cell

1. Fig. 3.7 shows the transient response of Exor-nor cell. In which A & B are two 1-bit input operands.

2. Fig 3.7 shows the output of Exor-nor cell which is logic 0 and logic 1 respectively, for the input pattern A = 0, B = 0.

3.3.2 Proposed implementation of 4-bit digital comparator cell

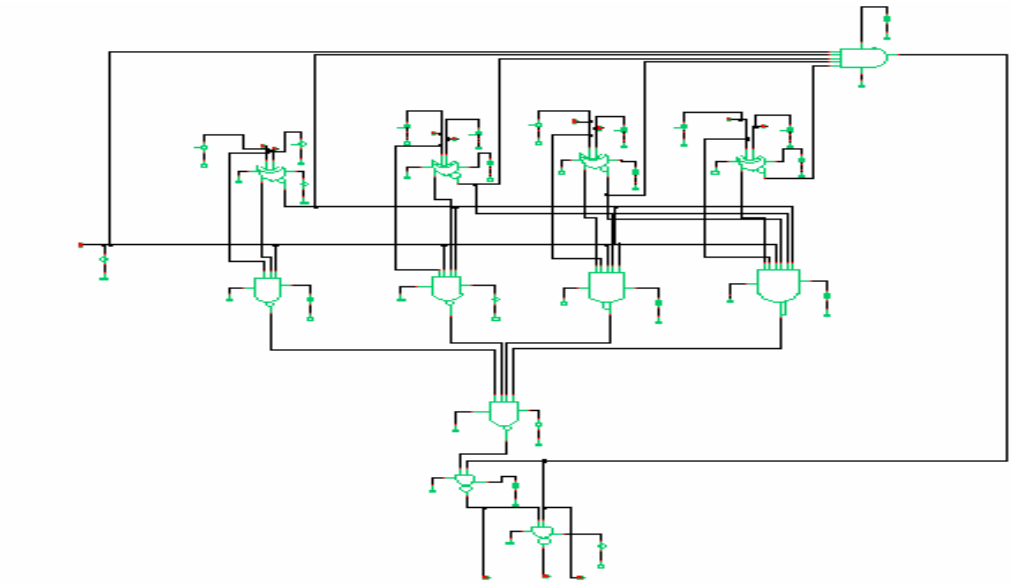

Figure 3.8: Novel 4-bit digital comparator design using cadence

Different input gates shown in fig 3.7 are used as basic building block for 4-bit comparator design shown in Fig 3.8.

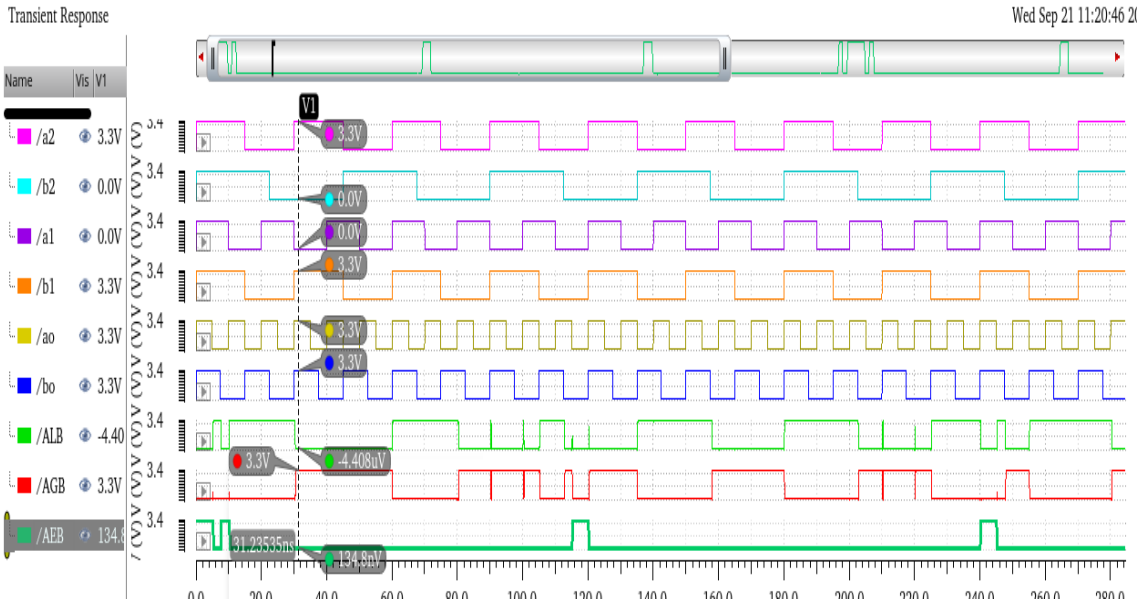

Figure 3.9: Transient response of 4-bit digital comparator

1. Fig 3.9 shows the transient response of 4-bit digital comparator. The 4-bit digital comparator input represented as $a_3a_2a_1a_0$, $b_3b_2b_1b_0$ and the output signals ALB (A less than B), AGB (A larger than B) and AEB (A equal to B) respectively.

2. Vertical cursor of Fig 3.9 shows output of 4-bit digital comparator which is ALB = 0, AGB = 1, AEB = 0 for input combination $a_3a_2a_1a_0 = 1101$, $b_3b_2b_1b_0 = 0011$.

3.3.3 Proposed implementation of 8-bit digital comparator cell

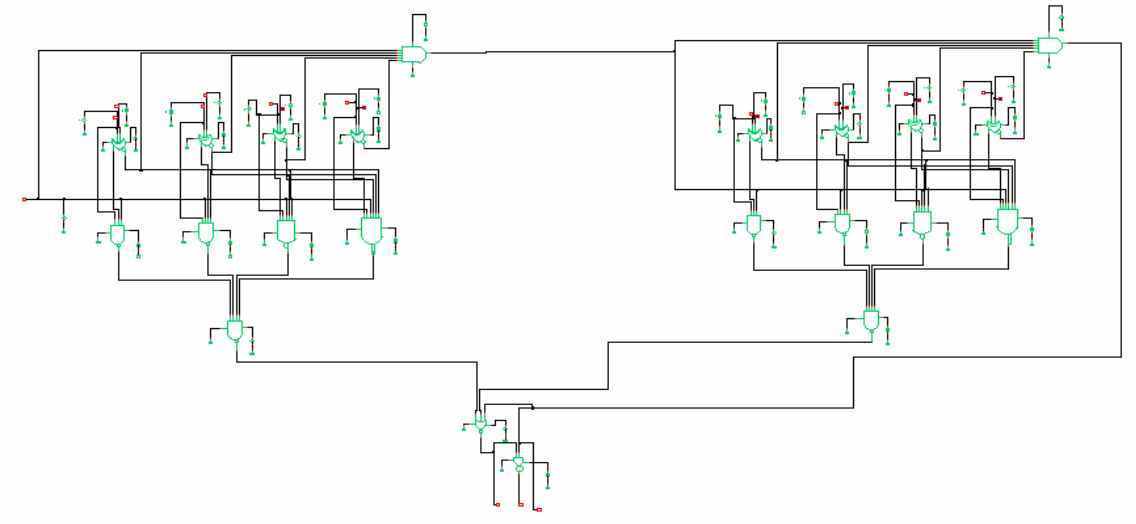

Figure 3.10: Novel 8-bit digital comparator design using cadence

Fig 3.10 shows design of 8-bit digital comparator by connecting two 4-bit digital comparator cell in pipelined order.

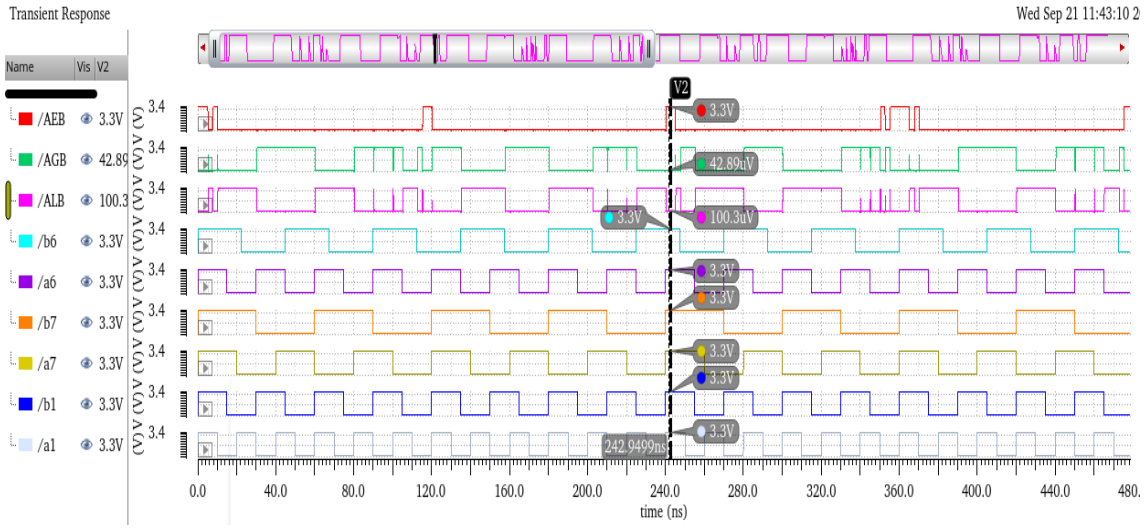

Figure 3.11: Transient response of 8-bit digital comparator

1. Fig 3.11 shows the transient response of 8-bit digital comparator. Input & output of the comparator is in the form of $a_7a_6a_5a_4a_3a_2a_1a_0$, $b_7b_6b_5b_4b_3b_2b_1b_0$ and AGB, ALB, AEB respectively.

2. Vertical cursor of Fig. 3.11 shows output of 8-bit digital comparator which is ALB = 0, AGB = 0, AEB = 1 for input combination $a_7a_6a_5a_4a_3a_2a_1a_0$ = 11111111, $b_7b_6b_5b_4b_3b_2b_1b_0$ = 11111111.

3.3.4 Proposed Implementation of 16-bit digital comparator cell

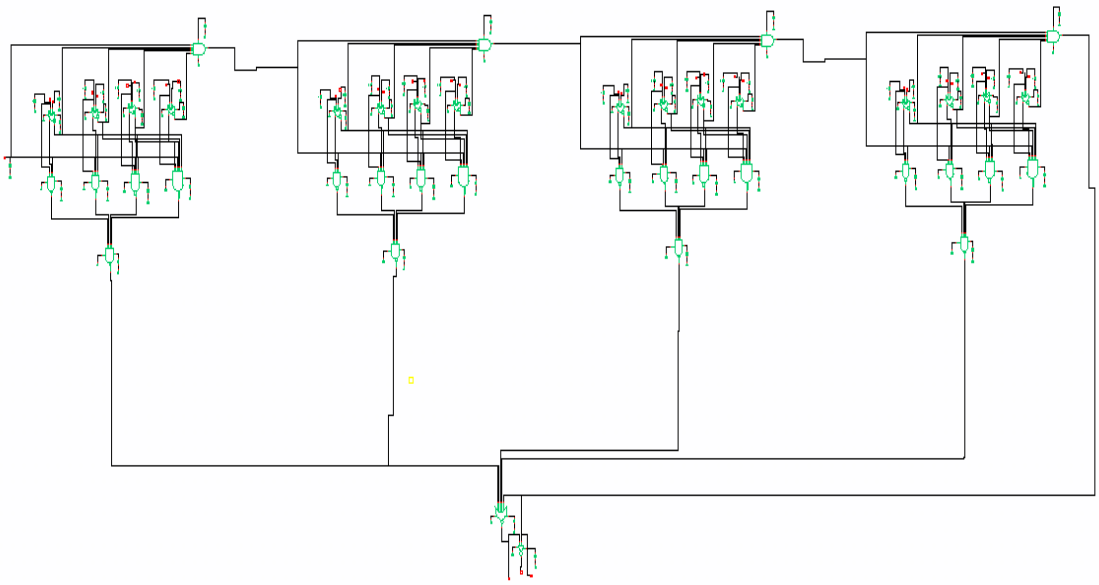

Figure 3.12: Novel 16-bit digital comparator design using cadence

Fig 3.12 shows design of 16-bit digital comparator by connecting four 4-bit digital comparator cell in pipelined order.

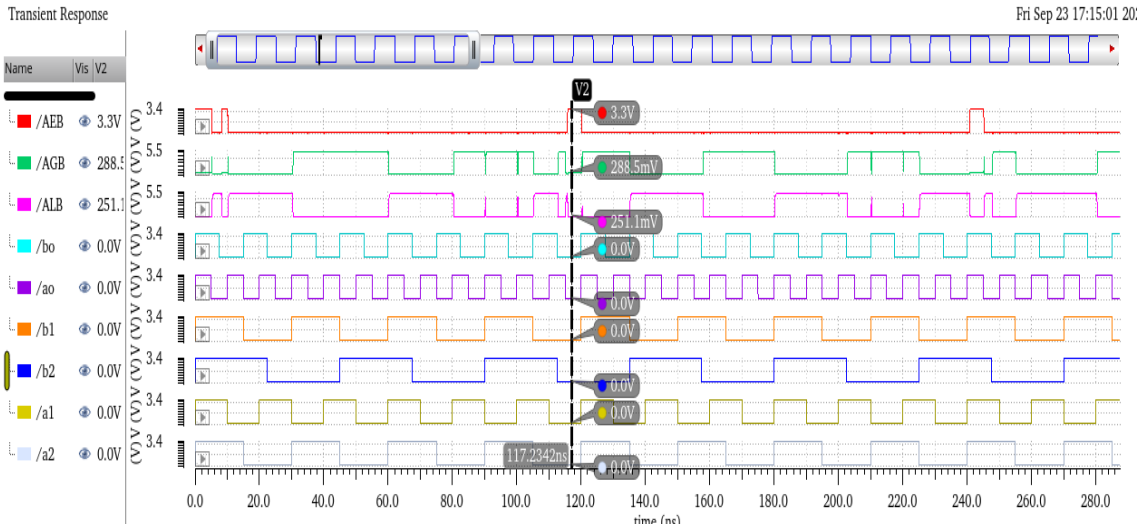

Figure 3.13: Transient response of 16-bit digital comparator

1. Fig 3.13 shows transient response of 16-bit digital comparator. Input & output of 16-bit digital comparator is in the form of $a_{15}a_{14}a_{13}a_{12}...a_3a_2a_1a_0$, $b_{15}b_{14}b_{13}b_{12}...b_3b_2b_1b_0$.

2. Vertical cursor of fig 3.13 shows output of 16-bit digital comparator which is ALB = 0, AGB = 0, AEB = 1 for input combination $a_{15}a_{14}a_{13}a_{12}...a_3a_2a_1a_0$ = 1111...1111, $b_{15}b_{14}b_{13}b_{12}...b_3b_2b_1b_0$= 1111...1111.

3.3.5 Proposed Implementation of 32-bit digital comparator cell

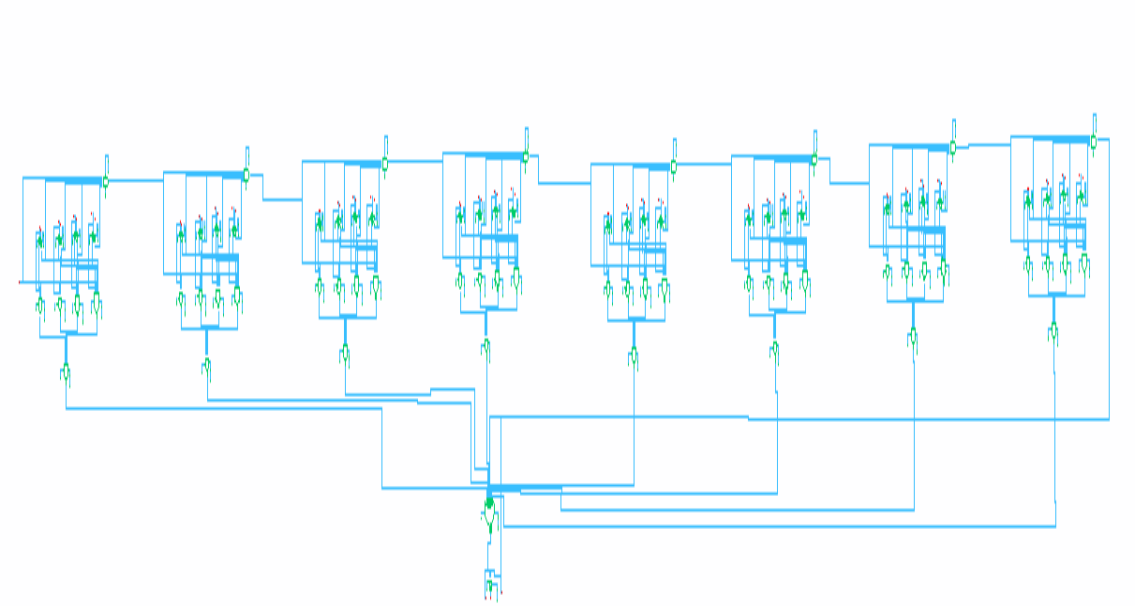

Figure 3.14: Novel 32-bit digital comparator design using cadence

Fig 3.14 shows design of 32-bit digital comparator by connecting eight 4-bit digital comparator cells in pipelined order.

1. Fig 3.15 shows transient response of 32-bit digital comparator.

2. Vertical cursor of fig 3.15 shows output of 32-bit digital comparator which is ALB = 0, AGB = 0, AEB = 1 for input combination $a_{31}a_{30}a_{29}a_{28}...a_3a_2a_1a_0$ = 0000...0000, $b_{31}b_{30}b_{29}b_{28}...b_3b_2b_1b_0$= 0000...0000.

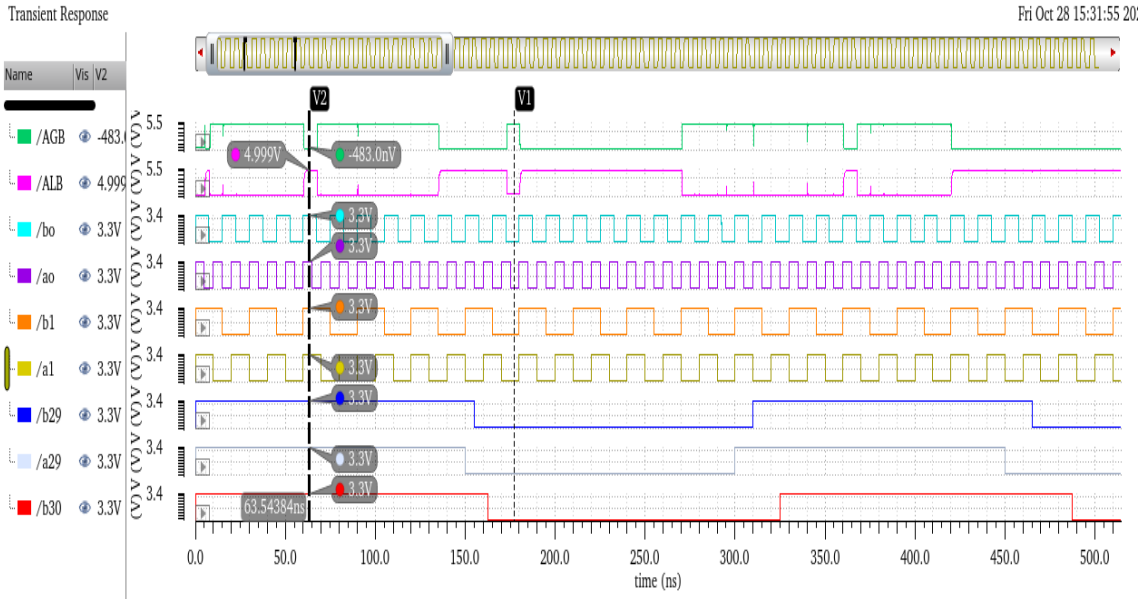

Figure 3.15: Output waveform of Novel 32-bit digital comparator

3.3.6 Proposed Implementation of 64-bit digital comparator cell

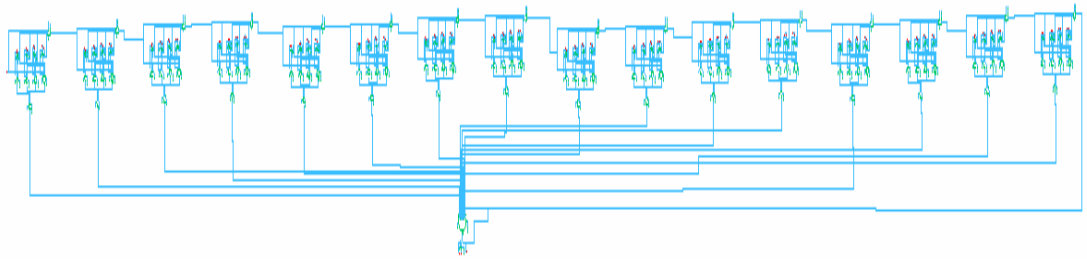

Figure 3.16: Novel 64-bit digital comparator design using cadence

Fig 3.16 shows design of 64-bit digital comparator by connecting sixteen 4-bit digital comparator cells in pipelined order.

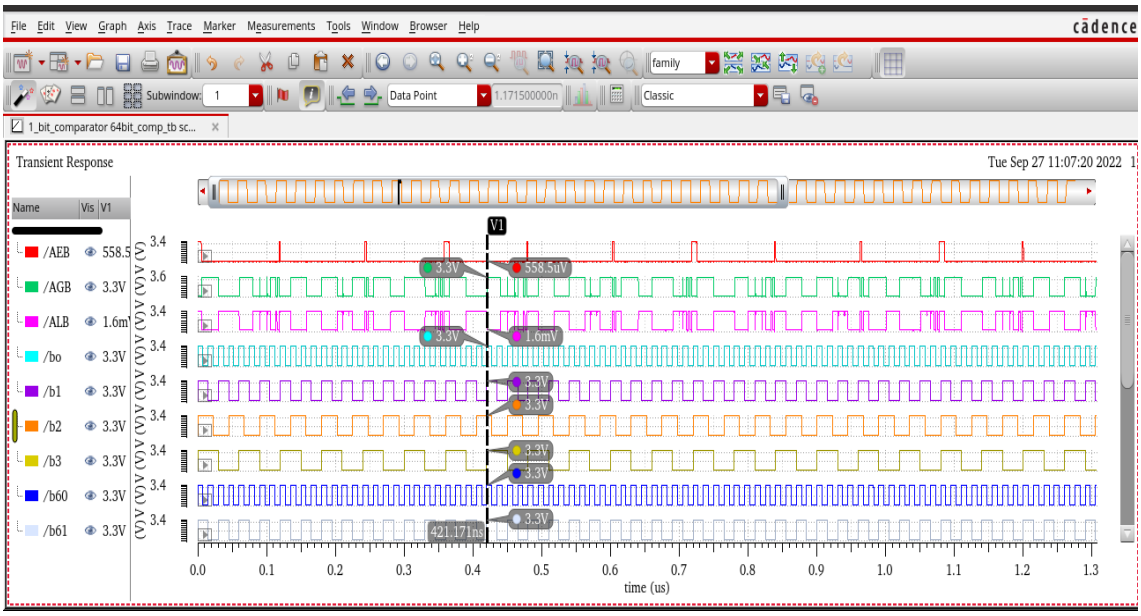

Figure 3.17: Output waveform of Novel 64-bit digital comparator

1. Fig 3.17 shows transient response of 64-bit digital comparator.

2. Vertical cursor of fig 3.17 shows output of 64-bit digital comparator which is ALB = 0, AGB = 0, AEB = 1 for input combination $a_{63}a_{62}a_{61}a_{60}...a_3a_2a_1a_0$ = 1111...1111, $b_{63}b_{62}b_{61}b_{60}...b_3b_2b_1b_0$ = 1111...1111.

3.3.7 Proposed Implementation of 128-bit digital comparator cell

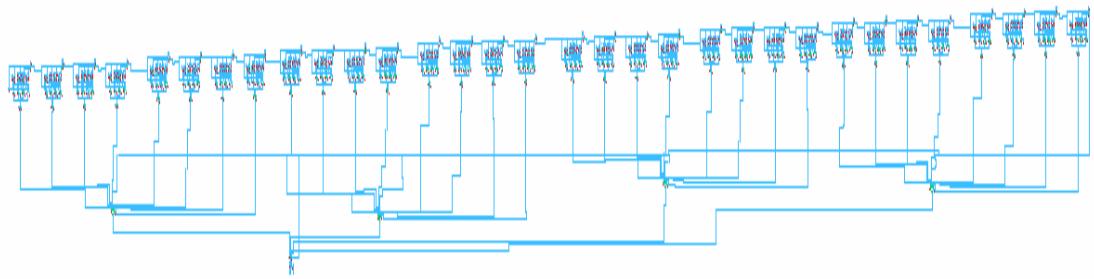

Figure 3.18: Novel 128-bit digital comparator design using cadence

Fig 3.18 shows design of 128-bit digital comparator cell by connecting two 64-bit digital comparator cell in pipelined order.

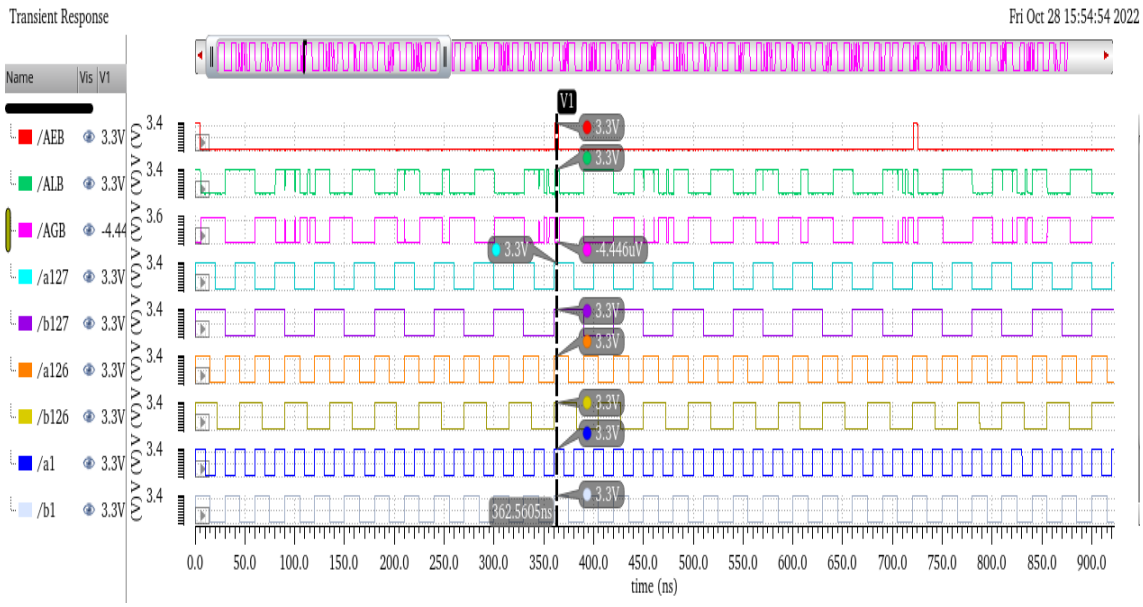

Figure 3.19: Output waveform of Novel 128-bit digital comparator

Fig 3.19 shows transient response for 128-bit digital comparator. Input pattern for 128-bit digital comparator is in the form of $a_{127}a_{126}a_{125}a_{124}...a_3a_2a_1a_0$, $b_{127}b_{126}b_{125}b_{124}...b_3b_2b_1b_0$.

3.4 Structure of bridge full adder

There are two types of full adders in case of logic structure. One is static style and the other is dynamic style. Static full adders are commonly more reliable, simpler and of lower power than dynamic ones. Dynamic is an alternative logic style to design a logic function. It has some advantages in comparison with static mode such as faster switching speeds, no static power consumption, non-ratioed logic, full swing voltage levels and less number of transistors. Bridge circuits provide a conditional conjunction between two circuit nodes.

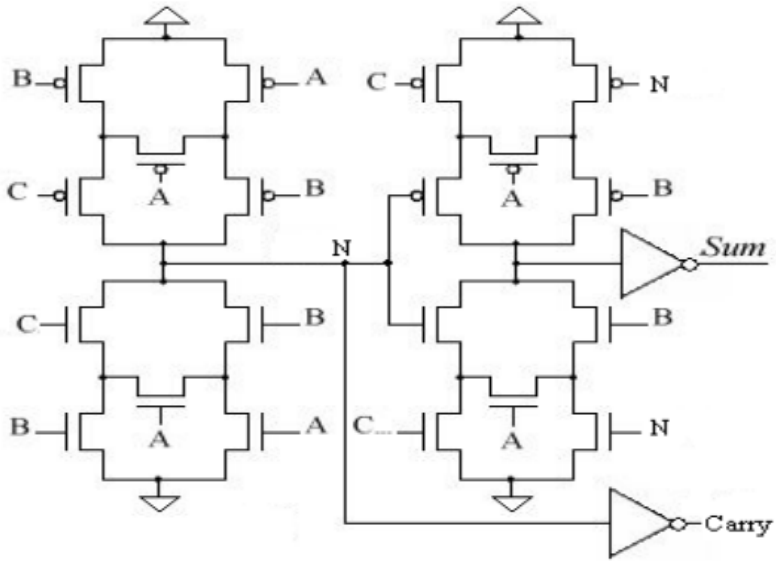

Figure 3.20: 24-Transistor bridge full adder [9]

Fig. 3.20 shows the bridge full adder. The bridge style circuits is classified into two structures both are fully-symmetric. In bridge full adder a bridge circuit generates Carry and another bridge circuit is utilized in series with the prior one to generate Sum. The main purpose of comparator design using bridge full adder is carry and sum signals are produced in a parallel way.

3.5 Implementation of bridge full adder

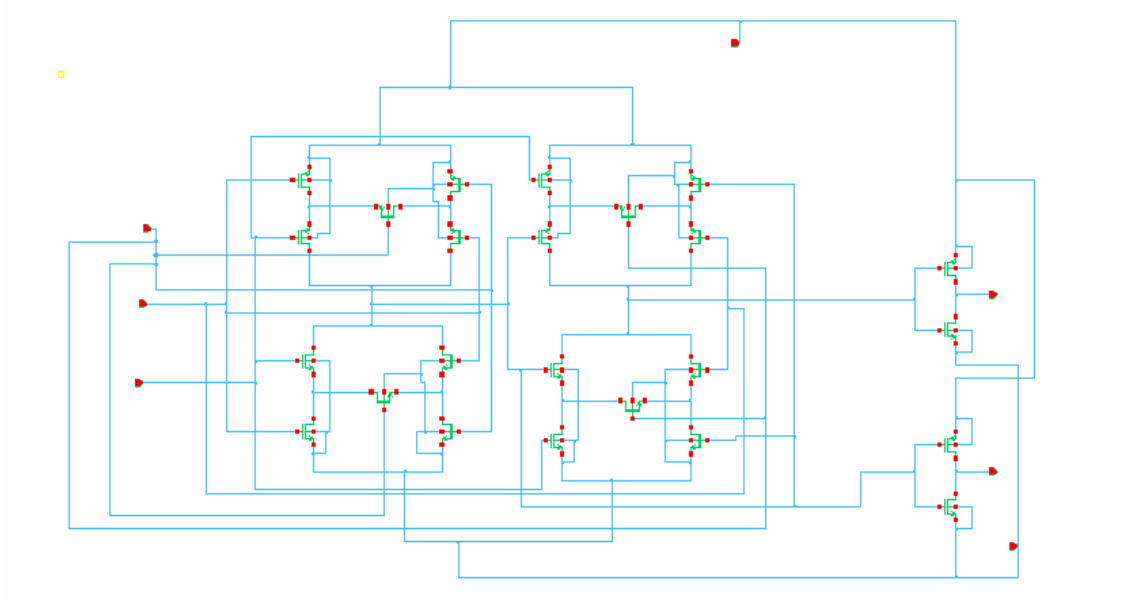

Figure 3.21: Bridge Full adder cell design using cadence

The bridge full adder has 24 transistors shown in Fig. 3.21.

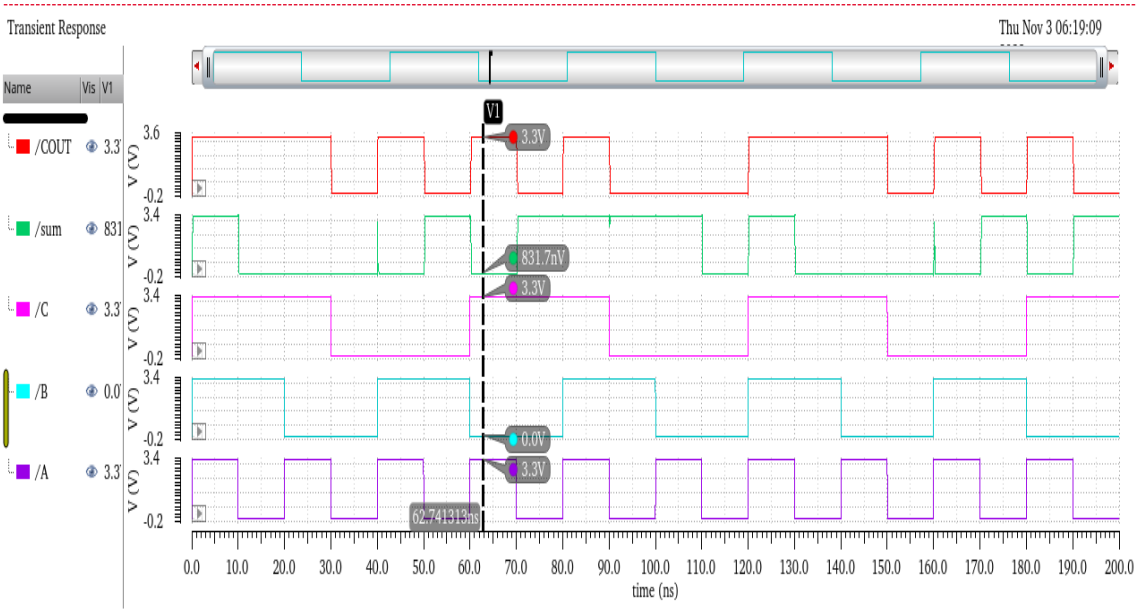

Figure 3.22: Output waveform of bridge full adder

Transient response full adder, based on bridge structure is shown in fig. 3.22. From vertical cursor of fig. 3.22 output of full adder is Sum =0 and C_{out} =1 for input combination A = 1, B = 0, C_{in} = 1.

3.6 Implementation of 4-bit comparator using bridge full adder

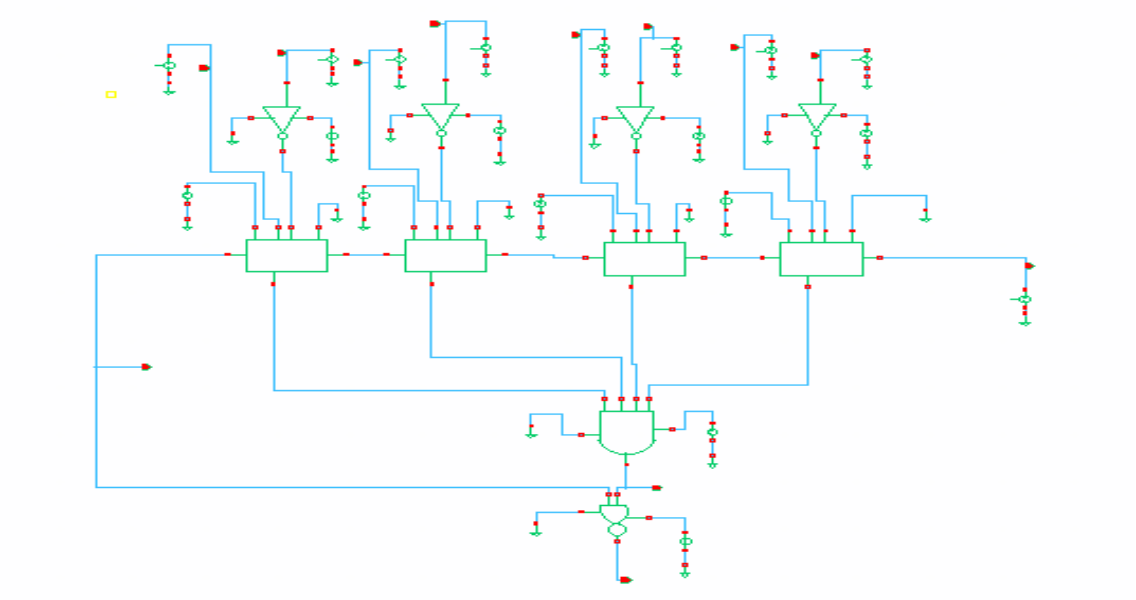

Figure 3.23: Schematic of 4-bit comparator design using bridge FA

1. Fig 3.23 shows implementation of 4-bit comparator. This implementation requires four 1-bit FA, one 4-input AND gate and one 2-input NOR gate. Input of each FA is in the form of a_0b_0, a_1b_1 and for each FA output is in the form of sum and carry out.

2. The output of each full adder fed into the AND gate, determines if an AEB is present.

3. The last FA's output carry decides if AGB. The output of NOR gate determines ALB.

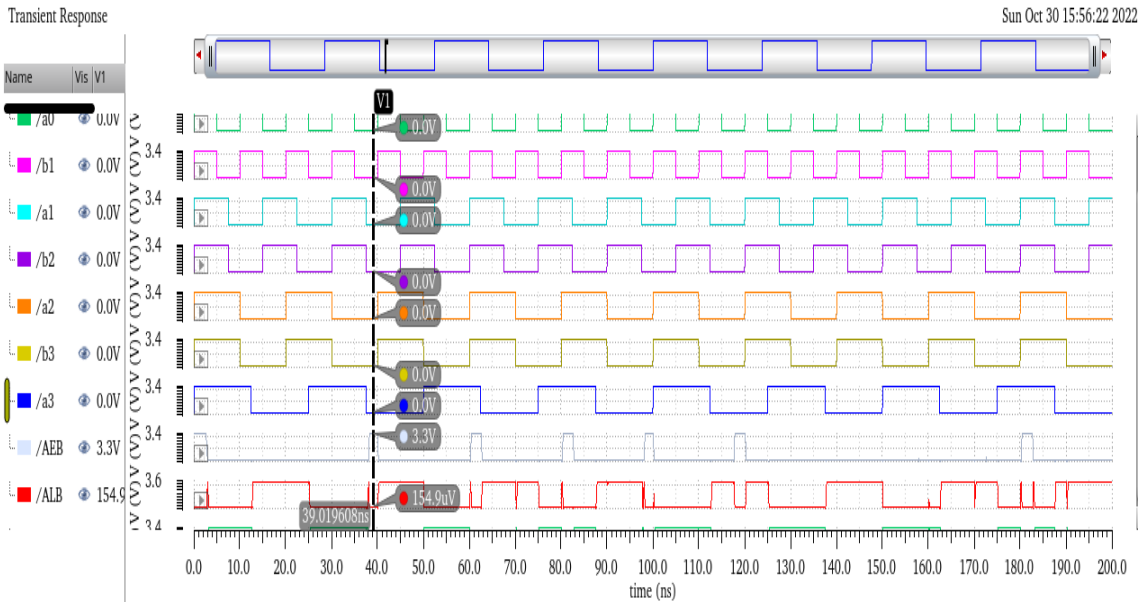

Figure 3.24: 4-Bit comparator transient response using bridge FA

Fig 3.24 shows the transient response of 4-bit digital comparator design using bridge FA. The output of the 4-bit digital comparator in Fig. 3.24 is AEB = 1, ALB = 0, AGB = 0 for input combination $a_3a_2a_1a_0 = 0000$, $b_3b_2b_1b_0 = 0000$.

3.7 Implementation of 8-bit comparator using bridge full adder

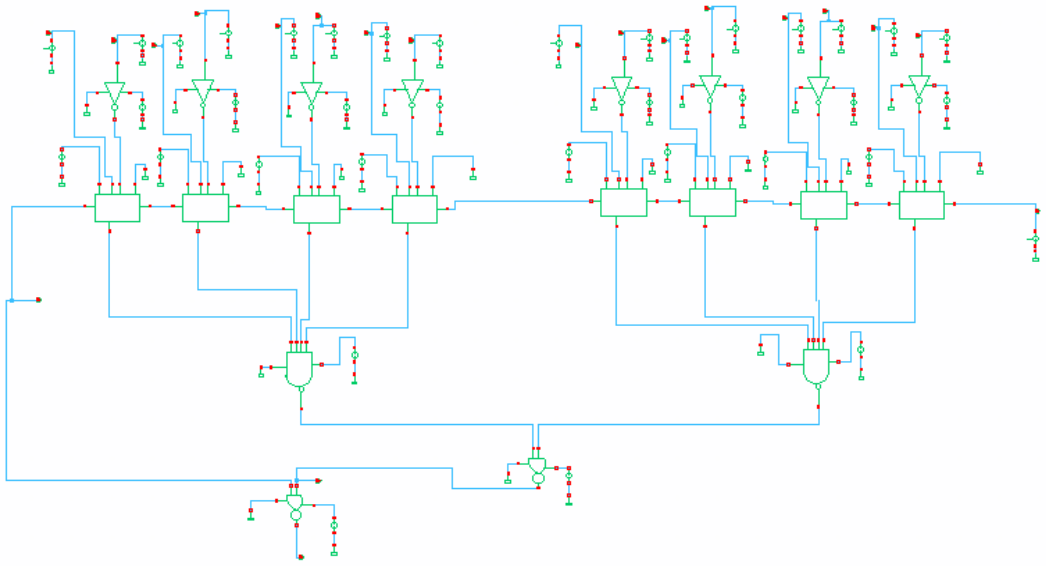

Figure 3.25: Schematic of 8-bit comparator design using bridge FA

Fig 3.25 shows the design of 8-bit digital comparator by connecting two 4-bit digital comparator cells in pipelined order.

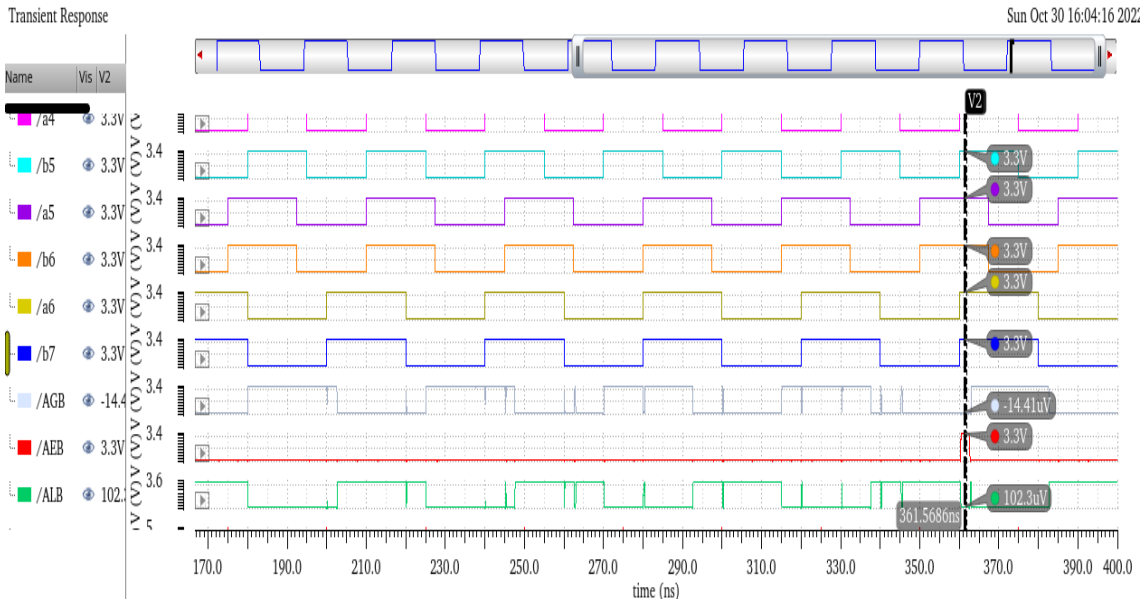

Figure 3.26: 8-Bit comparator transient response using bridge FA

Figure 3.26 shows the transient response of an 8-bit digital comparator designed using bridge FA. The output of the 8-bit digital comparator in Fig. 3.26 is AEB = 1, ALB = 0, AGB = 0 for input combination $a_7a_6a_5a_4a_3a_2a_1a_0$ = 11111111, $b_7b_6b_5b_4b_3b_2b_1b_0$ = 11111111.

3.8 Implementation of 16-bit comparator using full adder

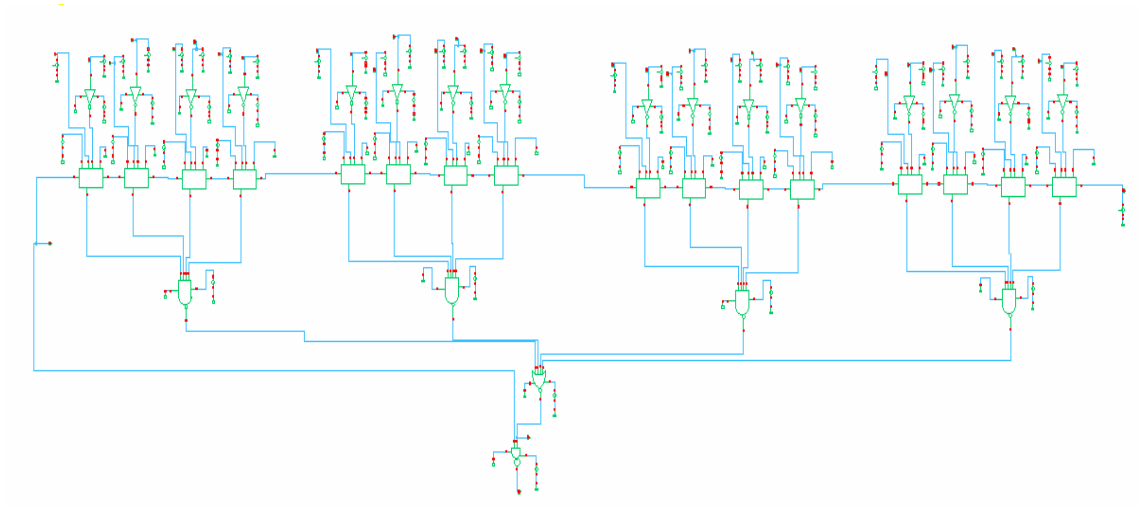

Figure 3.27: Schematic of 16-bit comparator design using bridge FA

Fig 3.27 shows the design of 16-bit digital comparator by connecting four 4-bit digital comparator cells in pipelined order.

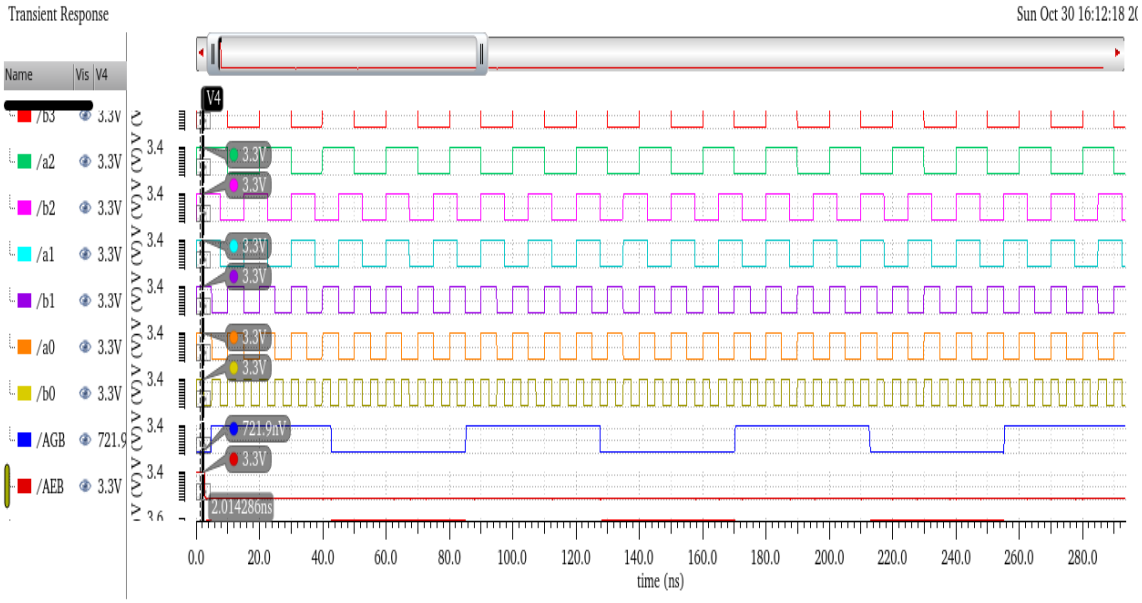

Figure 3.28: 16-Bit comparator transient response using bridge FA

The transient response of a 16-bit digital comparator using bridge FA is shown in fig. 3.28. The output of the 16-bit digital comparator in Fig. 3.28 is AEB = 1, ALB = 0, and AGB = 0 for the input combination $a_{15}a_{14}a_{13}a_{12}...a_3a_2a_1a_0$ = 1111...1111, $b_{15}b_{14}b_{13}b_{12}...b_3b_2b_1b_0$= 1111...1111.

3.9 Implementation of 32-bit comparator using full adder

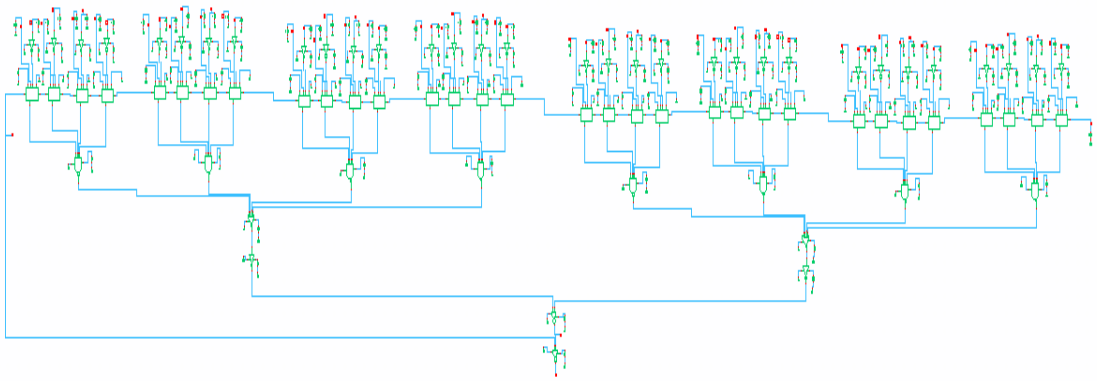

Figure 3.29: 32-Bit comparator design schematic using bridge FA

Fig 3.29 shows the design of 32-bit digital comparator by connecting eight 4-bit digital comparator cells in pipelined order.

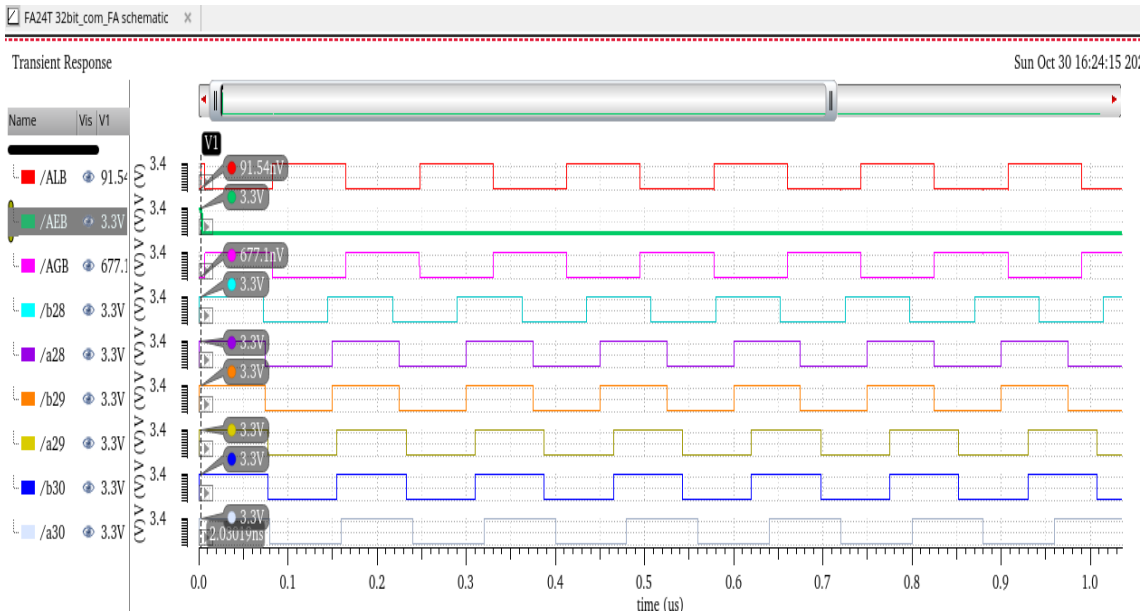

Figure 3.30: Transient response of 32-bit comparator design using bridge FA

Fig 3.30 shows the transient response of 32-bit digital comparator design using bridge FA. The output of the 32-bit digital comparator in Fig. 3.30 is AEB = 1, ALB = 0, and AGB = 0 for the input combination $a_{31}a_{30}a_{29}a_{28}...a_3a_2a_1a_0$ = 1111...1111, $b_{31}b_{30}b_{29}b_{28}...b_3b_2b_1b_0$= 1111...1111.

3.10 Implementation of 64-bit comparator using full adder

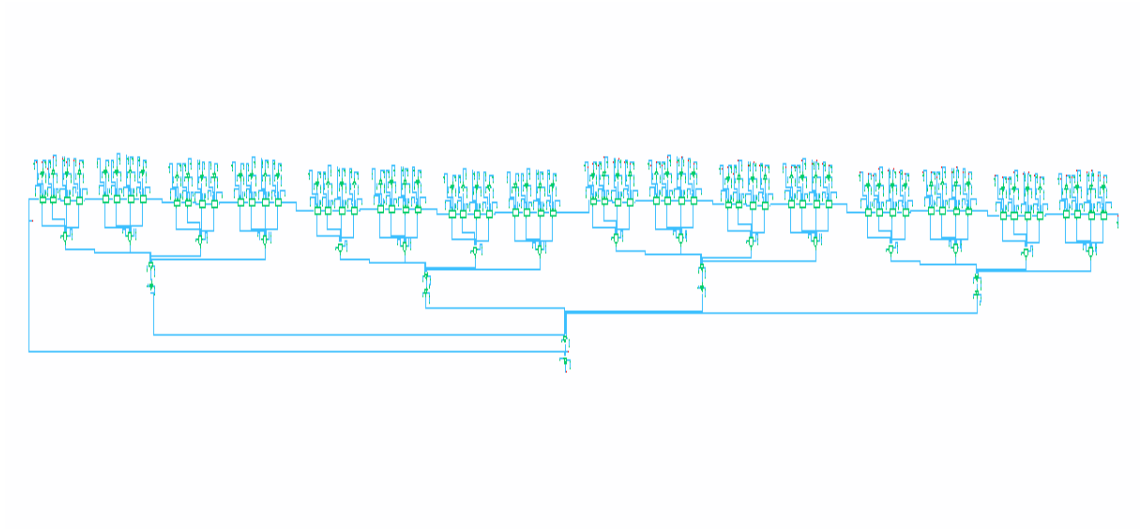

Figure 3.31: Schematic of 64-bit comparator design using bridge FA

Fig 3.31 shows the design of 64-bit digital comparator cell by connecting sixteen 4-bit digital comparator cells in pipelined order.

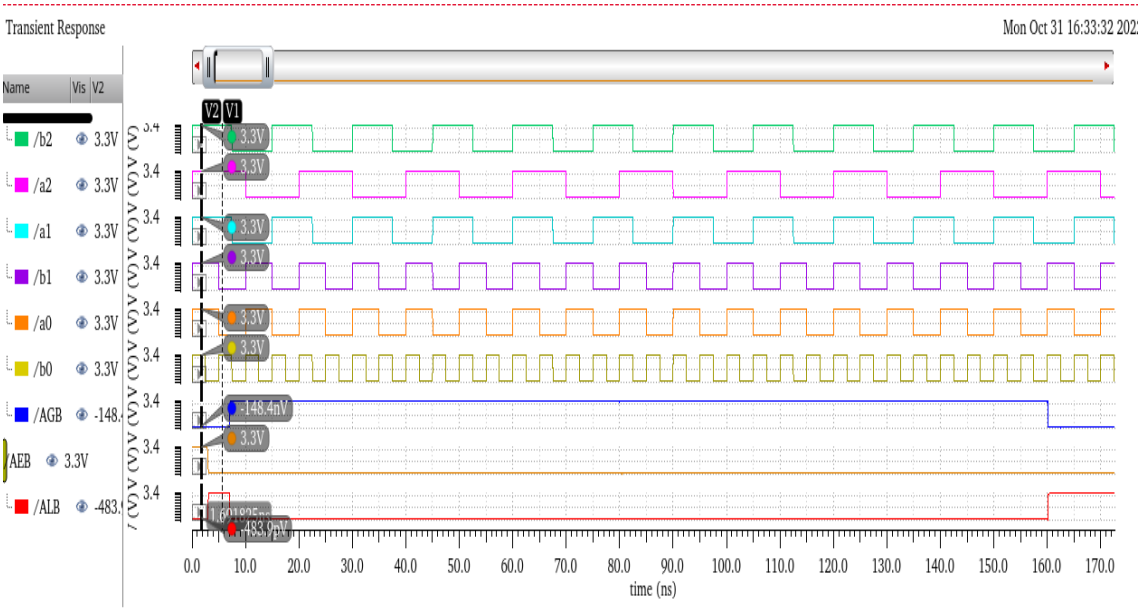

Figure 3.32: Transient response of 64-bit comparator design using bridge FA

Fig 3.32 shows the transient response of 64-bit digital comparator design using bridge FA. The output of the 64-bit digital comparator in Fig. 3.32 is AEB = 1, ALB = 0, AGB = 0 for input combination $a_{63}a_{62}a_{61}a_{60}...a_3a_2a_1a_0$ = 1111...1111, $b_{63}b_{62}b_{61}b_{60}...b_3b_2b_1b_0$ = 1111...1111.

3.11 Implementation of 128-bit comparator using full adder

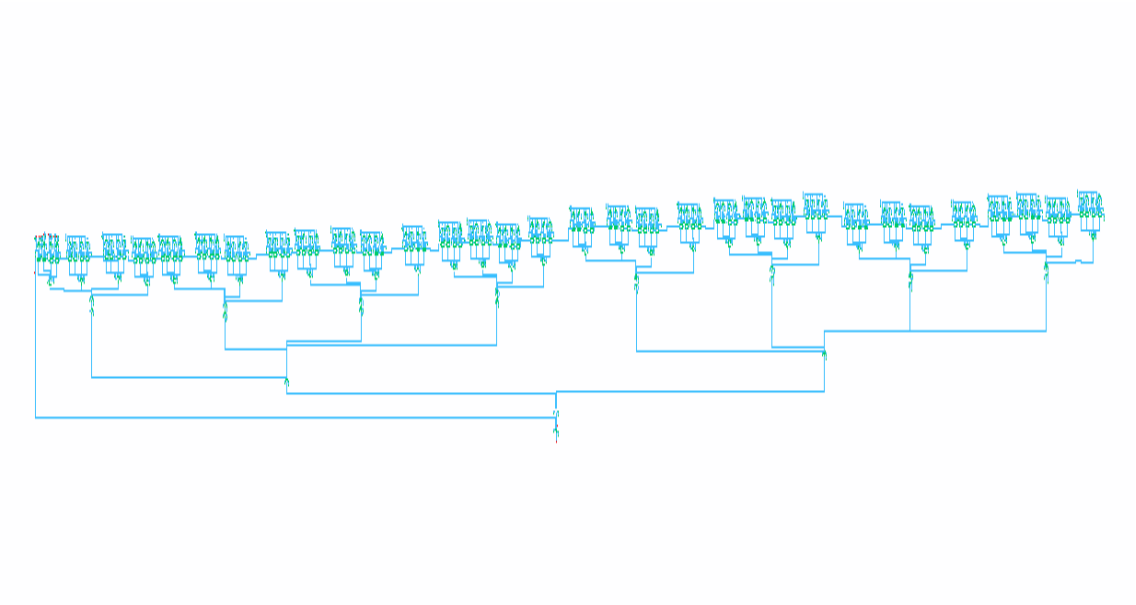

Figure 3.33: Schematic of 128-bit comparator design using bridge FA

Fig 3.33 shows the design of 128-bit digital comparator cell by connecting two 64-bit digital comparator cells in pipelined order.

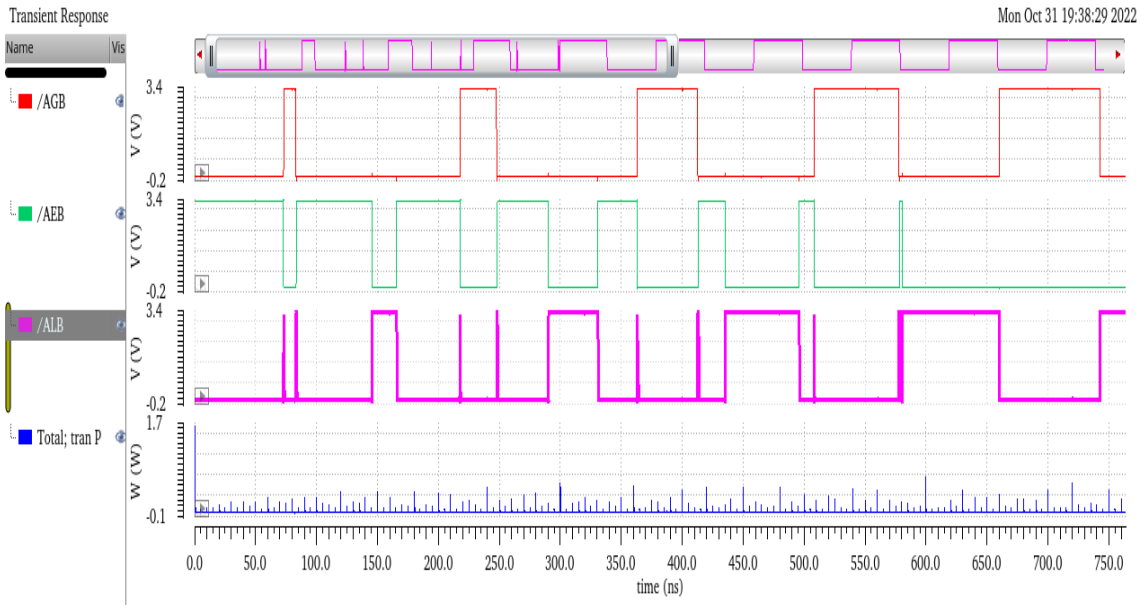

Figure 3.34: Transient response of 128-bit comparator design using bridge FA

Fig. 3.34 shows the transient response for 128-bit digital comparator. 128-Bit digital comparator's input represented as $a_{127}a_{126}a_{125}a_{124}...a_3a_2a_1a_0$ and $b_{127}b_{126}b_{125}b_{124}...b_3b_2b_1b_0$.

Chapter 4

Area, power consumption and operating speed estimations

4.1 Analysis of area

In the proposed comparator area is calculated by determining the total number of cells required in the various Sets and then converting the logic cell count into the total number of transistors. Equation (4.1) and (4.2) show the total number of logic cells required for CEM (C_{CEM}) and FM (C_{FM}).

$$C_{CEM} = (N \times (Set\,1\,cell)) + (\frac{N}{4} \times Set\,2\,cell)) + (N \times (Set\,3\,cell)) + (\frac{N}{4} \times (Set\,4\,cell)) \tag{4.1}$$

$$C_{FM} = (2 \times (Set\,5\,cell)) \tag{4.2}$$

Tables 4.1 and 4.2 show the cumulative number of cells and transistors required for various bitwidths in CEM.

Bitwidth and bit	Set 1 (Number of Exor-nor cells in total)	Set 2 (Number of AND cells in total)	Set 3 (Number of NAND cells in total)	Set 4 (Number of NAND cells in total)
16	16	3	16	4
24	24	5	24	6
32	32	7	32	8
64	64	15	64	16
128	128	31	128	32

Table 4.1: Estimated number of logic cells required in comparison evaluation module

Bitwidth and bit	Set 1 (Total number of transistors)	Set 2 (Total number of transistors)	Set 3 (Total number of transistors)	Set 4 (Total number of transistors)	Overall transistor count
16	7×16	12×3	12×16	8 ×4	372
24	7×24	12×5	12×24	8×6	564
32	7×32	12×7	12×32	8×8	756
64	7×64	12×15	12×64	8×16	1524
128	7×128	12×31	12×128	8×32	3060

Table 4.2: Overall transistor count for various comparator bitwidths in comparison evaluation module

4.2 Consumption of power

Power losse occurs in the digital circuits due to switching operation in the circuit. By reducing switching operations minimises overall average power dissipation.

1. In Set 1, there is no power savings because the input operands activate all of the logic cells present in Set 1.

2. The logic cell in Set 2 that acts on the termination bits received from the most significant nibble partition of Set 1 is always active.

3. Set 3 contains cells that combine the results of Set 1 and Set 2. These outputs are then utilised to activate or deactivate cells at certain bitwise places. As a result, only one cell in Set 3 has switching activity, resulting in a considerable reduction in power dissipation.

4. In Set 3 single active logic cell activates a succeeding logic cell present in Set 4. As a result, only one cell of Set 4 will be active, resulting in further decrease in power consumption.

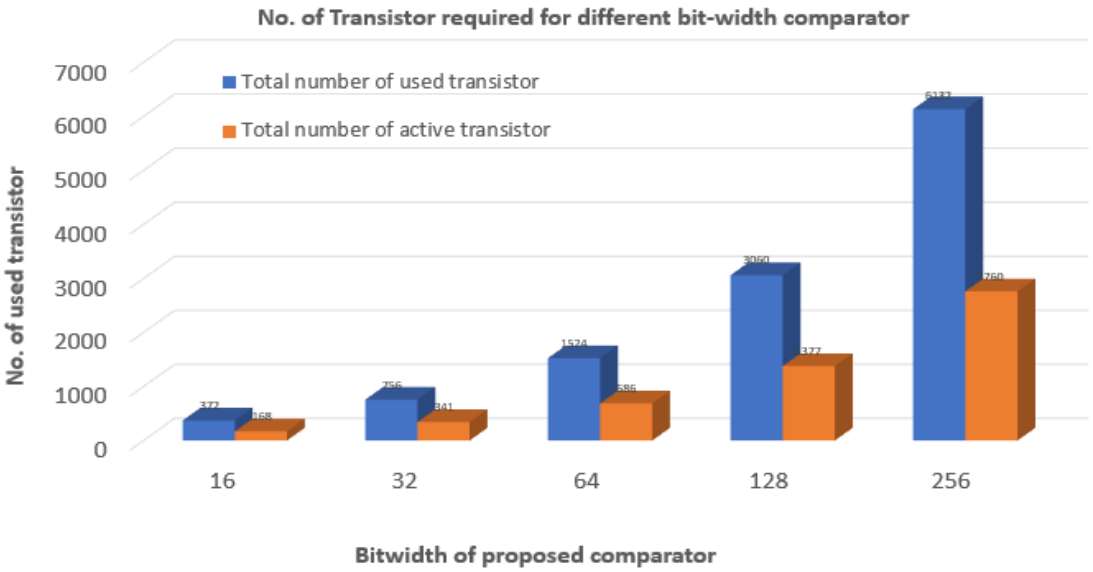

Figure 4.1: Total number of operational transistors for various bitwidths.

Figure 4.1 shows a graphical plot of comparator bitwidth vs number of transistors. The first blue colour bar represents the overall number of transistors used in the comparator design, and the second orange colour bar represents the overall number of transistors that are active during comparison.

4.3 Speed of operation

The critical delay is the sum of all cell delays encountered along the critical path. The total delay encountered in the critical path becomes the appropriate minimum time period of the input, which determines the maximum operating frequency. The CEM total path delay (D_{CEM}) can be mathematically represented as

$$D_{CEM} = D_{Set1} + D_{Set2} + D_{Set3} + D_{Set4} \tag{4.3}$$

The three terms D_{Set1}, D_{Set3}, and D_{Set4} are equal to the delay of a single activated cell (D_U)

$$D_{Set2} = (\frac{N}{4}) \times D_U \tag{4.4}$$

$$D_{CEM} = D_U + (\frac{N}{4}) \times D_U + D_U + D_U \tag{4.5}$$

where N is the bitwidth of the operand The delay caused by final module (D_{FM}) can be expressed as

$$D_{FM} = 2 \times D_U \tag{4.6}$$

The total delay of comparator expressed as

$$D_T = D_{CEM} + D_{FM} \tag{4.7}$$

$$D_T = 5 \times D_U + (\frac{N}{4}) \times D_U \tag{4.8}$$

Bitwidth, bit	Worst-case operands
4	A = 0000 and B = 0000
4	A = 0001 and B = 0000
4	A = 0000 and B = 0001
4	A = 0001 and B = 0001
8	A = 00000000 and B = 00000000
8	A = 00000001 and B = 00000000
8	A = 00000000 and B = 00000001
8	A = 00000001 and B = 00000001
⋮	⋮
64	A = 0000...0000 and B = 0000...0000
64	A = 0000...0001 and B = 0000...0000
64	A = 0000...0000 and B = 0000...0001
64	A = 0000...0001 and B = 0000...0001

Figure 4.2: Bitwidths for Worst-case input operand

Fig. 4.2 shows worst case input pattern at which maximum number of transistor are active which is useful for computation of maximum delay and power consumption.

4.4 Results and discussion

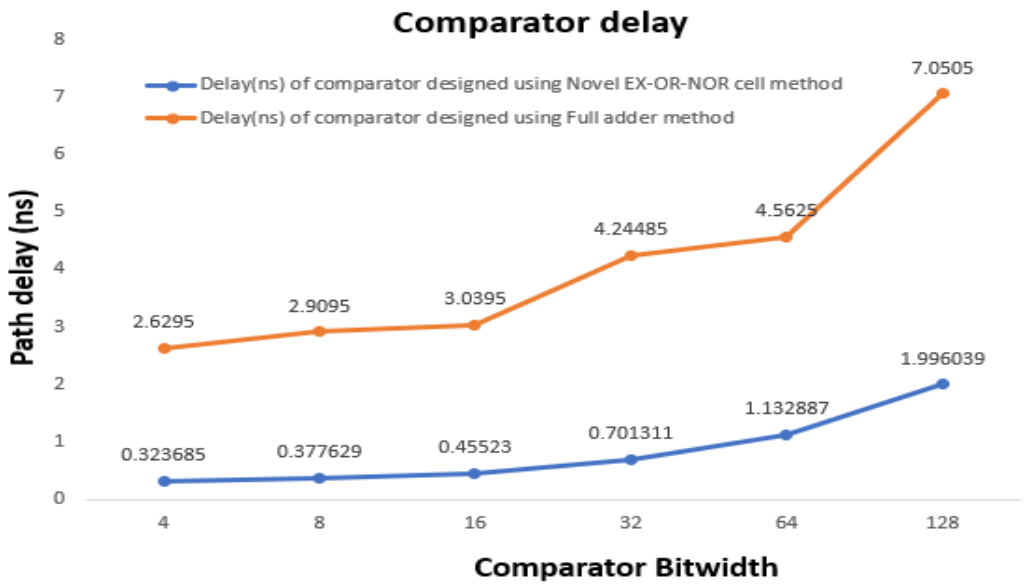

Figure 4.3: Critical path delay of digital comparator

Fig. 4.3. shows The maximum comparator bitwidths vs input-output latency. According to this figure, the comparator designed using the Exor-nor cell method and the comparator designed using the bridge full adder method have a maximum delay of 1.9960 ns and 7.0505 ns respectively for the worst-case input pattern for 128- bit comparison.

Bitwidths of operands used for execution	Maximum delay of comparator design using Novel Exor-nor cell method, ns	Maximum delay of comparator design using bridge full adder method, ns
4	0.323682	2.6295
8	0.377629	2.9095
16	0.485523	3.0395
32	0.701311	4.2448
64	1.132887	4.5625
128	1.996039	7.0505

Table 4.3: Maximum delay of comparator

Table. 4.3 shows transient responses of the comparator for various bitwidths computed for worst-case input operands

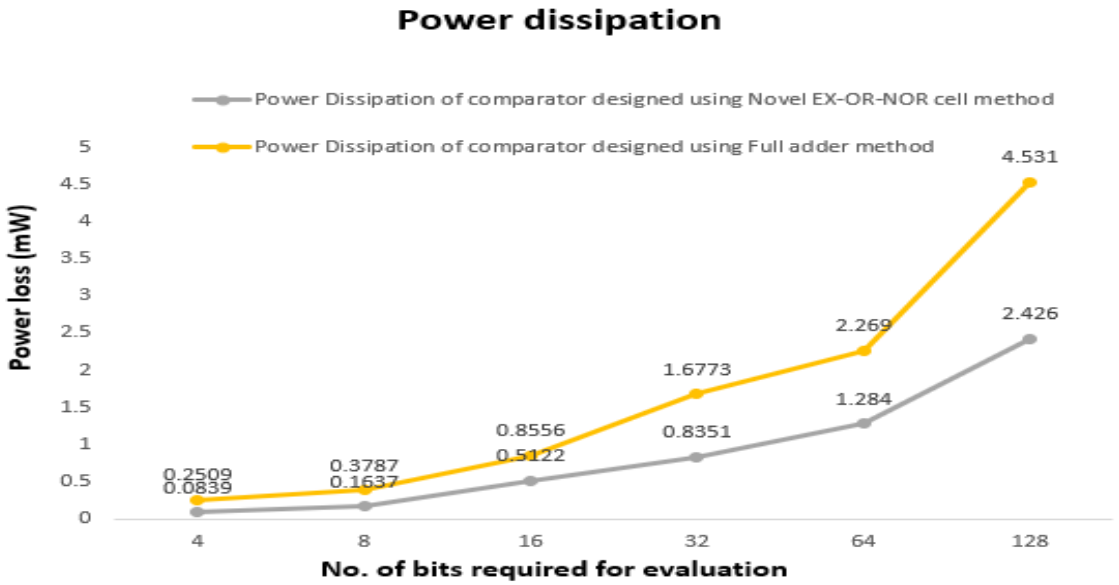

Figure 4.4: Power dissipation vs bitwidth

Fig. 4.4 shows the graphical representation of number of bits needed versus worst-case power dissipation. The first black colour line represents power dissipation of comparator design using Novel Exor-nor cell method, and the second yellow colour line represents power dissipation of comparator design using full adder method.

Bitwidth	Maximum power loss of comparator design using Novel Exor-nor cell method, mW	Maximum power loss of comparator design using bridge full adder method, mW
4	0.0839	0.2509
8	0.1637	0.3787
16	0.5122	0.8536
32	0.8351	1.6773
64	1.284	2.269
128	2.426	4.531

Table 4.4: Maximum power dissipation of comparator for different bitwidths

Table. 4.4 represents maximum power dissipation of the comparator for various bitwidths computed for worst-case input operands.

Chapter 5

Conclusion

In this project, Comparator designed using Novel Exor-nor cell method has a maximum speed of operation of 0.501 GHz while the comparator designed using bridge full adder method has a maximum speed of operation of 0.1418 GHz for the worst-case pattern of input for comparing two bit-streams of 128 bits.

Comparator designed using Novel Exor-nor cell method has a worst power dissipation of 2.426 mW and comparator designed using bridge full adder method has a worst dissipation of power is 4.531 mW in the worst-case input pattern for 128-bit comparison.

From simulation results we can conclude that the comparator designed using the Exor-nor cell method has a higher operating frequency, less power consumption, and smaller delay than the comparator designed using the bridge full adder method.

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