Cpr E 281 HW12 SOLUTION

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Fifteenth Week

P1.

(a) Four states are used:

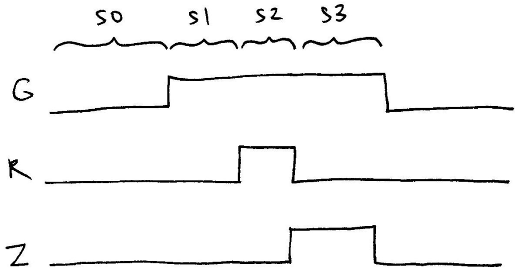
S0: idle

S1: G pushed, waiting for R

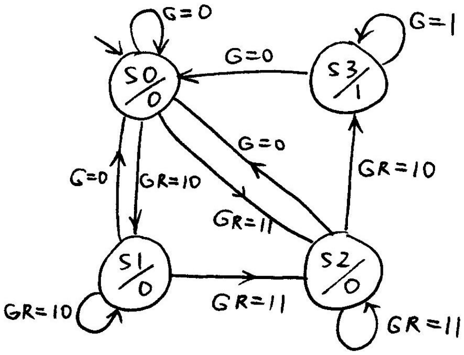
S2: G pushed, R pushed

S3: G pushed, R pushed and released (Z=1)

The four states are illustrated by the following figure:



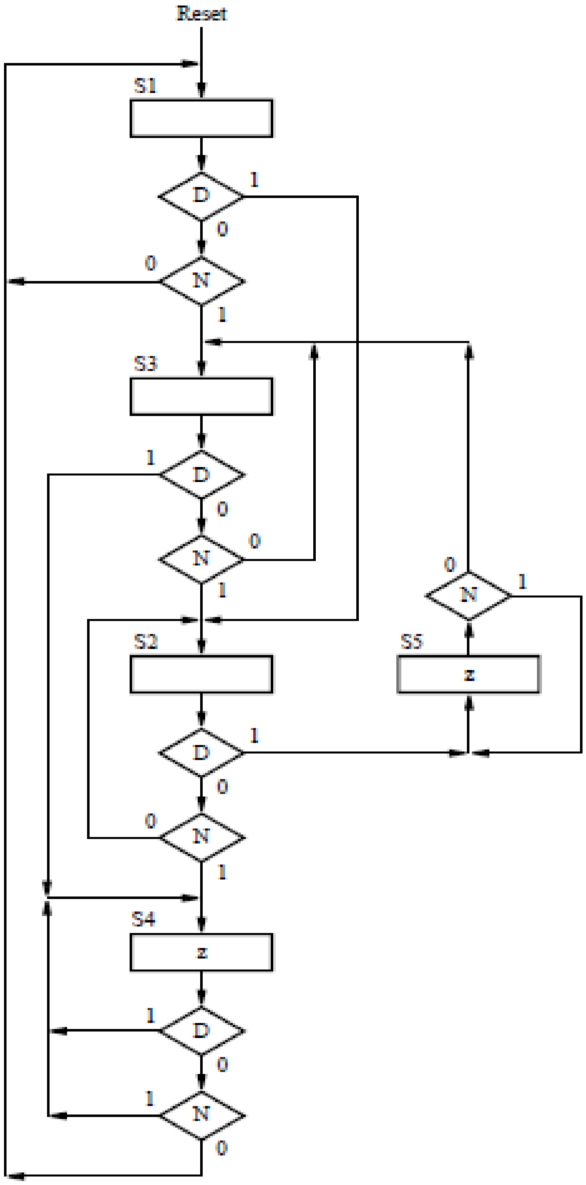
The state transition diagram is as follows:



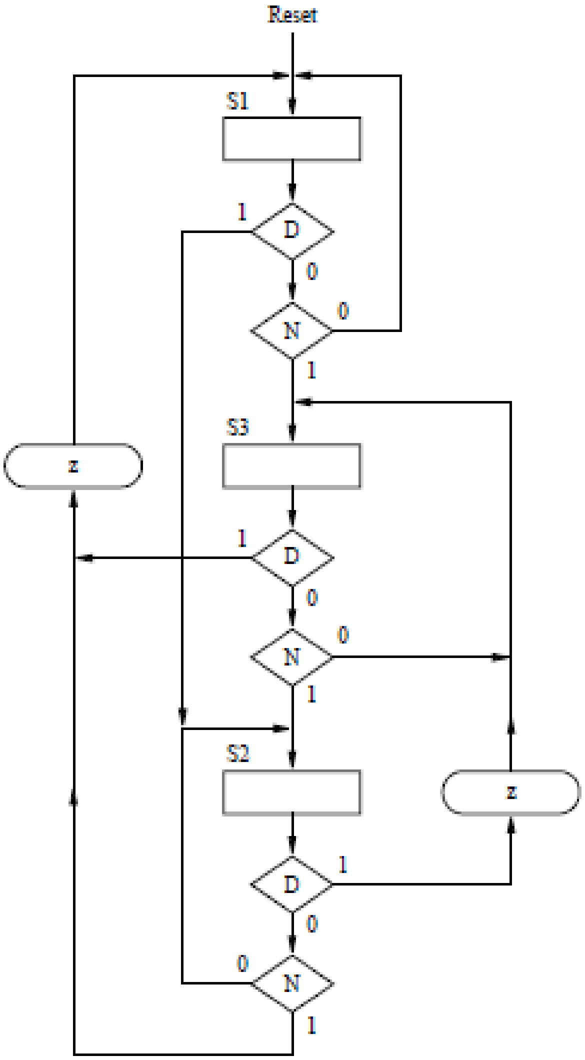
(b)

Clock edge	GR at clock edge	State after clock edge	Output Z after clock edge
1	00	S0	0
2	10	S1	0
3	11	S2	0
4	01	S0	0
5	00	S0	0
6	10	S1	0
7	10	S1	0
8	11	S2	0
9	10	S3	1
10	11	S3	1
11	10	S3	1
12	00	S0	0

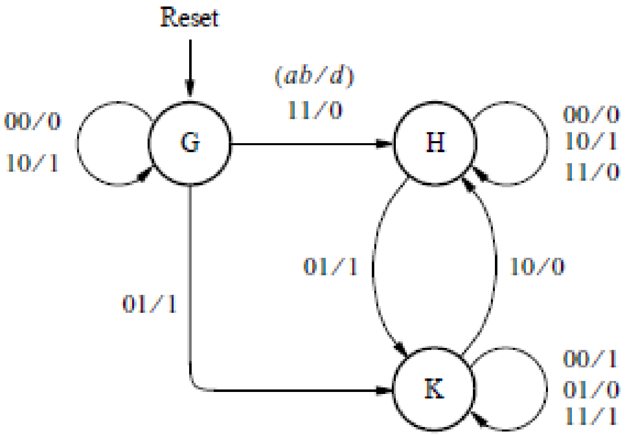
P2. An ASM chart for the FSM in the first figure is



An ASM chart for the FSM in the second figure is



P3. We can use the scheme given in Figure 6.39. However, instead of adding the vector B in its existing form, we need its 2's complement. This can be done by using the rule for finding 2's complements, in Section 3.3.1. Rather than generating the 2's complement of B explicitly, we can change the specification of the Adder FSM to deal with the bits of B using the rule. As a straightforward attempt, we can introduce an extra state to complement the incoming bits of B after the first 1 has been detected. This leads to the following state diagram:



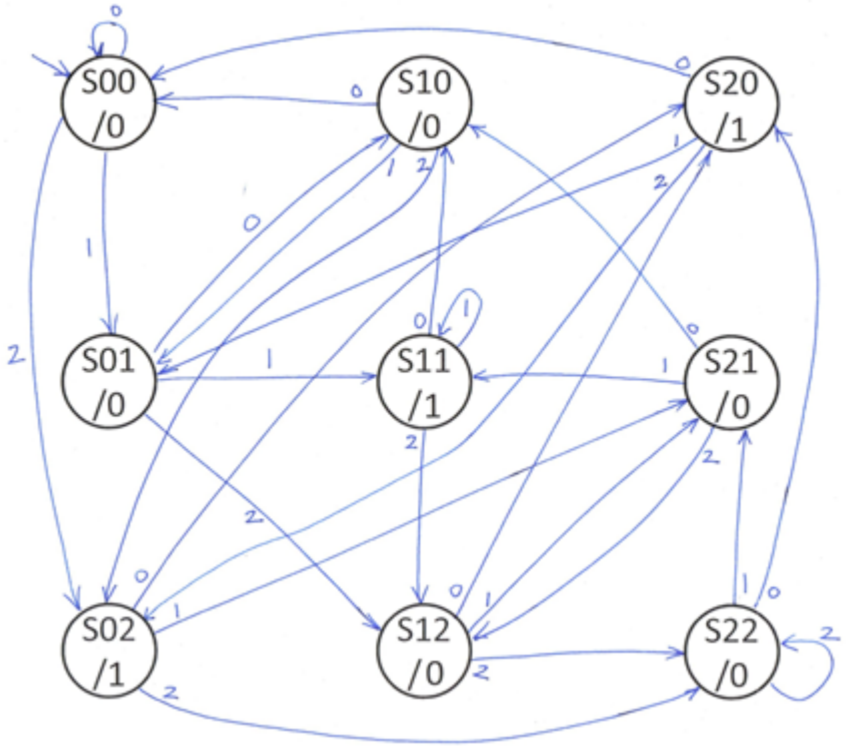
P4

A minimum state table is shown below. We assume that the 3-bit patterns do not overlap.

Present state	Next state		Output p
	$w = 0$	$w = 1$	
A	B	C	0
B	D	E	0
C	E	D	0
D	A	F	0
E	F	A	0
F	B	C	1

P5. Since we are using the minimum number of state bits, $k = log_2\, n$, then there are n choices for the first state code, $n - 1$ for the second state code, and so on, leading to n! possible combinations of state codes.

P6.


S00 /0
S10 /0
S20 /1
S01 /0
S11 /1
S21 /0
S02 /1
S12 /0
S22 /0