Cpr E 281 HW10 SOLUTION

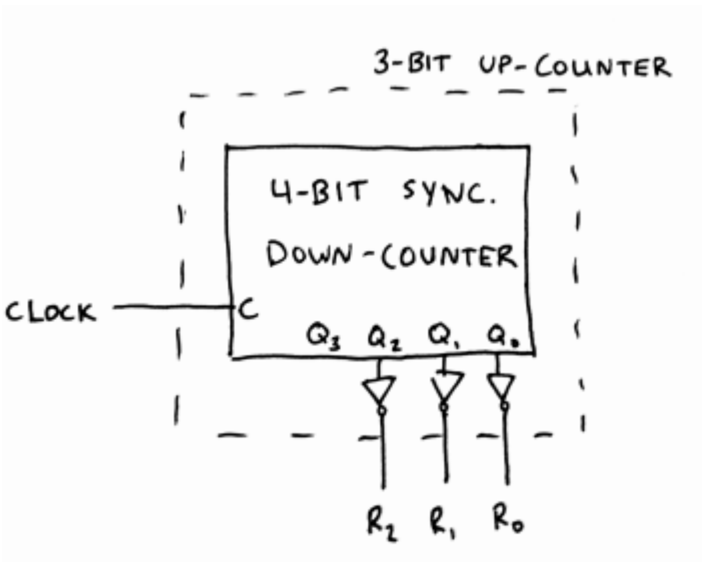
ELECTRICAL AND COMPUTER ENGINEERING

IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Thirteenth Week

Due Date: First class of 14th week

P1.



P2. a) The state diagram is

Present state	Next state $w=0$	Next state $w=1$	Output $z_2z_1z_0$
A	A	B	0 0 0
B	B	C	0 0 1
C	C	D	0 1 0
D	D	E	0 1 1
E	E	F	1 0 0
F	F	A	1 0 1

The state-assigned table is

Present state $y_2y_1y_0$	Next state $Y_2Y_1Y_0$, $w=0$	Next state $Y_2Y_1Y_0$, $w=1$	Output $z_2z_1z_0$
0 0 0	0 0 0	0 0 1	0 0 0
0 0 1	0 0 1	0 1 0	0 0 1
0 1 0	0 1 0	0 1 1	0 1 0
0 1 1	0 1 1	1 0 0	0 1 1
1 0 0	1 0 0	1 0 1	1 0 0
1 0 1	1 0 1	0 0 0	1 0 1

The next-state expressions are

$$\begin{aligned} Y_2 &= \overline{y}_0 y_2 + \overline{w} y_2 + w y_0 y_1 \\ Y_1 &= \overline{y}_0 y_1 + \overline{w} y_1 + w y_0 \overline{y}_1 \overline{y}_2 \\ Y_0 &= \overline{w} y_0 + w \overline{y}_0 \end{aligned}$$

The outputs are: z2 = y2, z1 = y1, and z0 = y0.

b) Using the state-assigned table given in the solution for P1, the excitation table for JK flip-flops is

Present state	Flip-flop inputs						Outputs
	$w = 0$			$w = 1$			
$y_2 y_1 y_0$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$	$J_2 K_2$	$J_1 K_1$	$J_0 K_0$	$z_2 z_1 z_0$
000	0 d	0 d	0 d	0 d	0 d	1 d	000
001	0 d	0 d	d 0	0 d	1 d	d 1	001
010	0 d	d 0	0 d	0 d	d 0	1 d	010
011	0 d	d 0	d 0	1 d	d 1	d 1	011
100	d 0	0 d	0 d	d 0	0 d	1 d	100
101	d 0	0 d	d 0	d 1	0 d	d 1	101

The expressions for the inputs of the flip-flops are

$$\begin{aligned} J_2 &= w y_1 y_0 \\ K_2 &= w y_2 y_0 \\ J_1 &= w \overline{y}_2 y_0 \\ K_1 &= w y_0 \\ J_0 &= w \\ K_0 &= w \end{aligned}$$

The outputs are: z2 = y2, z1 = y1, and z0 = y0.

c) Using the state-assigned table given in the solution for P1, the excitation table for T flip-flops is

Present state	Flip-flop inputs		Outputs
	$w=0$	$w=1$	
$y_2y_1y_0$	$T_2T_1T_0$	$T_2T_1T_0$	$z_2z_1z_0$
000	000	001	000
001	000	011	001
010	000	001	010
011	000	111	011
100	000	001	100
101	000	101	101

The expressions for T inputs of the flip-flops are

$$\begin{aligned} T_2 &= wy_1y_0 + wy_2y_0 \\ T_1 &= w\overline{y}_2y_0 \\ T_0 &= w \end{aligned}$$

The outputs are: z2 = y2, z1 = y1, and z0 = y0.

P3. Using straight forward state assignment:

	Present state	Next state				Output
		DN=00	01	10	11	
	$y_4y_3y_2y_1$	$Y_4Y_3Y_2Y_1$				z
S1	0 0 0 0	0 0 0 0	0 0 1 0	0 0 0 1	–	0
S2	0 0 0 1	0 0 0 1	0 0 1 1	0 1 0 0	–	0
S3	0 0 1 0	0 0 1 0	0 1 0 1	0 1 1 0	–	0
S4	0 0 1 1	0 0 0 0	–	–	–	1
S5	0 1 0 0	0 0 1 0	–	–	–	1
S6	0 1 0 1	0 1 0 1	0 1 1 1	1 0 0 0	–	0
S7	0 1 1 0	0 0 0 0	–	–	–	1
S8	0 1 1 1	0 0 0 0	–	–	–	1
S9	1 0 0 0	0 0 1 0	–	–	–	1

The next state and output expressions are:

$$\begin{aligned} Y_4 &= Dy_3 \\ Y_3 &= Dy_1 + Dy_2 + Ny_2 + \overline{D}y_3\overline{y}_2y_1 \\ Y_2 &= N\overline{y}_2 + y_3\overline{y}_1 + \overline{N}\overline{y}_3y_2\overline{y}_1 \\ Y_1 &= Ny_2 + D\overline{y}_2\overline{y}_1 + \overline{D}\overline{y}_2y_1 \\ z &= y_4 + y_1y_2 + \overline{y}_1y_3 \end{aligned}$$

Using the same approach for the second table:

	Present state $y_3y_2y_1$	Next state				Output z
		DN=00	01	10	11	
		$Y_3Y_2Y_1$				
S1	000	000	010	001	–	0
S2	001	001	011	100	–	0
S3	010	010	001	011	–	0
S4	011	000	–	–	–	1
S5	100	010	–	–	–	1

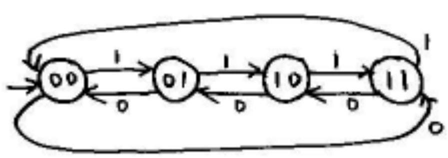
The next state and output expressions are:

$$
\begin{aligned}
Y_3 &= D\overline{y}_2y_1 \\
Y_2 &= y_3 + \overline{N}y_2\overline{y}_1 + N\overline{y}_2 \\
Y_1 &= \overline{D}\overline{y}_2y_1 + Ny_2\overline{y}_1 + D\overline{y}_3\overline{y}_1 \\
z &= y_3 + y_2y_1
\end{aligned}
$$

These expressions define a circuit that has considerably lower cost than the expressions resulting from the first table.

P4.

(a)

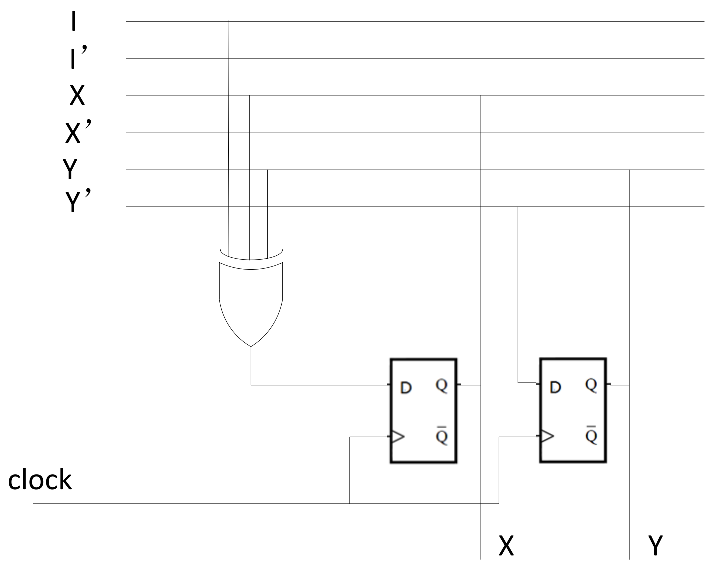


(b)

Canonical SOP:
Next X = X'Y'I' + X'YI + XY'I + XYI'
Next Y = X'Y'I' + X'Y'I + XY'I' + XY'I'

Simplified SOP:
= X'Y'I' + X'YI + XY'I + XYI'
= Y'

(c)



d) a. State 01

b. State 10

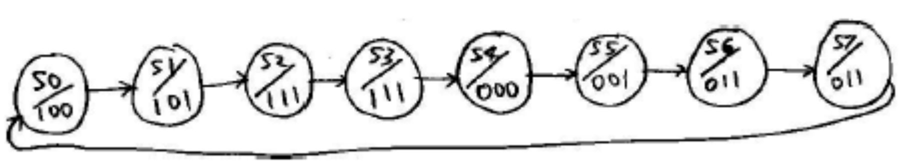
c. State 11

P5.

(a)

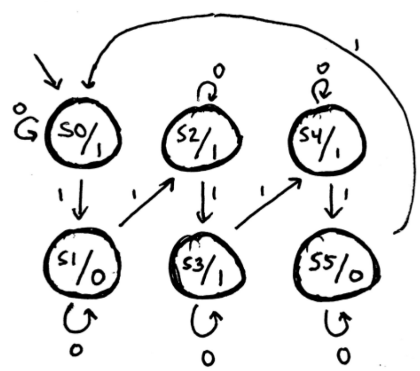
Current State				Next State			Output		
X	Y	Z	(Symbol)	X	Y	Z	A	B	C
0	0	0	(S0)	0	0	1	1	0	0
0	0	1	(S1)	0	1	0	1	0	1
0	1	0	(S2)	0	1	1	1	1	1
0	1	1	(S3)	1	0	0	1	1	1
1	0	0	(S4)	1	0	1	0	0	0
1	0	1	(S5)	1	1	0	0	0	1
1	1	0	(S6)	1	1	1	0	1	1
1	1	1	(S7)	0	0	0	0	1	1

(b)



(c) The circuit repeatedly outputs the sequence 100, 101, 111, 111, 000, 001, 011, 011.

P6. A Moore machine with six states is shown below.



P7. A minimum state table is shown below. We assume that the 3-bit patterns do not overlap.

Present state	Next state $w = 0$	Next state $w = 1$	Output p
A	B	C	0
B	D	E	0
C	E	D	0
D	A	F	0
E	F	A	0
F	B	C	1

P8.