KEY

Name CHRIS CHU

ISU Net ID _____@iastate.edu

Lab Section (circle one): **A** (T 6-9), **B** (W 3-6), **C** (R 4-7), **D** (F 12-3), **E** (F 3-6), **F** (T 12-3), **G** (W 6-9), **J** (W 12-3), **K** (T 3-6)

CprE 281
Digital Logic

Examination #2

4/13/2015 4:10-5:00PM

Directions: There are 8 questions in this exam. Each question is worth points indicated along with the problem. You should roughly spend 1 minute for every two point. So plan accordingly. If a problem appears to be hard, move on. Please read the questions carefully. Do not write more than what is required.

Calculator should NOT be used.

Problem	Score	
1	_____ / 3 points	BYRON
2	_____ / 13 points	BYRON
3	_____ / 6 points	BYRON
4	_____ / 18 points	PRATIK
5	_____ / 16 points	PRATIK
6	_____ / 10 points	CHRIS
7	_____ / 16 points	CHRIS
8	_____ / 18 points	CHRIS
Total	_____ (out of 100 points)	BYRON (CALC. TOTAL & ENTER TO Bb.)

KEY

1. (Total 3 points) Write your Name, ISU Net ID and Lab Section in the cover page.

2. (Total 13 points) For this question, assume that numbers in binary are represented as a **5-bit** word in **2's complement** form.

   (a) (2 points) What is the range of integer that can be represented by a 5-bit 2's complement number? -16 to 15

   (b) (2 points) Give the binary representations for the following decimal numbers:

   a. 12 = 01100

   b. -12 = 10100

   (c) (3 points) Give the decimal values for the following binary numbers in 2's complement representation:

   a. 01110 = 14

   b. 10010 = -14

   (d) (2 points) Negate the following numbers:

   a. 01101 10011

   b. 11000 01000

   (e) (4 points) Perform the following additions directly. Write the carry bits at the top and indicate whether or not an overflow occurs in each case.

```
  11111          01100
   10011          01101
+  11101       +  00110
   10000          10011
```

NO OVERFLOW OVERFLOW

3. (Total 6 points) Convert the following IEEE single-precision floating point number into decimal:

1 10000001 11100000000000000000000

-ve

129-127 = 2

$-1 \times 1.111 \times 2^2$

$= -111.1$

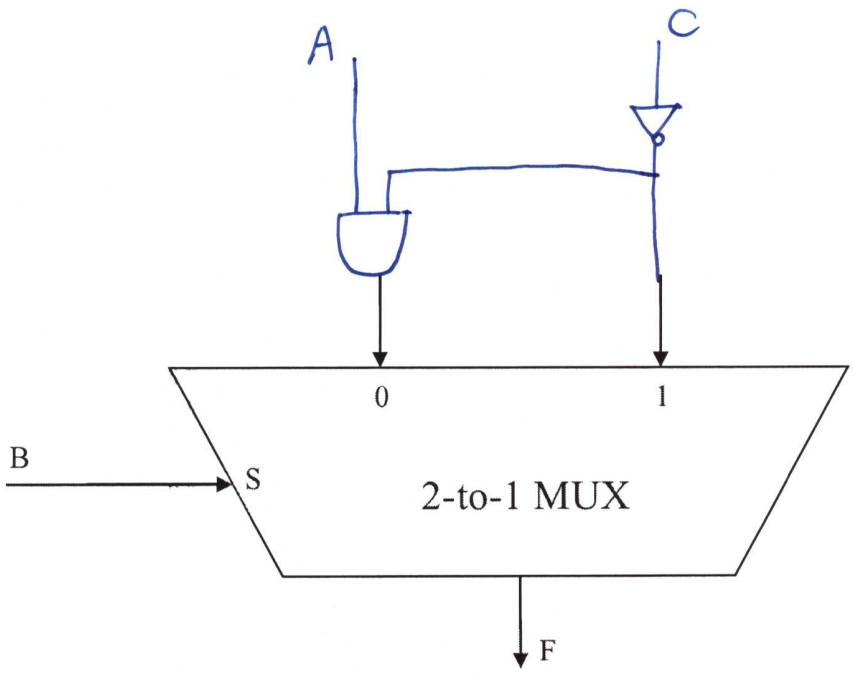
$= -7.5$

4. (Total 18 points) Consider the function F = A' B C' + A B' C' + A B C'.

(a) (5 points) Based on Shannon's expansion, implement F **exactly one 2-to-1 MUX** and a minimal amount of basic logic gates. Please make your design as simple as possible. Please use B as the selection signal of the MUX. Please show your steps and label your circuit diagram clearly.

$F(A, 0, C) = AC'$

$F(A, 1, C) = A'C' + AC' = C'$



(b) (4 points) Construct the truth table for function F.

(for part (c))

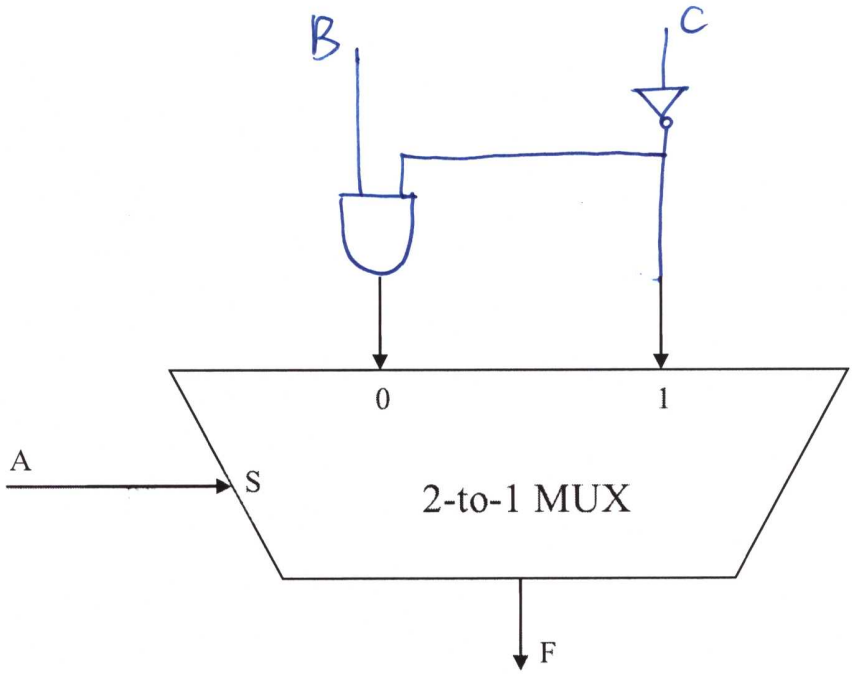
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

BC'

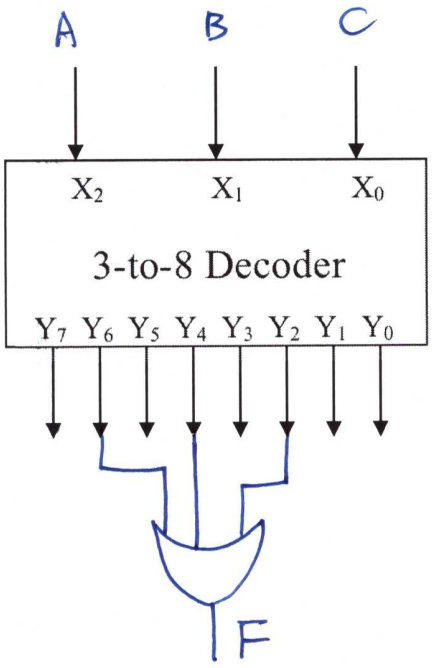
C'

(Question 4 continued.)

(c) (4 points) Based on the truth table in part (b), implement F using **exactly one 2-to-1 multiplexer** and a minimal amount of basic logic gates. Please make your design as simple as possible. Please use A as the selection signal of the MUX. Please label your circuit clearly.



(d) (5 points) Implement F using **exactly one 3-to-8 decoder** and a minimal amount of basic logic gates. Please make your design as simple as possible. Please label your circuit clearly. You **must** make use of the decoder appropriately in order to get any credit.

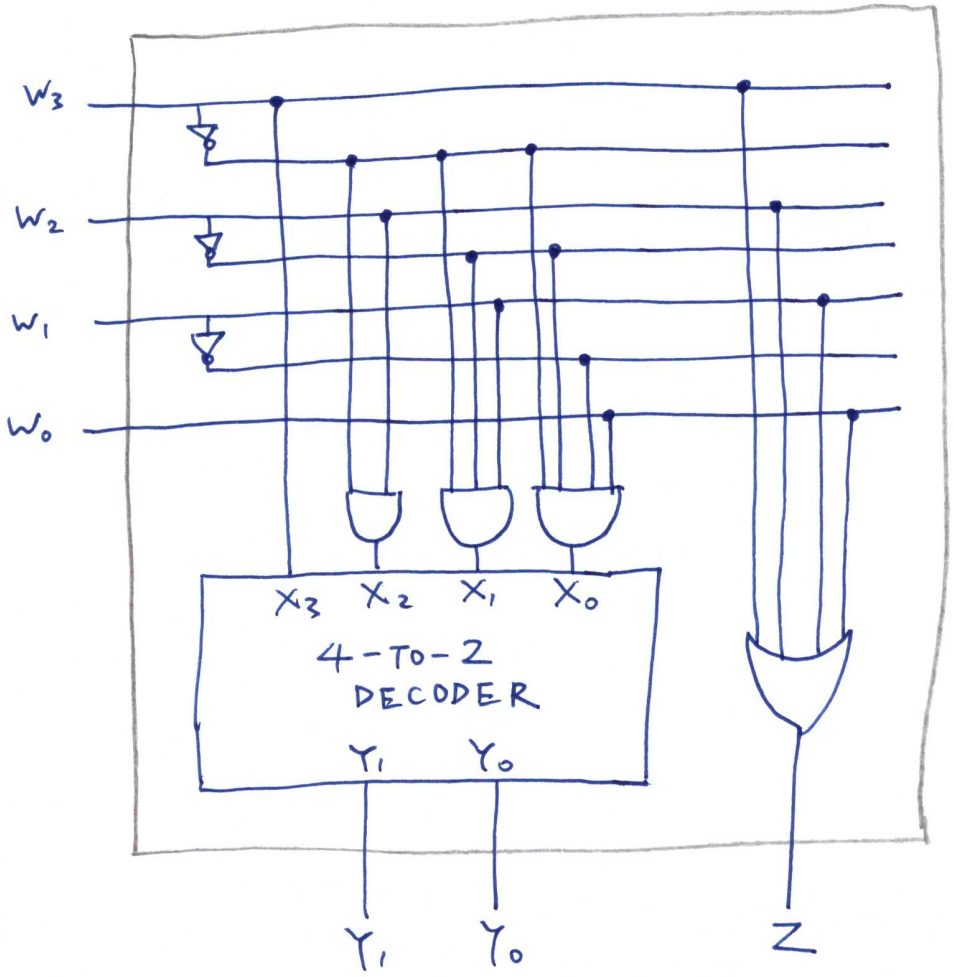


5. (Total 16 points) In this question, consider a 4-to-2 priority encoder with inputs w3, w2, w1, w0 and outputs y1, y0, z. w3 has the highest priority and w0 has the lowest. The outputs y1 y0 together indicate the active input with the highest priority. The output z indicates that some of the inputs is equal to 1.

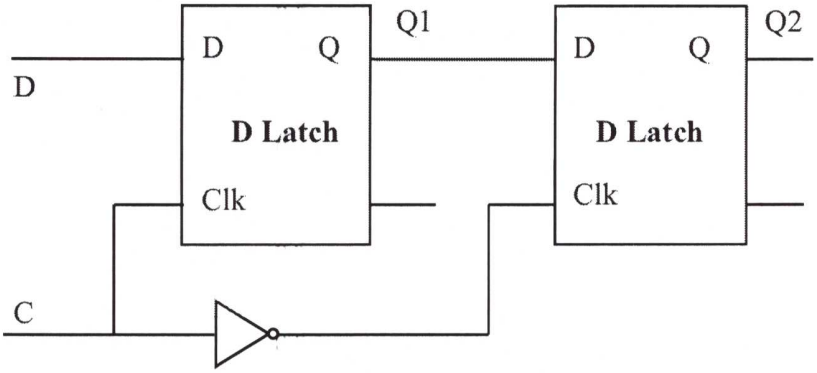
   (a) (6 points) Please complete the truth table for the priority encoder below. 'X' in the table represents both 0 and 1.

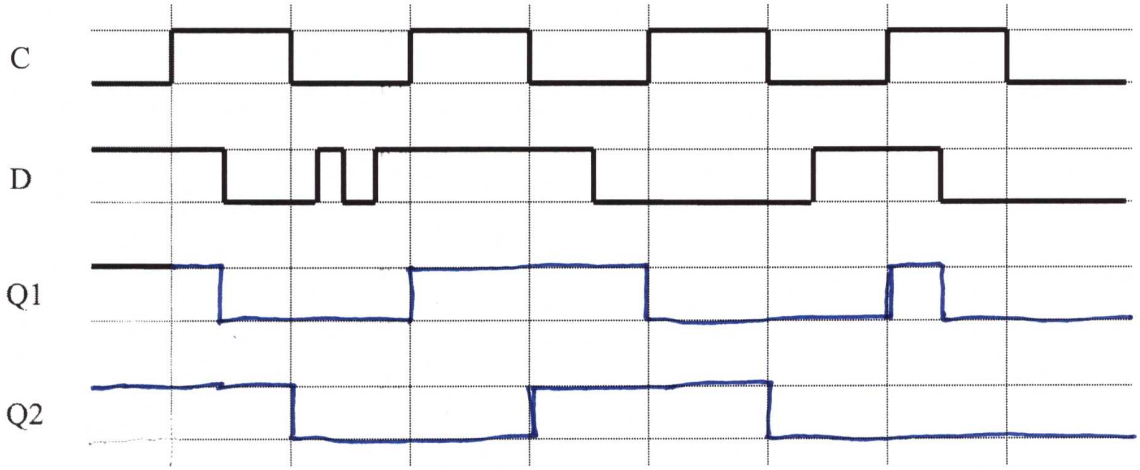
w3	w2	w1	w0	y1	y0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

   (b) (10 points) Design the priority encoder using **exactly one 4-to-2 encoder**, three AND gates, one OR gates, and three NOT gates. **Hint:** You may want to use the gates to convert the inputs to the priority encoder into some appropriate inputs to the encoder to generate y1 y0.



6. (Total 10 points) Assume all gates (including the gates inside the D latches) in the circuit below have **no delay**. Complete the waveform for Q1 and Q2 in the diagram below.





7. (Total 16 points)

(a) (4 points) Complete the truth table below which describes the behavior of T flip-flop.

T	Current Q	Next Q
0	0	0
0	1	1
1	0	1
1	1	0

D (for part (d))
0
1
1
0

$D = T \oplus Q$

(b) (4 points) Complete the truth table below which describes the behavior of D flip-flop.

D	Current Q	Next Q
0	0	0
0	1	0
1	0	1
1	1	1

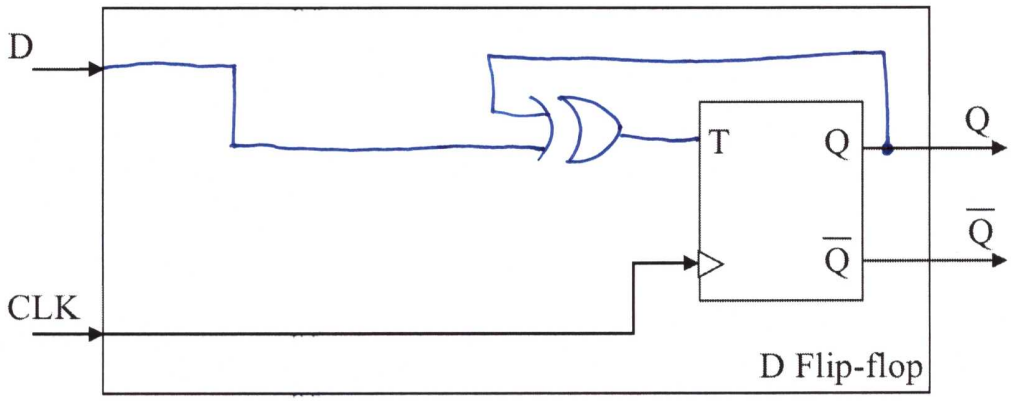
T (for part (c))
0
1
1
0

$T = D \oplus Q$

(Question 7 continued.)

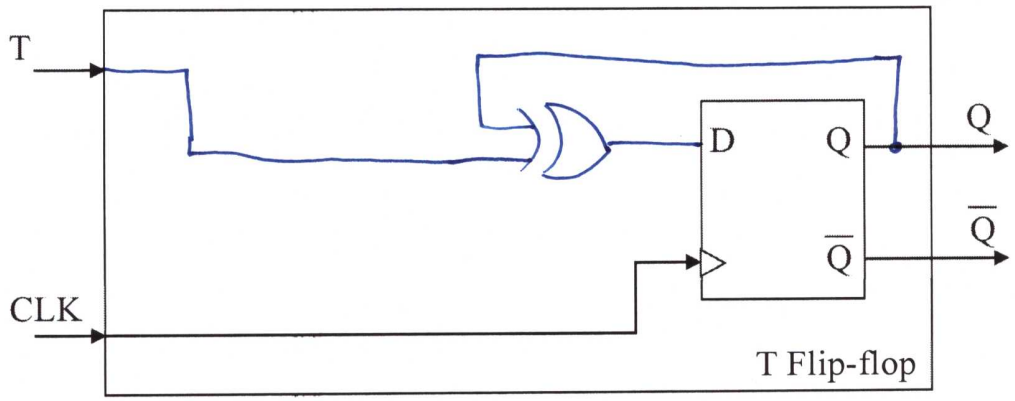
(c) (4 points) Construct a D flip-flop using one T flip-flop and some other gates. Please show how you come up with the design using the truth tables above.

see part (b).



(d) (4 points) Construct a T flip-flop using one D flip-flop and some other gates. Please show how you come up with the design using the truth tables above.

see part (a).



8. (Total 18 points) This question considers the design of a 3-bit synchronous up-counter with Enable using D flip-flops. Let the output of the counter be $Q_2\ Q_1\ Q_0$. (Q_2 is the MSB and Q_0 is the LSB.) Let the data inputs to the three D flip-flops be D_2, D_1 and D_0, respectively.

(a) (1 points) If Enable=0, how will Q_0 be changed after a clock edge?

Q_0 (i.e., remain the same)

(b) (1 points) If Enable=1, how will Q_0 be changed after a clock edge?

$\overline{Q_0}$ (i.e., toggled)

(c) (2 points) Based on parts (a) and (b), please give a logic expression for D_0.

$D_0 = Q_0 \oplus \text{Enable}$

(d) (2 points) Under what condition will Q_1 remain the same after a clock edge?

When $Q_0 = 0$ or Enable $= 0$

(e) (2 points) Under what condition will Q_1 toggle after a clock edge?

When $Q_0 = 1$ and Enable $= 1$

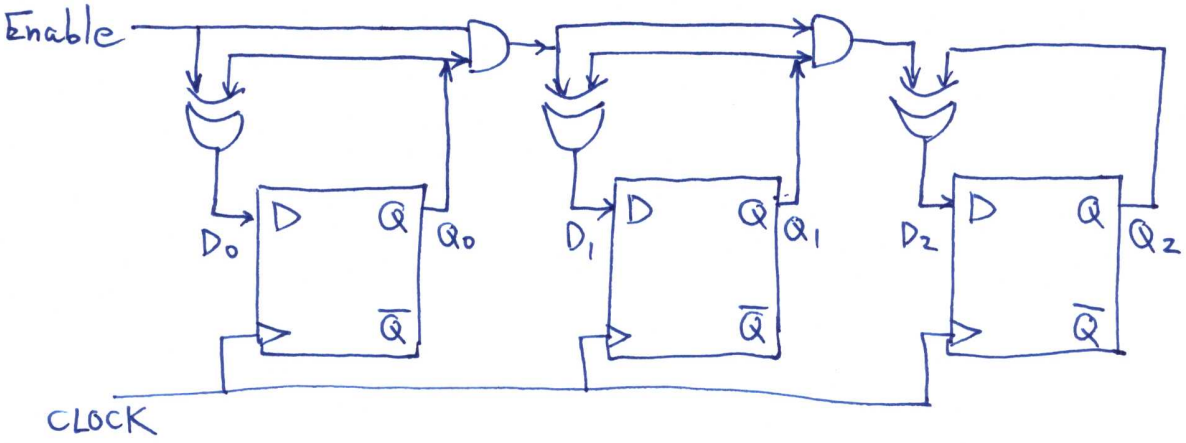
(f) (2 points) Based on parts (d) and (e), please give a logic expression for D_1.

$D_1 = Q_1 \oplus (Q_0 \cdot \text{Enable})$

(g) (3 points) Write a logic expression for D_2.

$D_2 = Q_2 \oplus (Q_1 \cdot Q_0 \cdot \text{Enable})$

(h) (5 points) Draw a circuit diagram for a 3-bit synchronous up-counter with Enable using some D flip-flops, 2-input AND gates, 2-input OR gates, 2-input XOR gates and NOT gates. *(Note that you do not need to use all components listed here.)* Please make your design as simple as possible. Please label your circuit clearly.



(END OF EXAM)