Name _____

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Lab Section (circle one): **A** (T 6-9), **B** (W 3-6), **C** (R 4-7), **D** (F 12-3), **E** (F 3-6), **F** (T 12-3), **G** (W 6-9), **J** (W 12-3), **K** (T 3-6)

CprE 281

Digital Logic

Mock Examination #1

Time limit: 50 minutes

Directions: There are 7 questions in this exam. Each question is worth points indicated along with the problem. You should roughly spend 1 minute for every two point. So plan accordingly. If a problem appears to be hard, move on. Please read the questions carefully. Do not write more than what is required.

Problem	**Score**
1	_____ **/ 14 points**
2	_____ **/ 16 points**
3	_____ **/ 17 points**
4	_____ **/ 10 points**
5	_____ **/ 12 points**
6	_____ **/ 14 points**
7	_____ **/ 17 points**

Total _____ (out of 100 points)

1. (Total 14 points) Consider the logic expression F = XY'+YZ'+ZX'.
   (a) (4 points) Write the truth table.

X Y Z	F
0 0 0	
0 0 1	
0 1 0	
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	

   (b) (2 points) Draw the circuit diagram using the logic gate symbols.

   (c) (2 points) Write the canonical sum-of-products expression. Do not use shorthand notation.

   (d) (2 points) Write the canonical sum-of-products expression in shorthand notation.

   (e) (2 points) Write the canonical product-of-sums expression. Do not use shorthand notation.

   (f) (2 points) Write the canonical product-of-sums expression in shorthand notation.

2. (Total 16 points) A 2-variable comparator circuit receives four input signals P1, P0, Q1, Q0 and produces an output signal F. The output F is 1 if either (i) P1>Q1 or (ii) P1=Q1 and P0 > Q0.

(a) (4 points) Write the truth table for the output function F.

P1	P0	Q1	Q0	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

(b) (5 points) Write the simplest logic expression for F by the Karnaugh map using SOP form.

(c) (5 points) Write the simplest logic expression for F by the Karnaugh map using POS form.

(d) (2 points) Let the cost of an expression be the total number of gates plus the total number of inputs of the circuit implementing the expression. Assume that AND gates and OR gates of any number of inputs can be used in the implementation. NOT gates to complement the input variables are also counted. What is the cost of the expressions in parts (b) and (c)?

3. (Total 17 points) Use K-map to get the **simplest SOP** expression for the functions below.
   (a) (4 points)

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	1	1	0	1
10	1	0	0	1

   (b) (4 points) ("d" means "Don't care conditions".)

CD \ AB	00	01	11	10
00	1	0	d	1
01	d	0	0	d
11	1	1	d	1
10	1	0	d	1

   (c) (9 points) F(A,B,C,D) = B'.C'.D' + A.C' + A'.B.C'.D + A.B'.C.D. + A.B.C.D'

4. (Total 10 points) Draw a CMOS circuit to implement the function f = ((a+b).(c+de))' using 5 NMOS and 5 PMOS transistors.

5. (Total 12 points) The rules of Boolean algebra are listed below:

1a: 0.0 = 0	10a: x.y = y.x
1b: 1+1 = 1	10b: x+y = y+x
2a: 1.1 = 1	11a: x.(y.z) = (x.y).z
2b: 0+0 = 0	11b: x+(y+z) = (x+y)+z
3a: 0.1 = 1.0 = 0	12a: x.(y+z) = x.y + x.z
3b: 1+0 = 0+1 = 1	12b: x+y.z = (x+y).(x+z)
4a: If x=0, then x' = 1	13a: x+x.y = x
4b: If x=1, then x' = 0	13b: x.(x+y) = x
5a: x.0 = 0	14a: x.y+x.y' = x
5b: x+1 = 1	14b: (x+y).(x+y') = x
6a: x.1 = x	15a: (x.y)' = x'+y'
6b: x+0 = x	15b: (x+y)' = x'.y'
7a: x.x = x	16a: x+x'.y = x+y
7b: x+x = x	16b: x.(x'+y) = x.y
8a: x.x' = 0	
8b: x+x' = 1	
9: (x')' = x	

Prove the equality (a + b).(a'b' + a + b') = a

(a) (2 points) by truth table.

(b) (5 points) by Boolean algebra. Please show **all steps** and write down the rule number for each step.

(c) (5 points) by verifying its dual theorem using Boolean algebra. Please show **all steps** and write down the rule number for each step.

6. (Total 14 points) Consider the logic function F(A,B) = A.B + A'.B'. **Assume A' and B' are given as inputs.**
   (a) (4 points) Draw a circuit diagram to show an implementation of F using 2-input NAND gates only. Use as few NAND gates as possible.

   (b) (1 points) If each 2-input NAND gate is implemented as a CMOS gate, how many transistors are there for the circuit in part (a)?

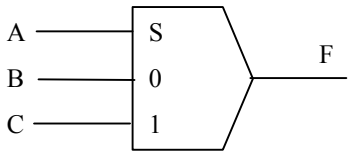
   (c) (6 points) Draw a circuit diagram to show an implementation of F using 2-input NOR gates only. Use as few NOR gates as possible.

   (d) (1 points) If each 2-input NOR gate is implemented as a CMOS gate, how many transistors are there for the circuit in part (c)?

   (e) (2 points) If F is implemented directly as a CMOS complex gate, how many transistors are required? You do not need to show the circuit.

7. (Total 17 points) A company MacroHard introduces a new type of gate called BILL (**B**rilliant **I**ndustrial **L**ow-power **L**ogic) gate with three inputs A, B and C and one output F. Its functionality is specified by the following truth table. Its circuit symbol is also shown below. Since the inputs of the BILL gate is not symmetric, please label the inputs of the gate by "S", "0" and "1" as in the circuit symbol shown.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



They claim that the BILL gate can be used to replace all other types of gates. We will verify their claim in this question. (Hint: You may find it useful to derive a simplified SOP expression for F from the truth table. The simplified SOP is **not** required but it may be a good way to try if you do not have any idea how to do this question.)

(a) (4 points) Draw a circuit to show how to implement a NOT gate using one BILL gate.

(b) (5 points) Draw a circuit to show how to implement an AND gate using one BILL gate.

(Question 7 cont'd)

(c) (6 points) Draw a circuit to show how to implement an OR gate using one BILL gate.

(d) (2 points) In fact, the BILL gate is a very commonly used circuit that you have seen several times in the class. What is the name of this circuit?

(END OF EXAM)

Extra Exercises

1. Perform the following conversions:
   (a) $(110011)_2$ to decimal
   (b) $(81)_{10}$ to binary
   (c) $(0111101110)_2$ to hexadecimal
   (d) $(1A3)_{16}$ to binary
   (e) $(FEE)_{16}$ to octal
   (f) $(321)_5$ to base 6 representation

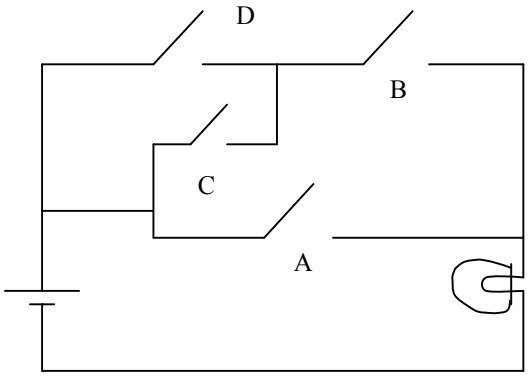
2. For the logic expressions (X+Y)(X'+Y),
   (a) Give the truth table
   (b) Draw the circuit using the logic gate symbols
   (c) Derive the canonical sum-of-products expression.
   (d) Derive the canonical product-of-sums expression.

3. For the function in Mock Examination #1 Question 2:
   (a) Write the canonical SOP expression for F. Do not use shorthand notation.
   (b) Write the canonical SOP expression for F in shorthand notation.
   (c) Write the canonical POS expression for F. Do not use shorthand notation.
   (d) Write the canonical POS expression for F in shorthand notation.

4. The designers in the car manufacturing company Atoyot want to design a safety system such that an warning light will turn on if the condition below is satisfied:
   - Either the doors are closed and seat belts are unbuckled
   - Or seat belts are buckled and parking brake is on
   - Or parking brake is off and doors are not closed.

   Use a truth table to write a sum-of-products expression which indicates when to turn the warning light on. Is the condition used by the safety system a reasonable one? (In other words, will the light turn on for some safe situation, or turn off for some unsafe situation?)

5. The circuit as shown consists of four 2-position switches, lamp and a power source. Give the truth table listing all possible combinations of switch positions. Assign a "1" for the condition of a switch being closed and for the condition of lamp being lit. Minimize the logic expression using Karnaugh map.



6. Prove or disprove the following:
   (a) a + a' = 1
   (b) ab + a'b' = 1

(c) ab'c + a'bc' = 1
(d) (ab + a'b')' = (a'b + ab')

7. Use Boolean algebra to simplify the following functions. Please show all the steps and state explicitly all axioms/theorems/properties (i.e., 1a, 1b, …., 16b) that you used.
   (a) (a + b).a'.b'
   (b) a'.(a + a'b)
   (c) (a + a'bc).(a + c)'

8. Use K-map to simplify the function in Question 6(c).

9. This question compares different ways to implement the function
   f(a, b, c, d) = Σ m(1, 2, 3, 13, 14, 15)
   Let the cost of a circuit be defined as the number of transistors to implement the circuit. All gates used are implemented as CMOS gates. Gates of any number of inputs are allowed.
   (a) Simplify f by K-map using SOP form. Draw the circuit for the simplified SOP expression. What is the cost of the circuit?
   (b) Simplify f by K-map using POS form. Draw the circuit for the simplified POS expression. What is the cost of the circuit?
   (c) By factoring the simplified SOP expression in (a), we can show that f = (a'b' + ab).(d + c). Draw the corresponding circuit. Notice that it is a 4-level circuit (including NOT gates). What is the cost of the circuit?
   (d) Suppose we use the DeMorgan's law to transform the circuit in (a) to use NAND, NOR and NOT gates. Draw the resulting circuit. What is the cost of this circuit?
   (e) Suppose we use the DeMorgan's law to transform the circuit in (b) to use NAND, NOR and NOT gates. Draw the resulting circuit. What is the cost of this circuit?
   (f) Suppose we use the DeMorgan's law to transform the circuit in (c) to use NAND, NOR and NOT gates. Draw the resulting circuit. What is the cost of this circuit?

10. Implement the following two functions at the same time into a PLA similar to the one in Figure B.26 / B.27 but has 4 input variables a,b,c,d:
    f1(a, b, c, d) = Σ m(1, 3, 5, 7, 10, 11, 14, 15)
    f2(a, b, c, d) = Σ m(1, 4, 5, 6, 7, 10, 12, 13, 14, 15)

11. Simplify the following function by K-map:
    f(d, c, b, a) = Π M(0, 1, 2, 5, 9, 10) + D(3, 8, 11, 13, 14)
    (Note that the expression is in POS shorthand notation.)
    (a) in SOP form.
    (b) in POS form.

12. Given the function f = (ab + a'b' + c).(de + d'f).g
    (a) What is the minimum number of 2-input LUTs required to implement f?
    (b) What is the minimum number of 3-input LUTs required to implement f?