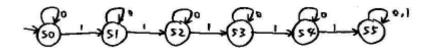
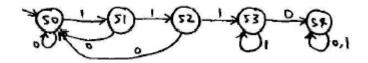
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ELECTRICAL AND COMPUTER ENGINEERING IOWA STATE UNIVERSITY Synchronous Sequential Circuits Assigned Date: Fourteenth Week Due Date: First class of 15th week

P1. (a)

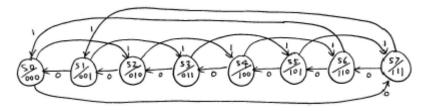


(b)



P2.

State transition diagram:



State table with a straightforward state assignment (000 for S0, 001 for S1, etc.):

Present			Next state								
	state			w=0			w=1		(Outpu	t
y2	y1	y0	Y2	Y1	Y0	Y2	Y1	Y0	z 2	z1	z 0
0	0	0	1	1	1	0	1	0	0	0	0
0	0	1	0	0	0	0	1	1	0	0	1
0	1	0	0	0	1	1	0	0	0	1	0
0	1	1	0	1	0	1	0	1	0	1	1
1	0	0	0	1	1	1	1	0	1	0	0
1	0	1	1	0	0	1	1	1	1	0	1
1	1	0	1	0	1	0	0	0	1	1	0
1	1	1	1	1	0	0	0	1	1	1	1

The next-state expressions (inputs to D flip-flops) and output expressions are:

$$D_2 = Y_2 = w \, \overline{y}_2 \, y_1 + \, \overline{w} \, y_2 \, y_1 + \, w \, y_2 \, \overline{y}_1 + \, \overline{w} \, y_2 \, y_0 + \, \overline{y}_2 \, \overline{y}_1 \, \overline{y}_0 \, w$$

$$\mathbf{D}_1 = \mathbf{Y}_1 = \mathbf{w} \ \overline{\mathbf{y}}_1 + \overline{\mathbf{y}}_1 \ \overline{\mathbf{y}}_0 + \overline{\mathbf{w}} \ \mathbf{y}_1 \ \mathbf{y}_0$$

$$\mathbf{D}_0 = \mathbf{Y}_0 = \overline{\mathbf{y}}_0 \, \overline{\mathbf{w}} + \mathbf{y}_0 \, \mathbf{w}$$

$$\mathbf{z}_2 = \mathbf{y}_2$$

$$\mathbf{z}_1 = \mathbf{y}_1$$

$$z_0 = y_0$$

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P3. The state table is:

Present	Next	Count	
state	w = 0	w = 1	
A	Н	С	0
В	A	D	1
C	В	E	2
D	C	F	3
Е	D	G	4
F	Е	Н	5
G	F	A	6
Н	G	В	7

The state-assigned table is:

	Present	Next	Output	
	state	w = 0	w = 1	$z_2 z_1 z_0$
	Y 2 Y 1 Y 0	$Y_2Y_1Y_0$	$Y_2 Y_1 Y_0$	
A	0 0 0	111	0 1 0	0 0 0
В	0 0 1	0 0 0	0 1 1	0 0 1
C	0 1 0	0 0 1	100	0 1 0
D	0 1 1	0 1 0	1 0 1	0 1 1
E	100	0 1 1	1 1 0	100
_	1 0 1	100	1 1 1	1 0 1
F	110	1 0 1	$0 \ 0 \ 0$	1 1 0
G	1 1 1	110	0 0 1	111

The excitation table for T flip-flops is:

Present	Flip-flo	Outputs	
state	w = 0	w = 1	$z_2 z_1 z_0$
y ₂ y ₁ y ₀	$T_2T_1T_0$	$T_2T_1T_0$	
000	111	010	000
001	001	010	001
010	011	110	010
011	001	110	011
100	111	010	100
101	001	010	101
110	011	110	110
111	001	110	111

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The expressions for *T* inputs of the flip-flops are:

$$T_2 = \overline{y_1} \cdot \overline{y_0} \cdot \overline{w} + y_1 \cdot w$$

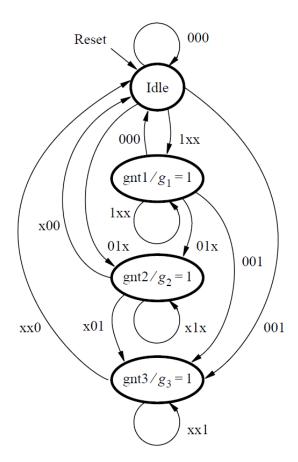
$$T_1 = w + \overline{y_0}$$

$$T_0 = \overline{w}$$

The outputs are:

$$z_2 = y_2, z_1 = y_1, z_0 = y_0.$$

P4. To ensure that Device 3 will get serviced the FSM in Figure 6.72 can be modified as follows:



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A B C

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P5. For the state table in Fig. 6.51, using a straightforward state assignment, we have:

	Present	Next	Output	
	state	w = 0	w = 1	Z
	<i>y</i> 3 <i>y</i> 2 <i>y</i> 1	$Y_3 Y_2 Y_1$	$Y_3 Y_2 Y_1$	
4	000	0 0 1	010	1
В	0 0 1	0 1 1	101	1
\mathbb{C}	0 1 0	101	100	0
)	0 1 1	0 0 1	110	1
Е	100	1 0 1	010	0
F	1 0 1	100	0 1 1	0
Ĵ	1 1 0	1 0 1	1 1 0	0

$$Y_{3} = \overline{w}y_{3} + \overline{y}_{1}y_{2} + wy_{1}\overline{y}_{3}$$

$$Y_{2} = wy_{3} + w\overline{y}_{1}\overline{y}_{2} + wy_{1}y_{2} + \overline{w}y_{1}\overline{y}_{2}\overline{y}_{3}$$

$$Y_{1} = \overline{y}_{3}\overline{w} + \overline{y}_{1}\overline{w} + wy_{1}\overline{y}_{2}$$

$$z = y_{1}\overline{y}_{3} + \overline{y}_{2}\overline{y}_{3}$$

For the state table in Fig. 6.52, using a straightforward state assignment, we have:

Present	Next	Output	
state	w = 0	w = 1	Z
<i>y</i> ₂ <i>y</i> ₁	Y_2Y_1	Y_2Y_1	
0 0	0 1	1 0	1
0 1	0 0	1 1	1
10	1 1	10	0
1 1	1 0	0 0	0

$$Y_2 = \overline{w}y_2 + \overline{y}_1y_2 + w\overline{y}_2$$

$$Y_1 = \overline{y}_1\overline{w} + wy_1\overline{y}_2$$

$$z = \overline{y}_2$$

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P6. A minimal state table is

Present	Next	Output	
state	w = 0	w = 1	z
Α	A	В	0
В	E	C	0
C	D	C	0
D	Α	F	1
E	A	F	0
F	E	C	1

b) An initial attempt at deriving a state table may be

Present	Next	state	Output z	
state	w = 0	w = 1	w = 0	w = 1
A	A	В	0	0
В	D	C	0	0
C	D	C	1	0
D	Α	E	0	1
Е	D	C	0	0

States B and E are equivalent; hence the minimal state table is

Present	Next	state	Output z	
state	w = 0	w = 1	w = 0	w = 1
A	A	В	0	0
В	D	C	0	0
C	D	C	1	0
D	Α	В	0	1