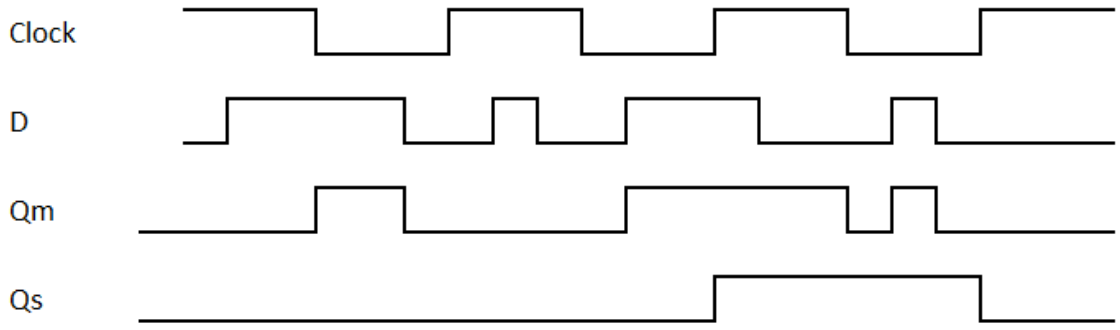
Cpr E 281 HW09 SOLUTION

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

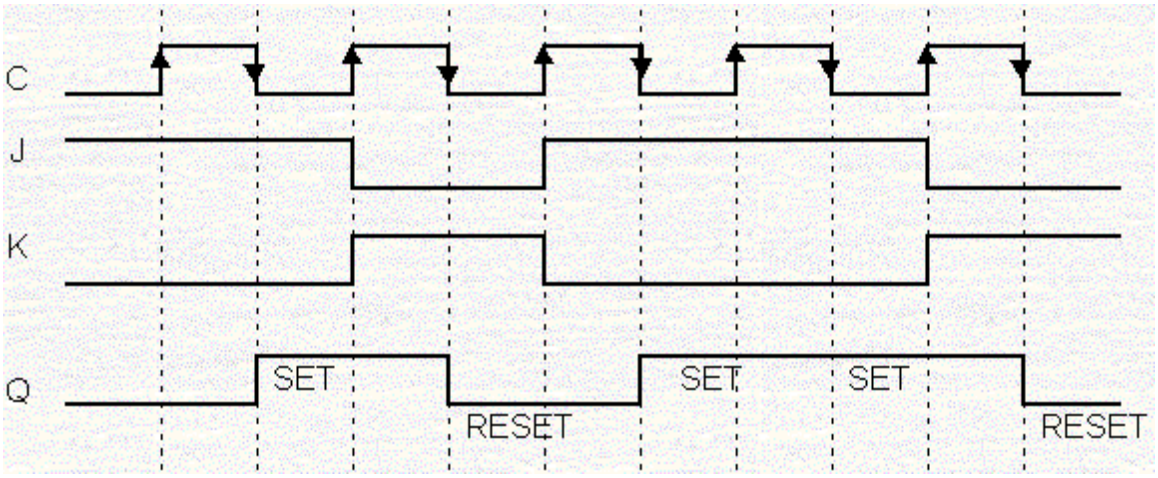
Registers and Counters
Assigned Date: Eleventh Week
Due Date: First class of 13th week

P1.



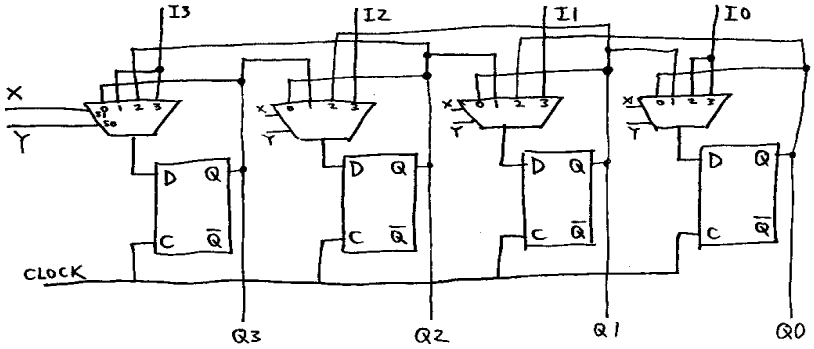
When the Clock is low, the master copies D to Q_m and Q_s is not changed. When the Clock is high, Q_m is not changed and the slave copies Q_m to Q_s. Hence the only time that Q_s (=Q) is changed is when the Clock is changing from low to high (i.e., positive clock edge). Then value stored in Q after the positive clock edge is the last value copied from D to Q_m right before the Clock is switched to high.

P2.



P3. This gated D latch design consists of 4 NAND gates and 1 NOT gate.
So total # of transistors in one gated D latch = 4x4 + 1x2 = 18.
A 64-bit register consists of 128 gated D latches and 64 NOT gates.
Total # of transistors in a 64-bit register = 128x18 + 64x2 = 2432.

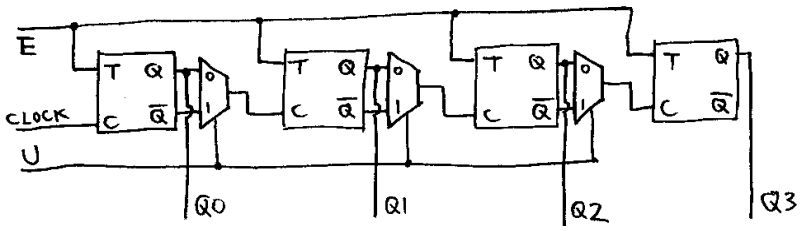
P4. We can construct the circuit using four D flip-flops and four 4-to-1 MUXs only.



P5. The counting sequence is 000, 001, 010, 111.

P6. w=8, x=3, y=8, z=16, p=2, q=3, r=8

P7.



P8.

Solution: let, S_1 select= right shift and S_0 select=left shift

s_1	s_0	y_3	y_2	y_1	y_0
0	0	w_3	w_2	w_1	w_0
0	1	0	w_3	w_2	w_1
1	0	w_2	w_1	w_0	0
1	1	X	X	X	X