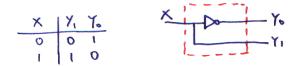
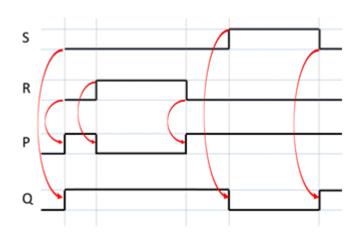
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P1.



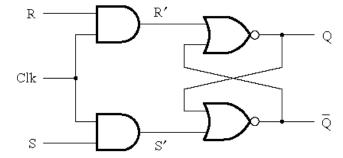
P2. a)



- b) i. This is an undesirable input combination. Both Q and P will become 1 (i.e., not complement of each other). If both R and S switched to 1 at the same time, the outputs will start to oscillate.
 - ii) Q=0 and P=1.
 - iii) Q=1 and P=0.
 - iv) Q and P will remain unchanged if P is complement of Q originally.

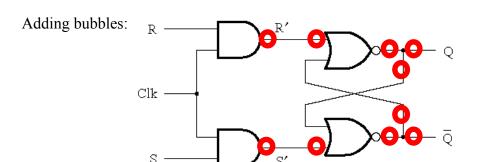
P3.

Fig. 5.5(a):



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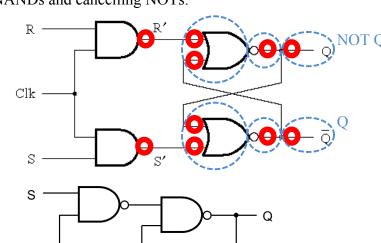
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Converting to NANDs and cancelling NOTs:

Clk

R



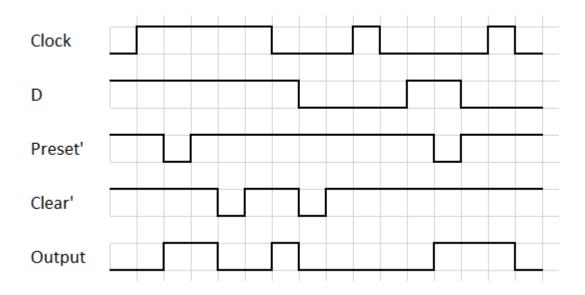
ā

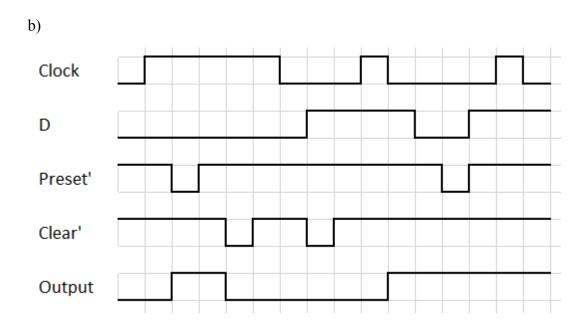
Fig. 5.6:

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P4. a) (In the diagram below, Preset' = Preset_n, Clear'=Clear_n, Output=Q.)

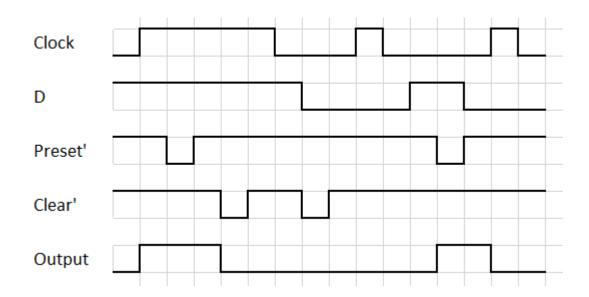




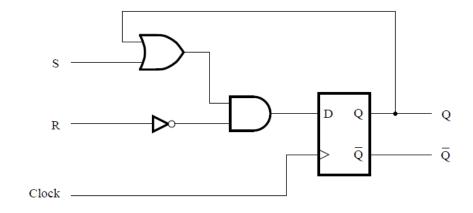
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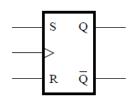
c)







S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	0



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b)

Clock

Clock

P6. Assuming both flip-flops are initialized with internal values of 0:

