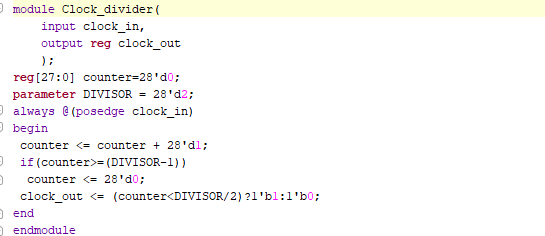
Name: - Patoriya Jayraj

ID NO.: - 21EL065

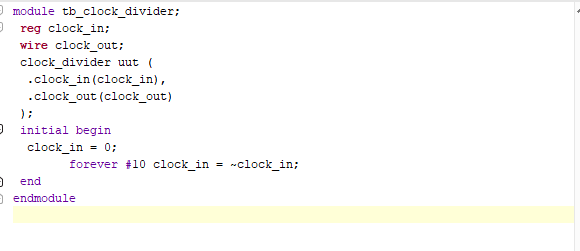
Division: - 04

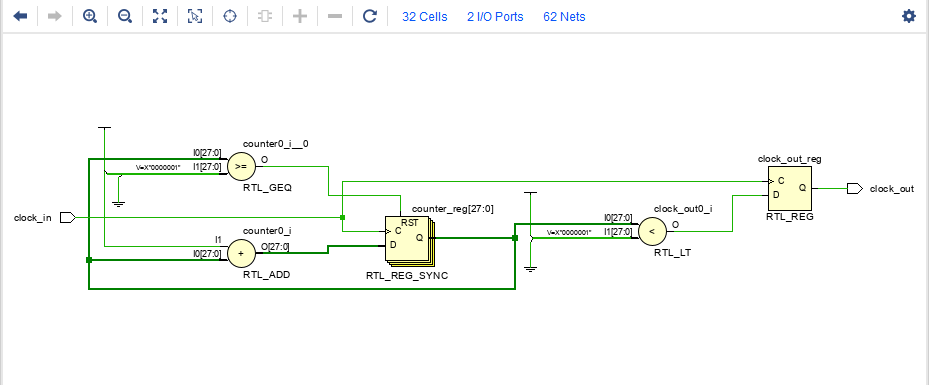
Subject: - Digital System Design (3EL42)

VERILOG CODE: -

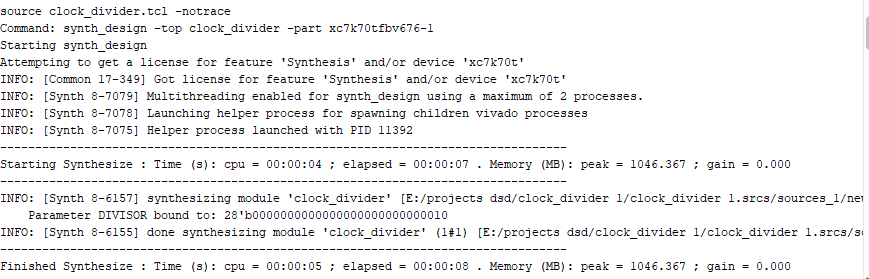


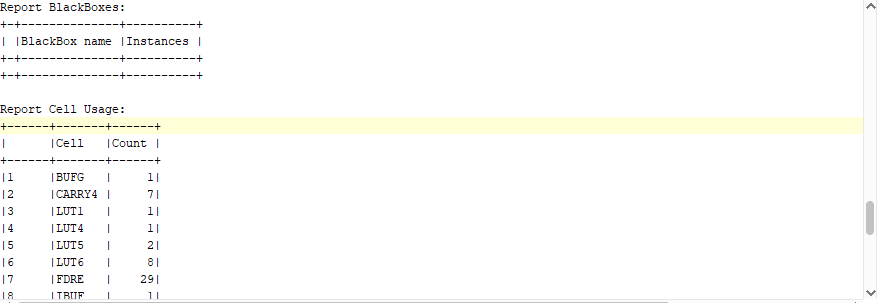
TEST BENCH: -

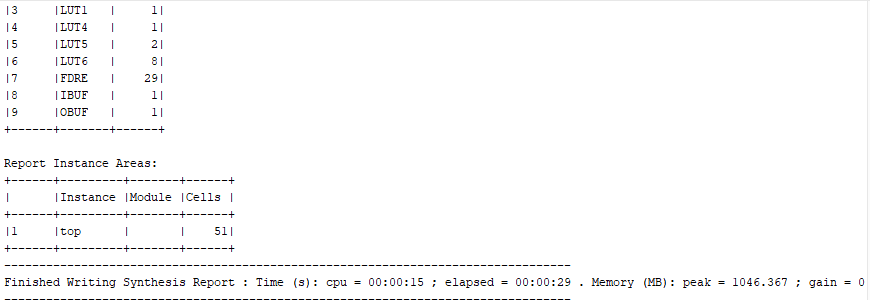




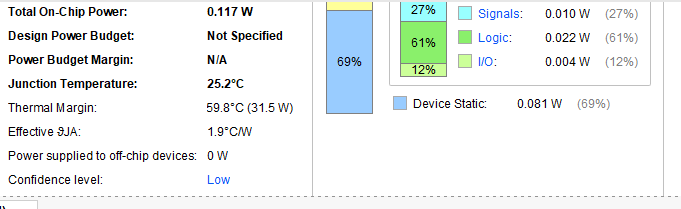
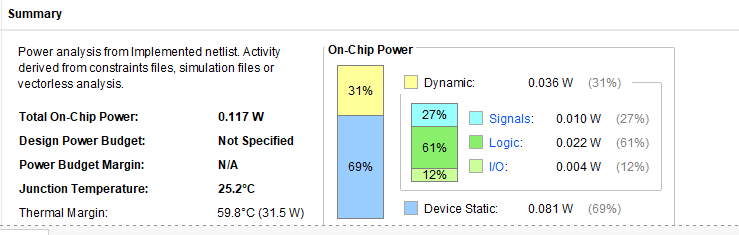
SYNTHESIS REPORT: -





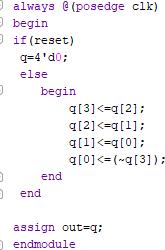
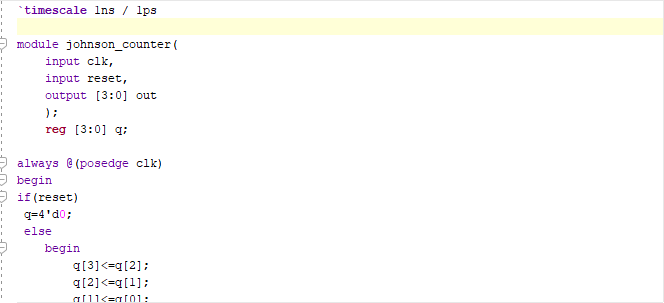


POWER REPORT: -

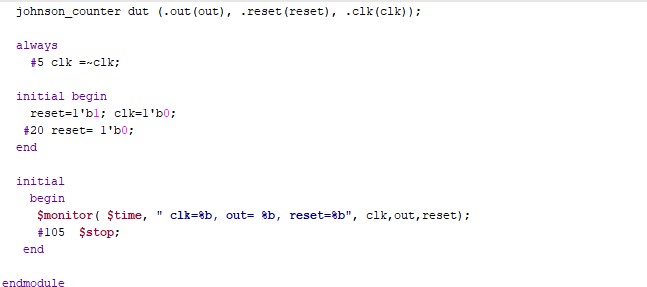
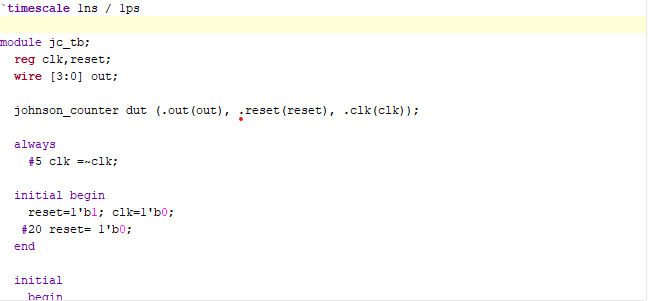


Q2. Johnson Counter

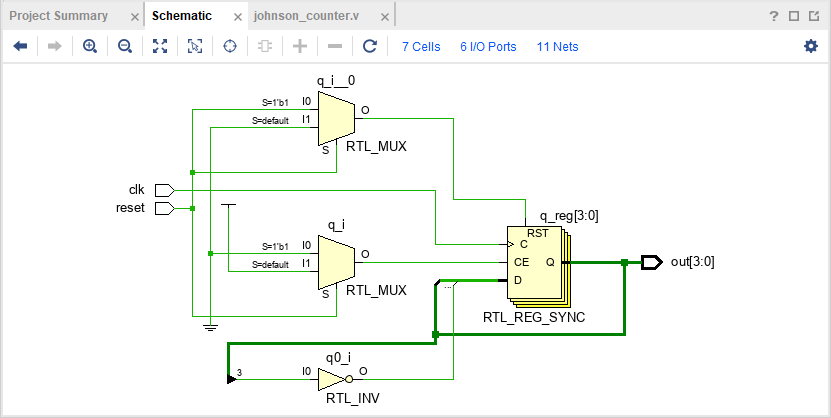
VERILOG CODE: -

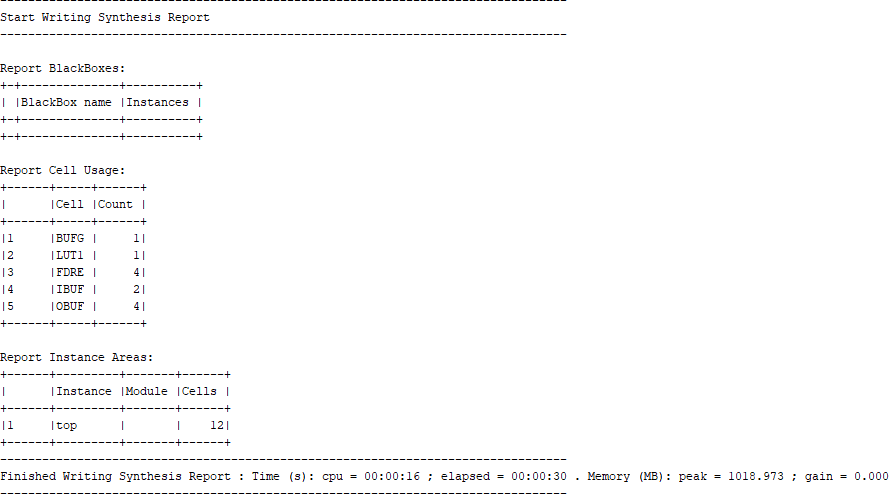


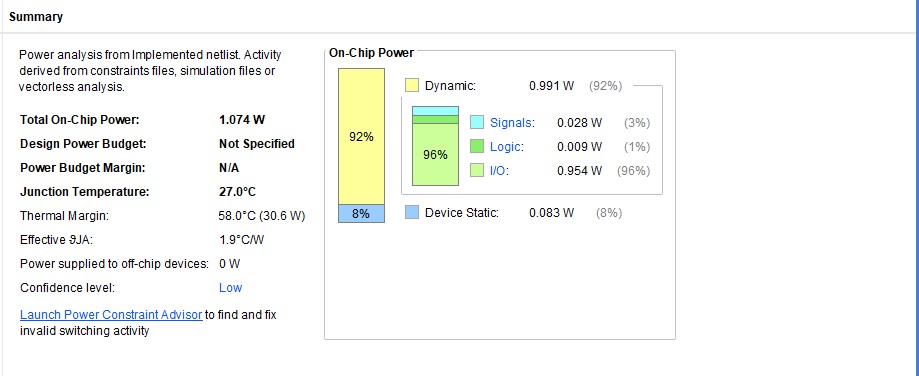
TEST BENCH: -



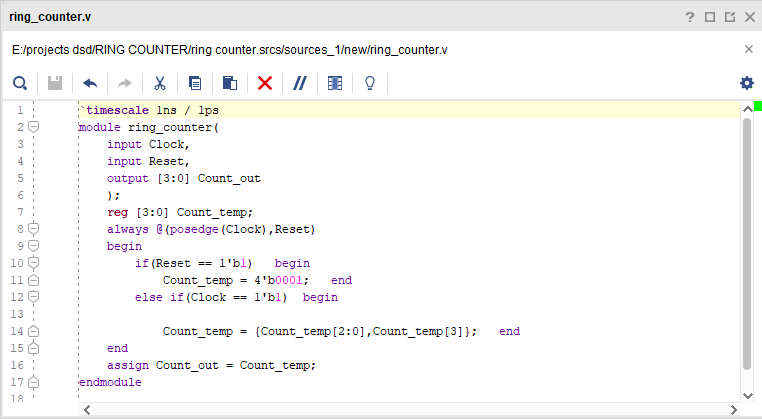
RTL SCHEMATIC: -



SYNTHESIS REPORT:

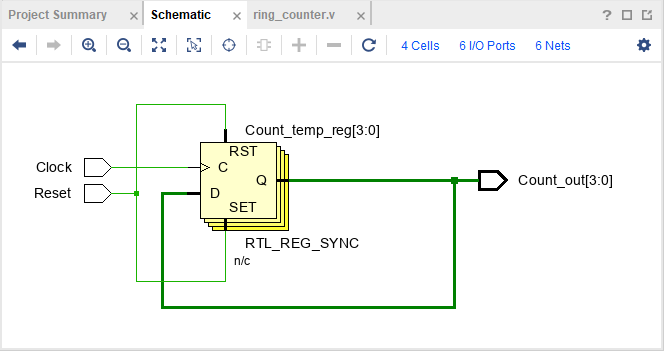


VERILOG CODE: -

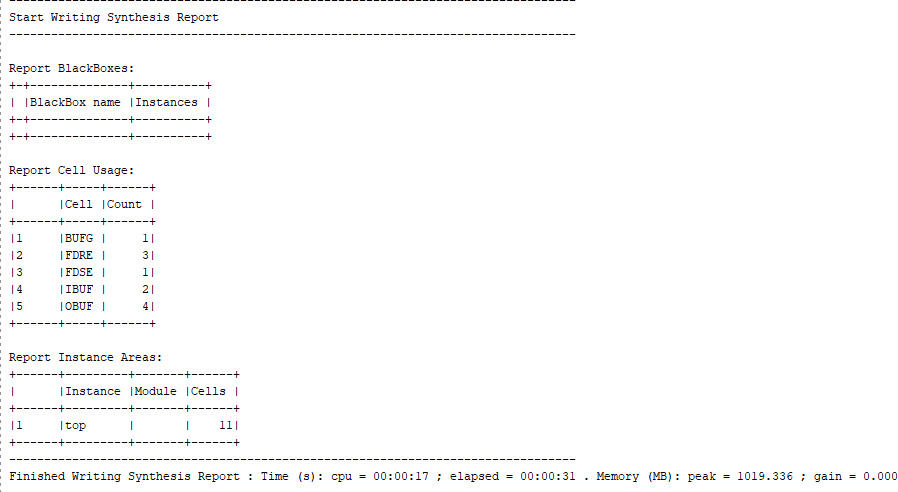


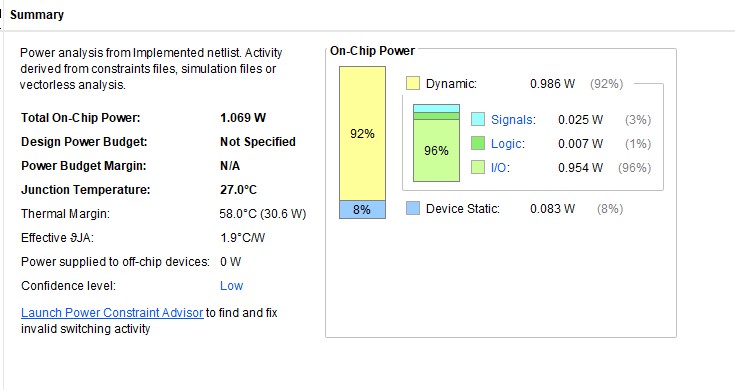
TEST BENCH: -





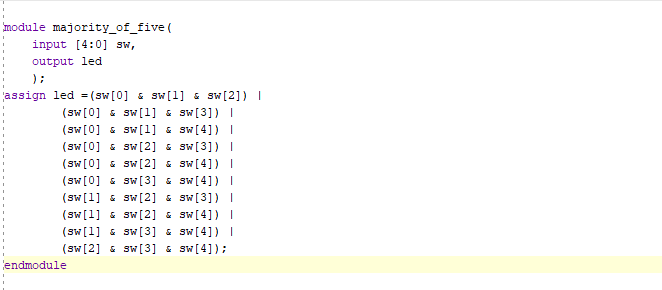
SYNTHESIS REPORT: -



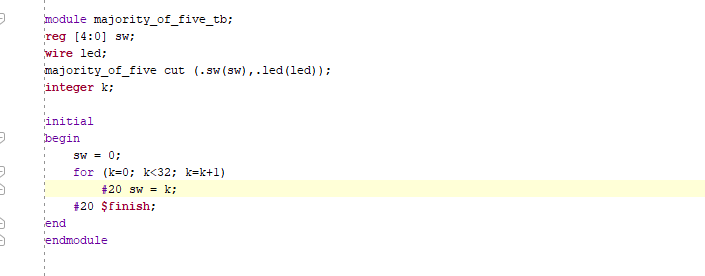


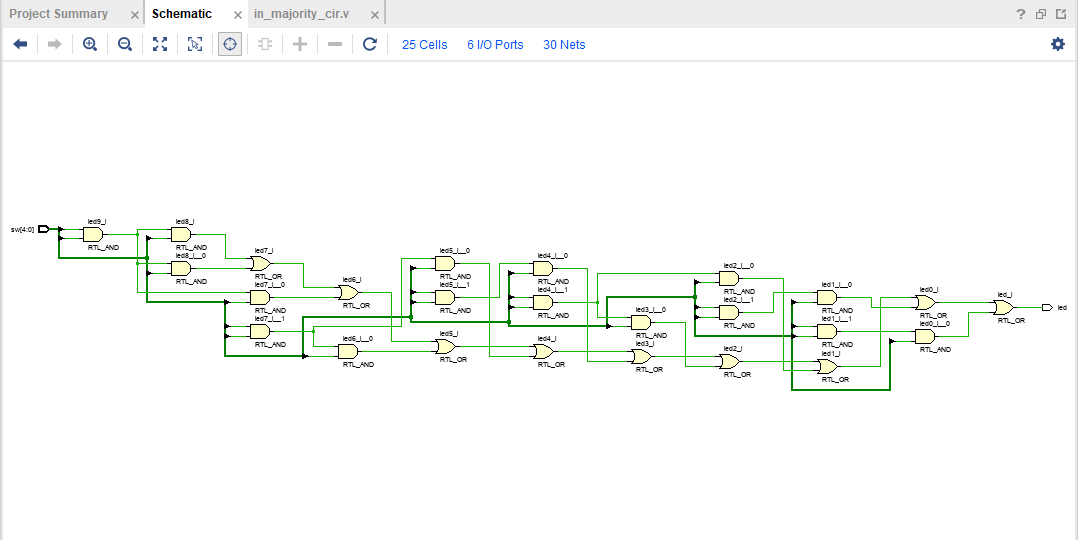
Q4. 5 INPUT MAJORITY CIRCUIT

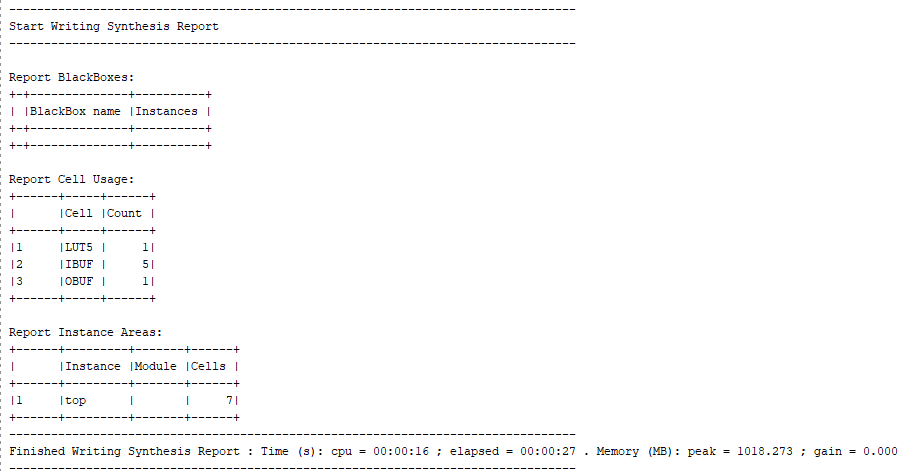
VERILOG CODE: -

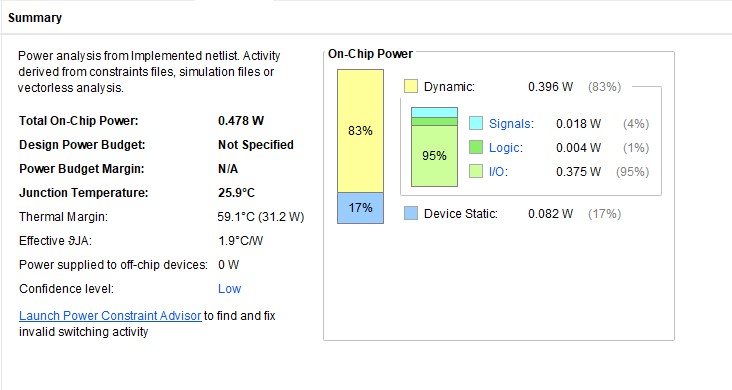


TEST BENCH:-

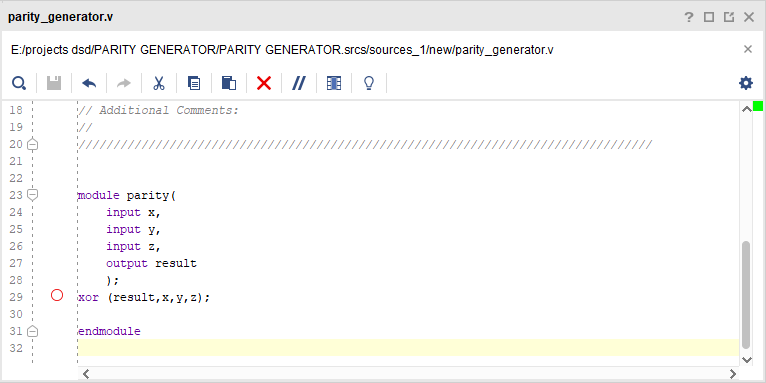






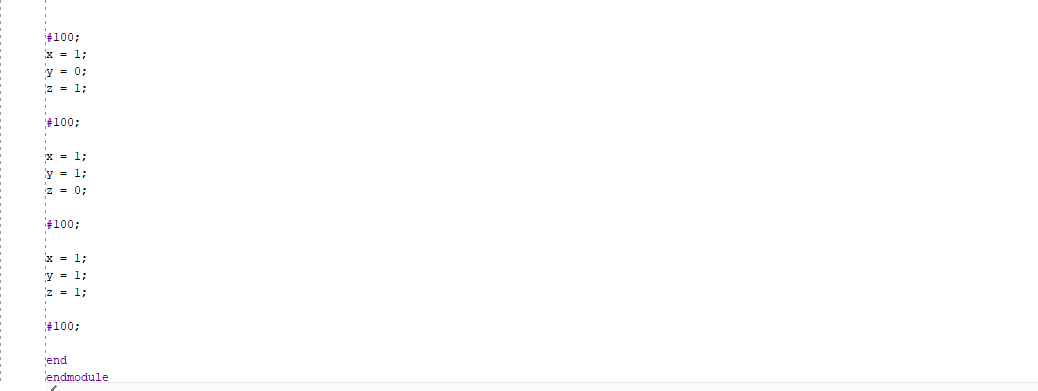


VERILOG CODE:-

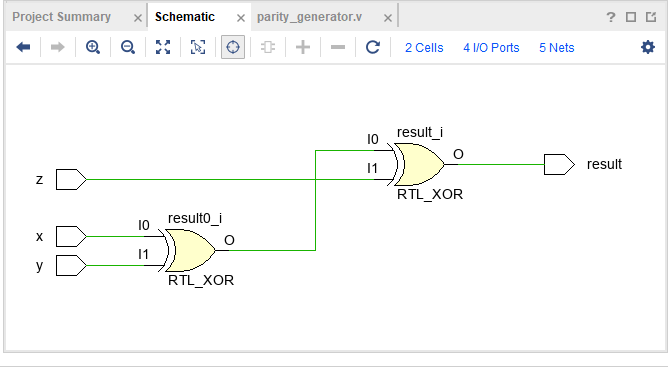


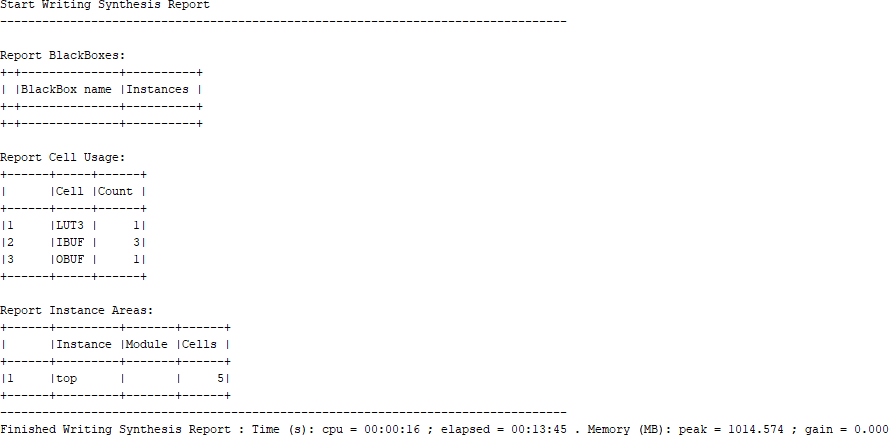
TEST BENCH:-



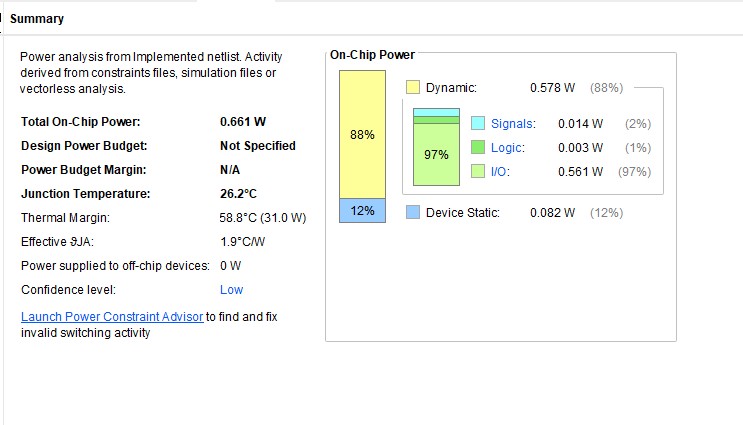


RTL SCHEMATIC:-

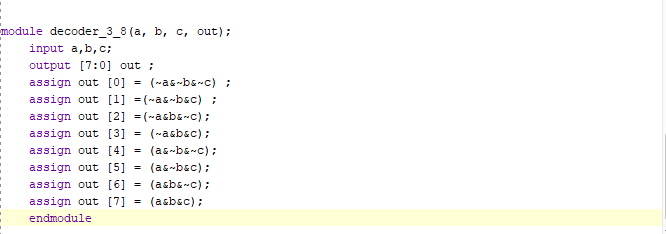




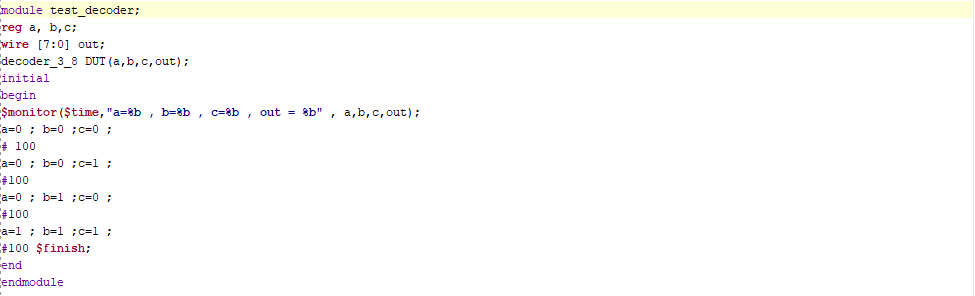
POWER REPORT:-

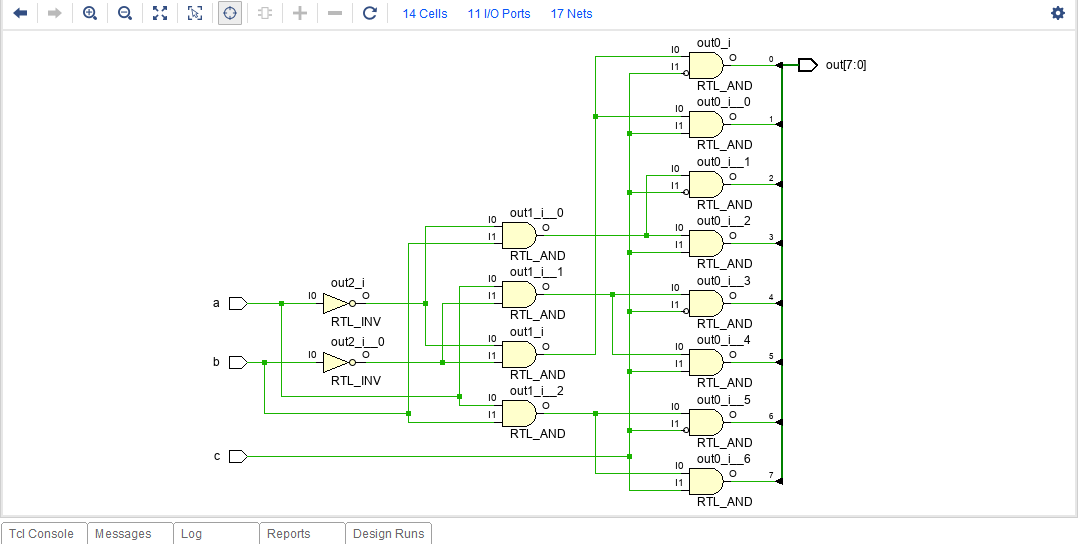


VERILOG CODE:-

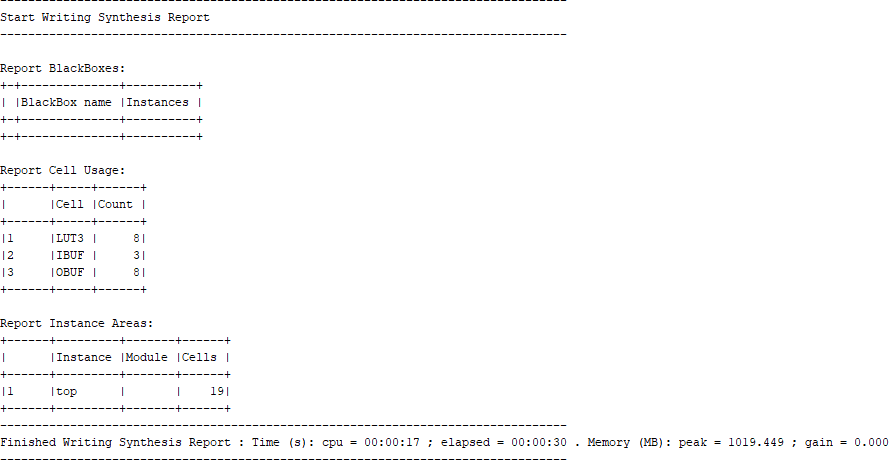


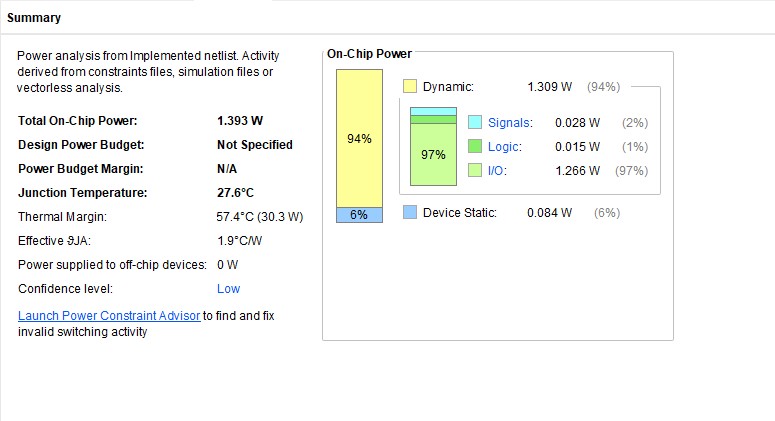
TEST BENCH:-



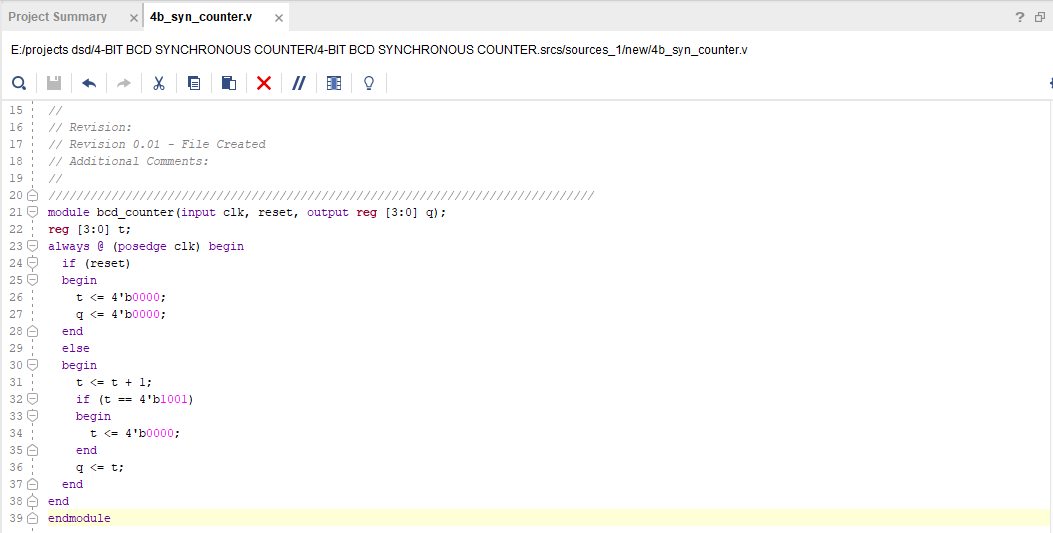


SYNTHESIS REPORT:-



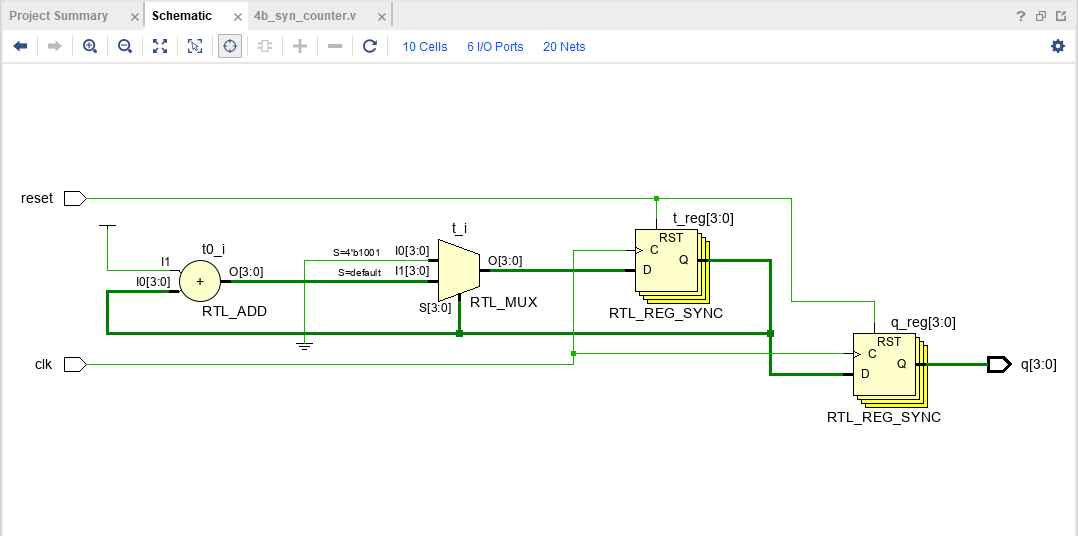


VERILOG CODE:-

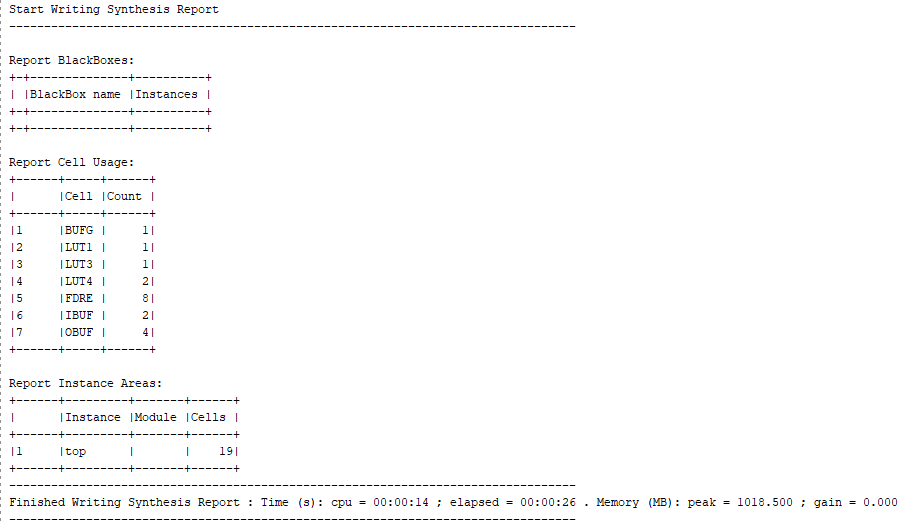


TEST BENCH:-

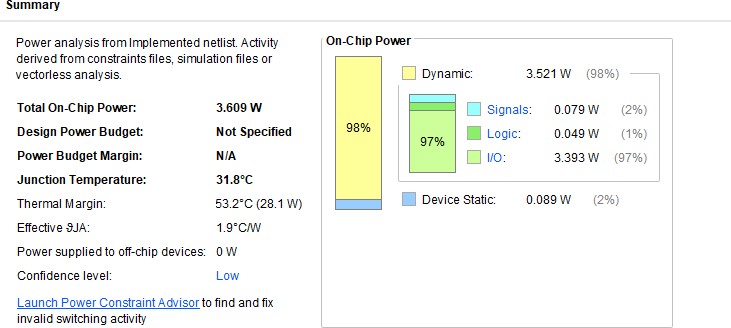




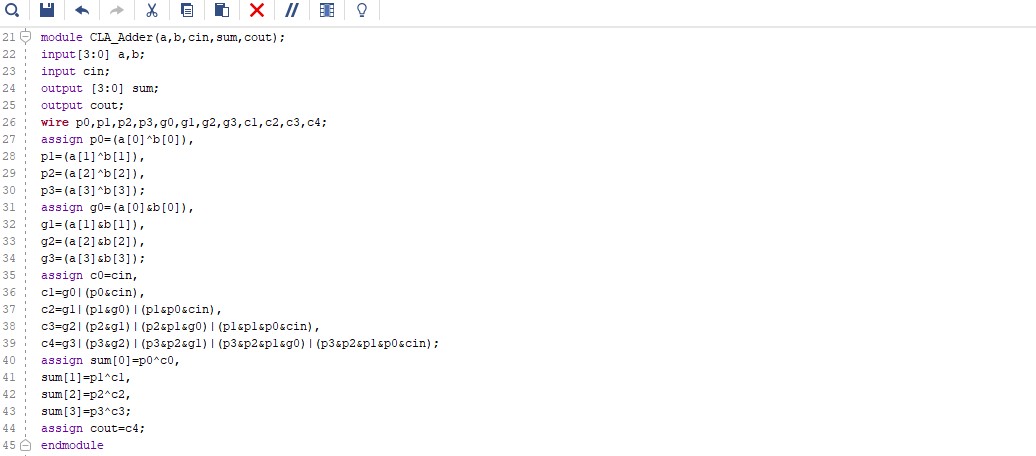
SYNTHESIS REPORT:-



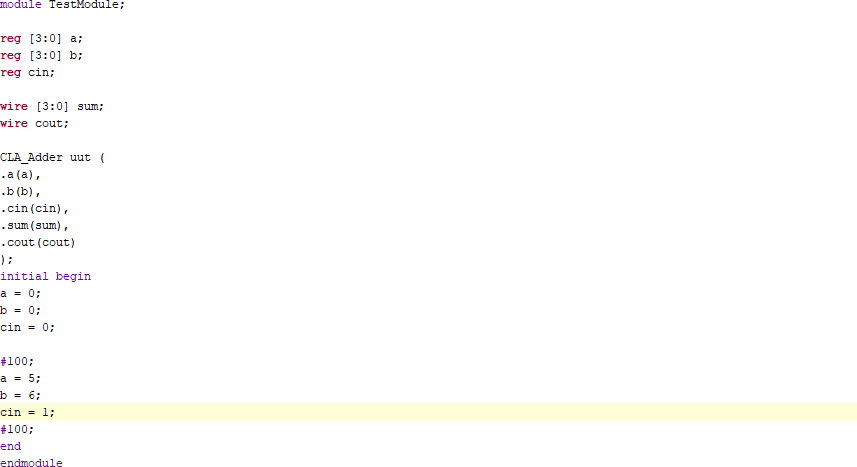
POWER REPORT:-

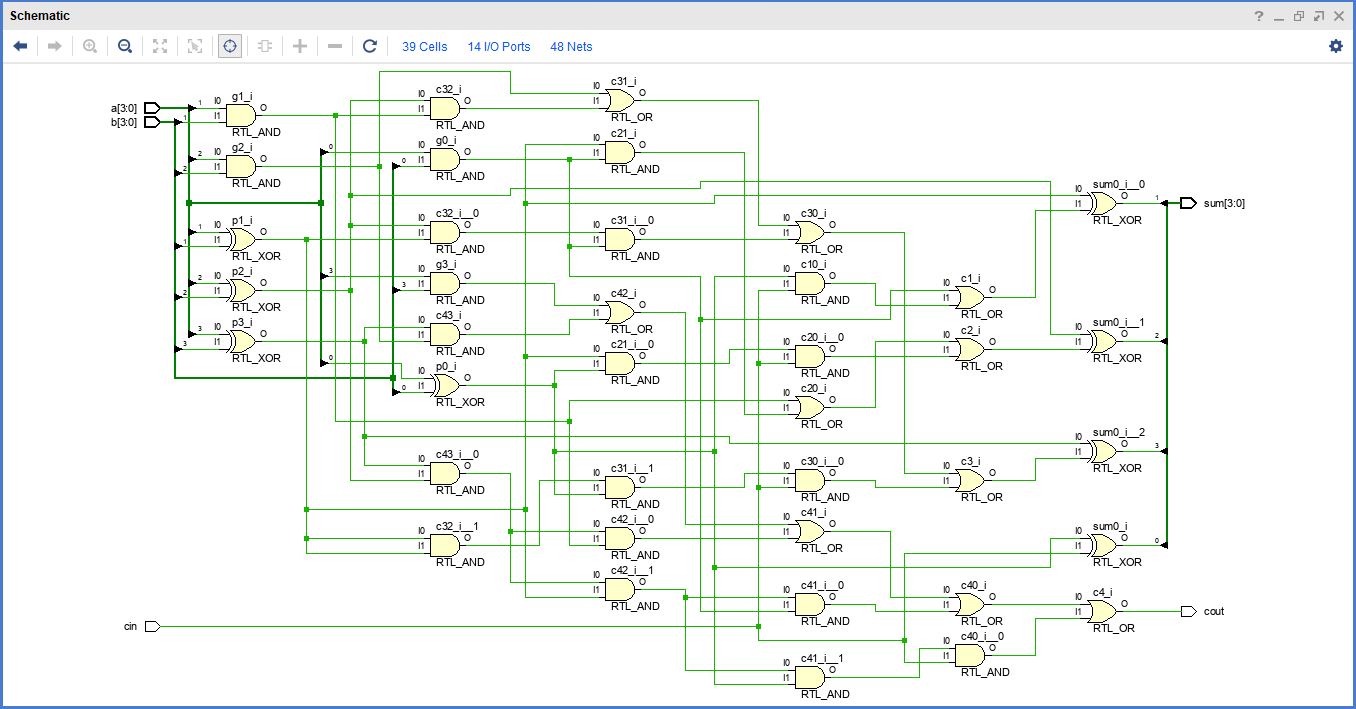


VERILOG CODE:-

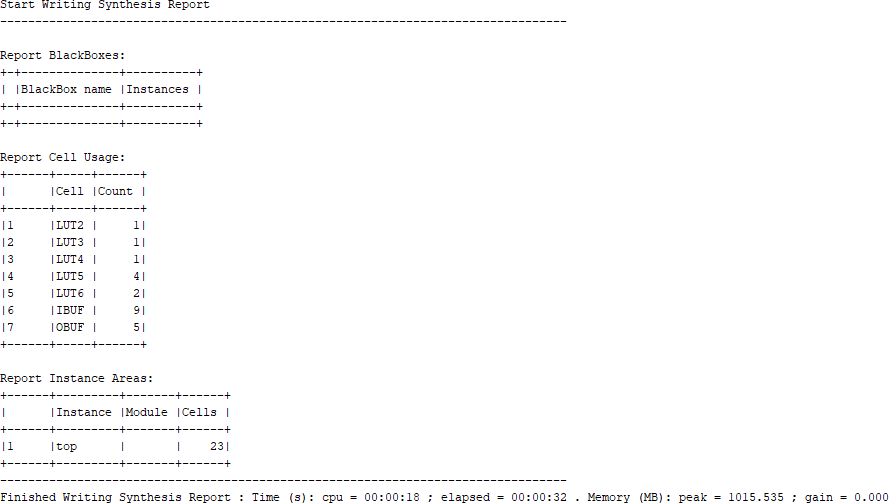


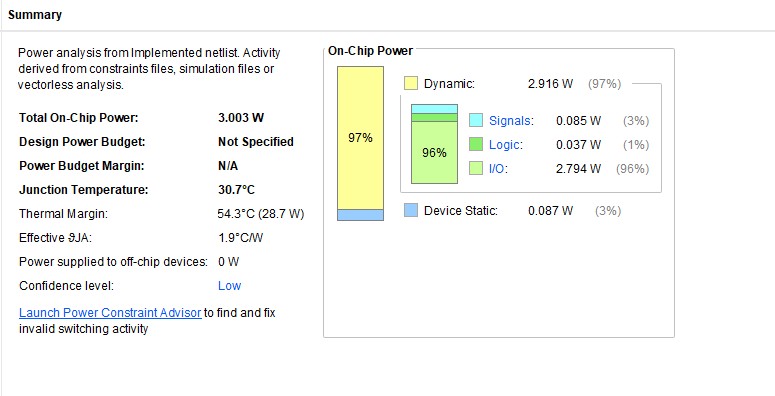
TEST BENCH:-



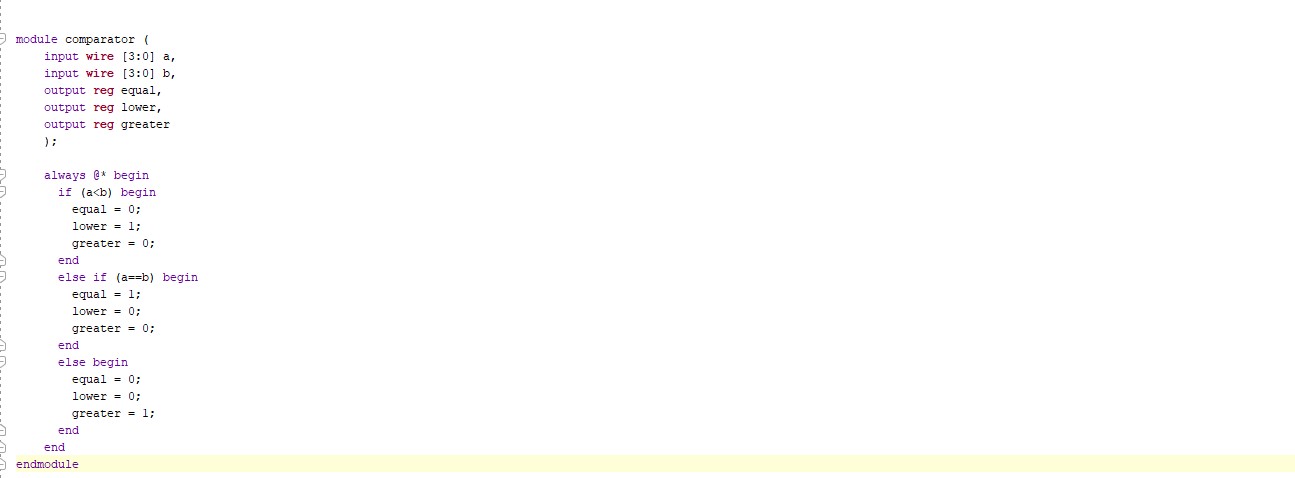


SYNTHESIS REPORT:-



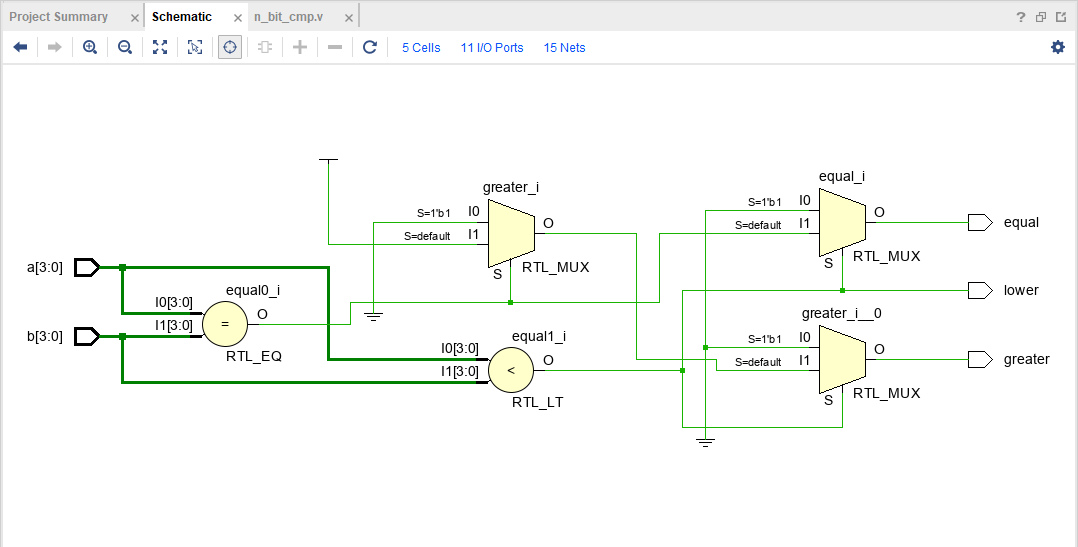


VERILOG CODE:-

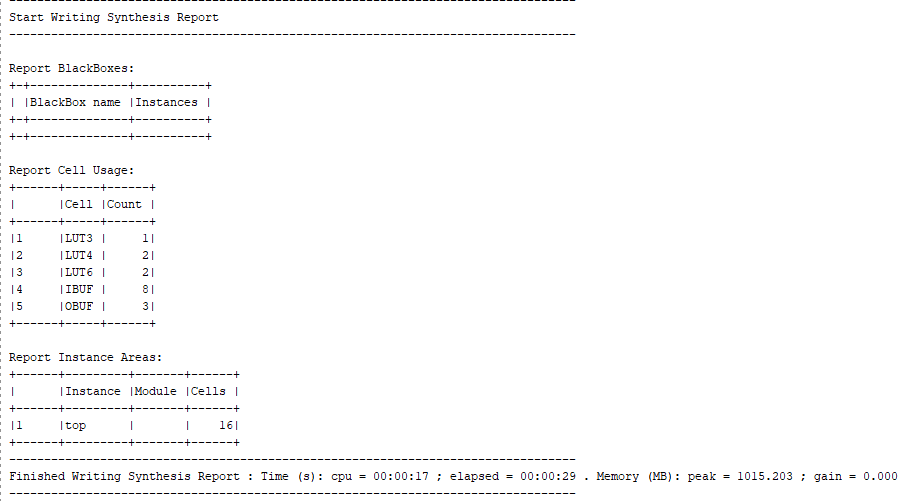


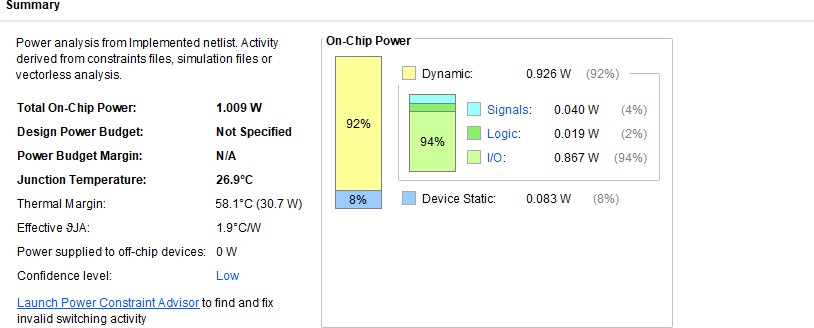
TEST BENCH:-



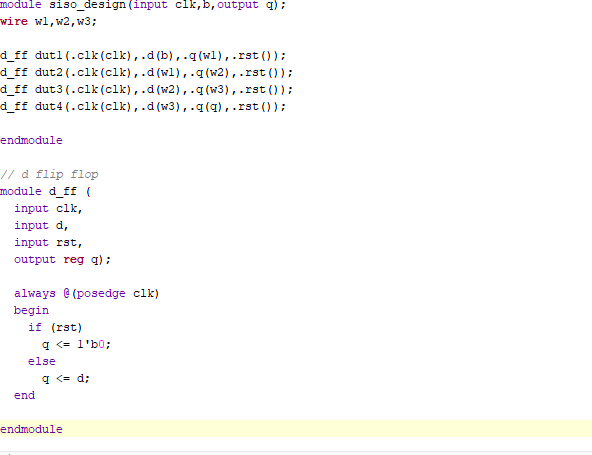


SYNTHESIS REPORT:-

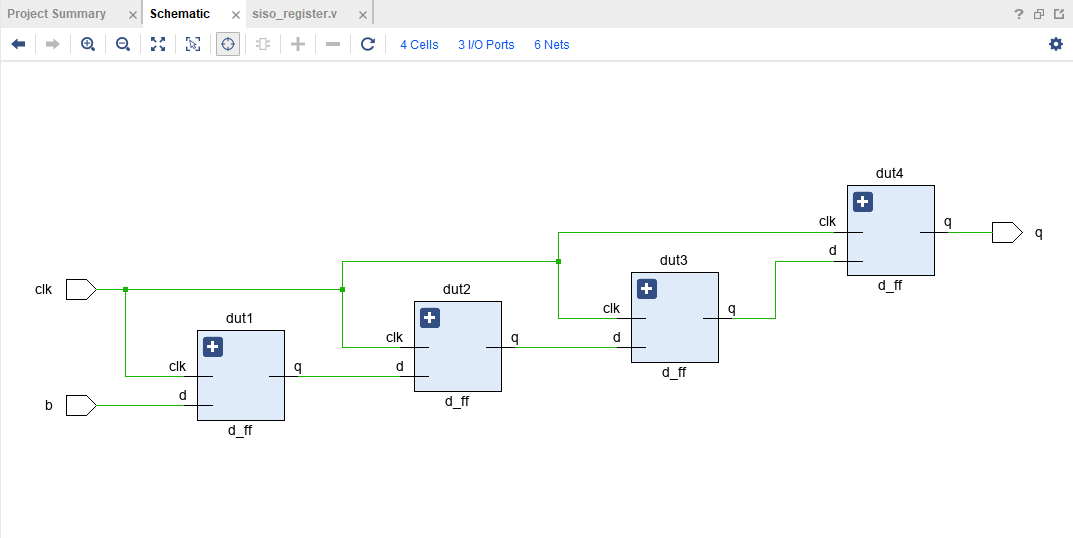




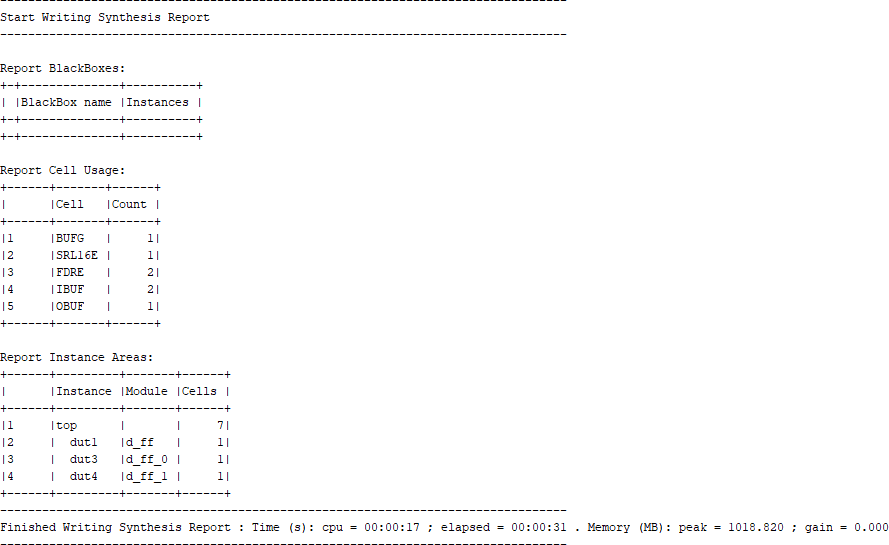
VERILOG CODE:-

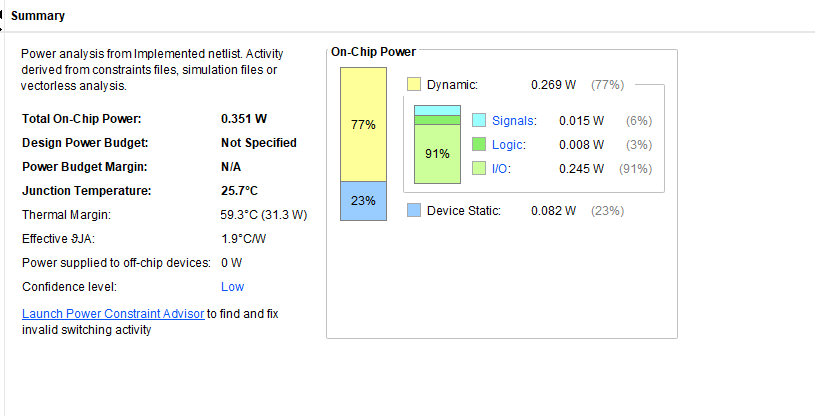




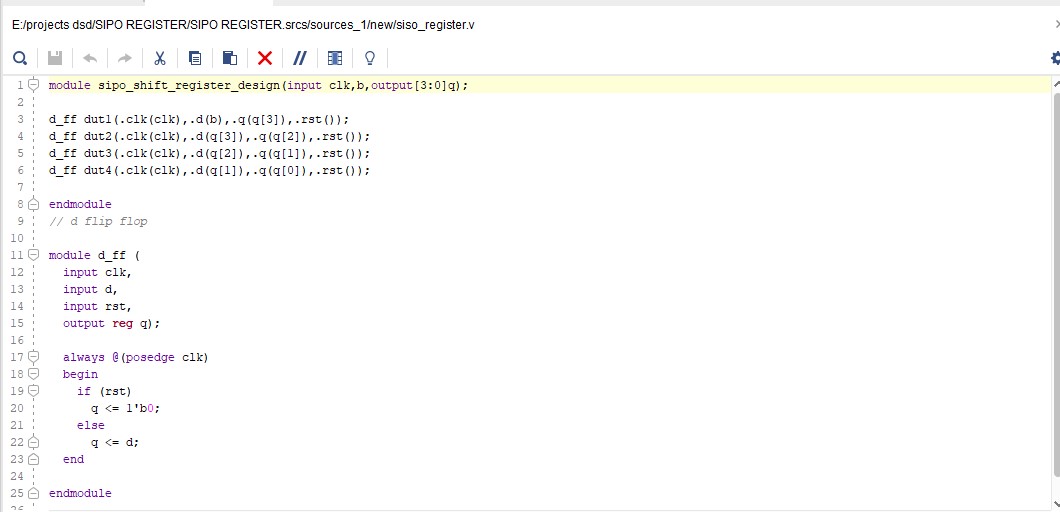


SYNTHESIS REPORT:-

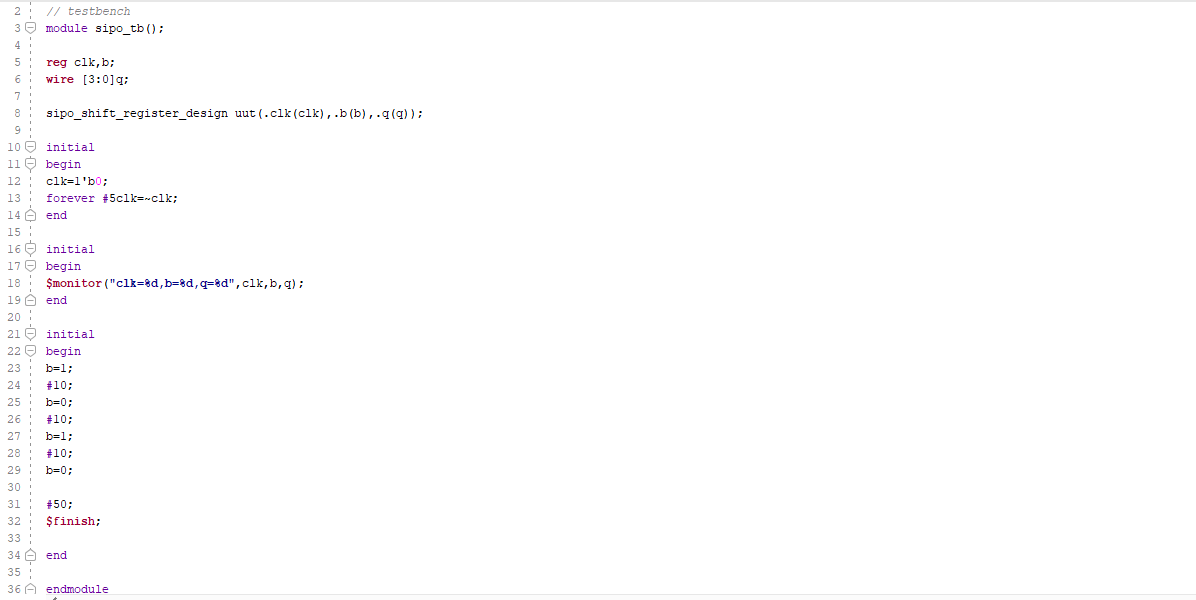


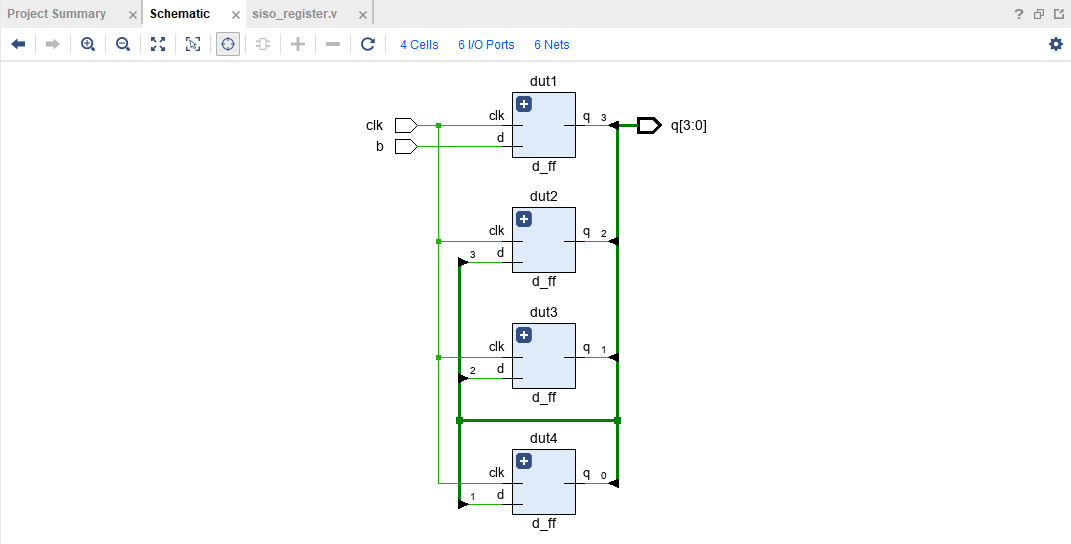


VERILOG CODE:-

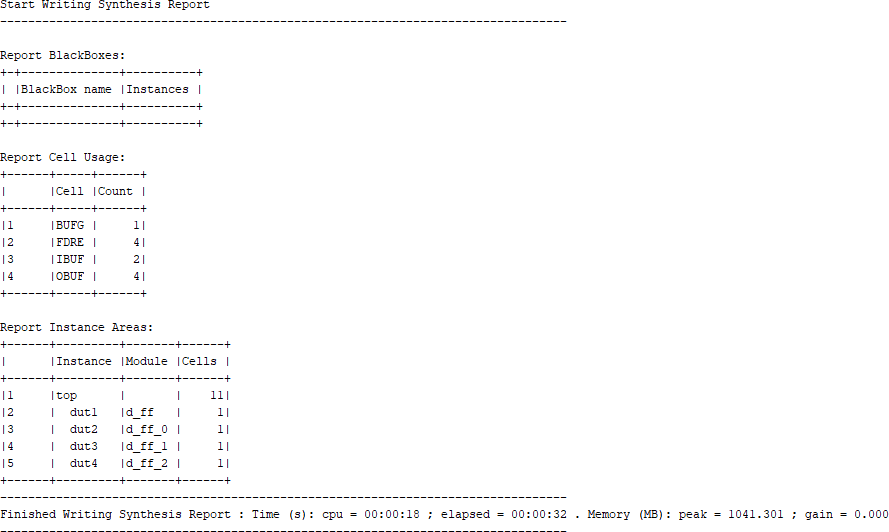


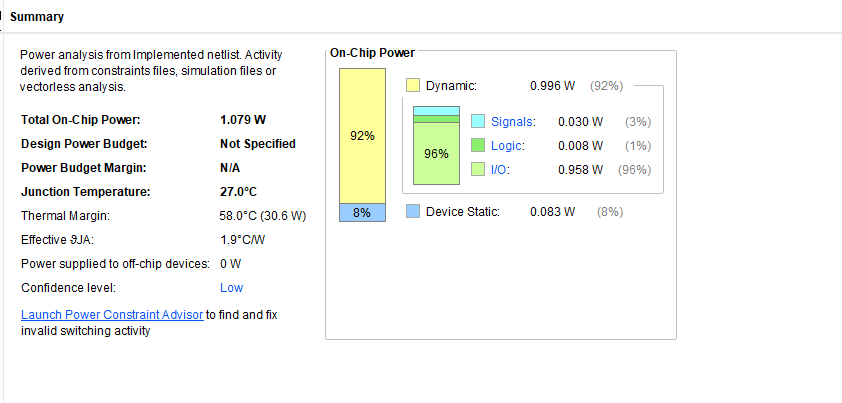
TEST BENCH:-





SYNTHESIS REPORT:-



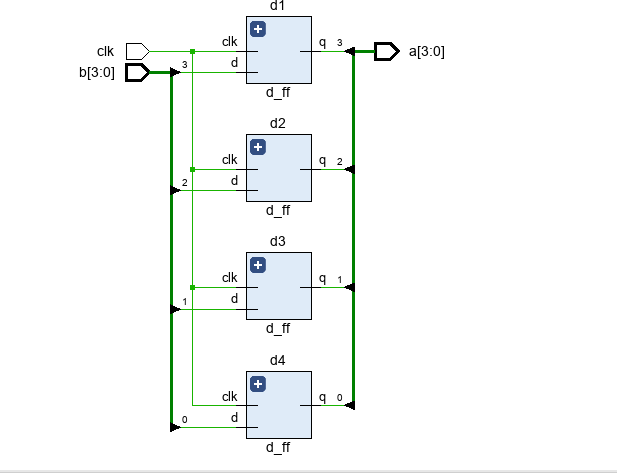


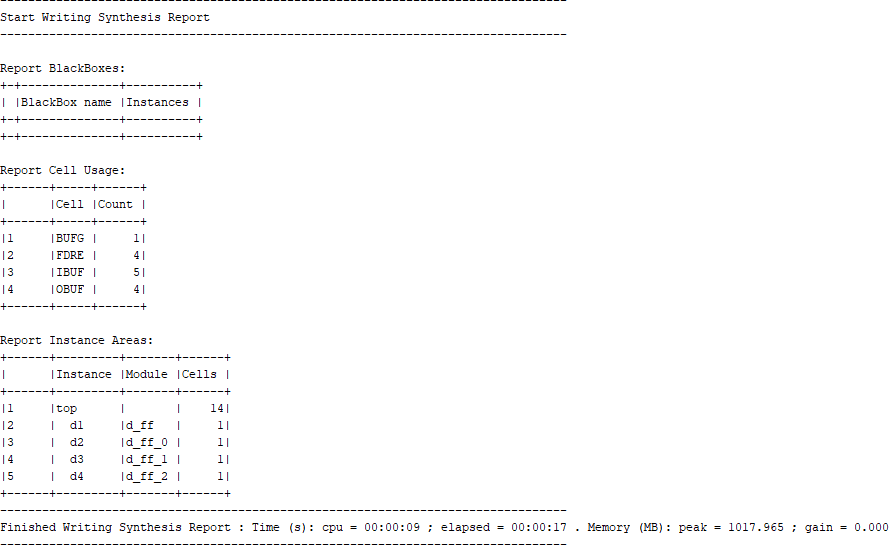
VERILOG CODE:-



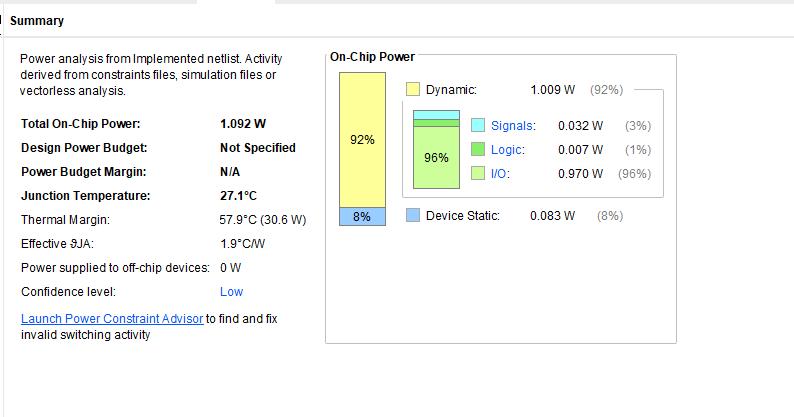
TEST BENCH:-



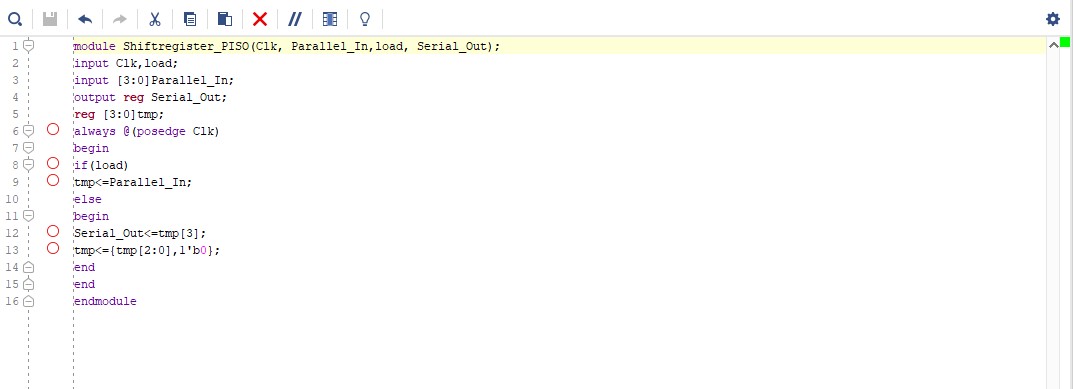




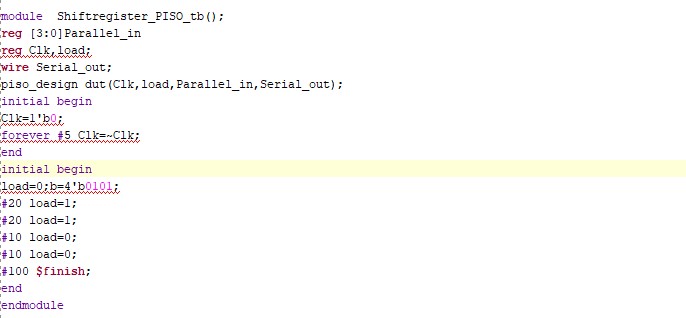
POWER REPORT:-

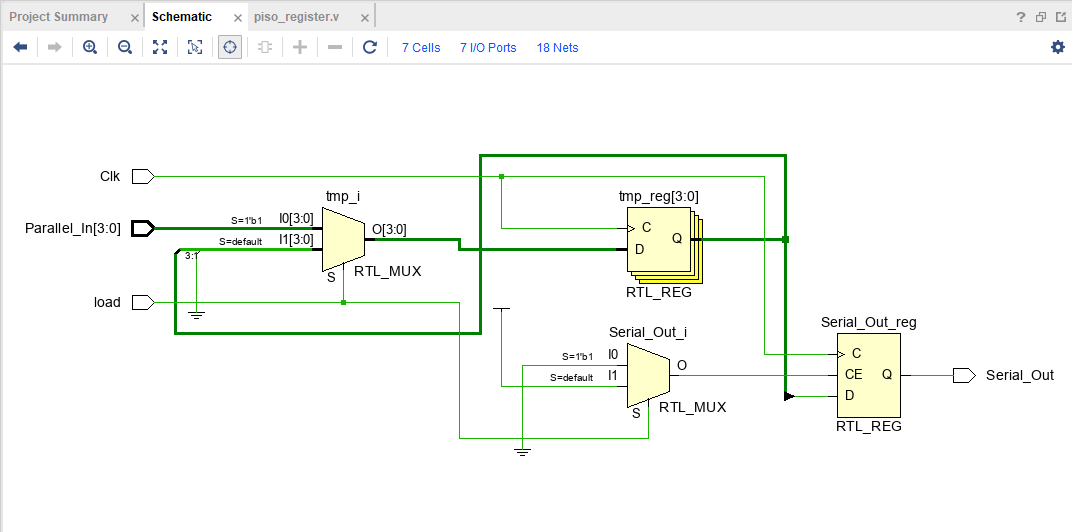


# Q13. PARALLEL IN SERIAL OUT REGISTER VERILOG CODE:-

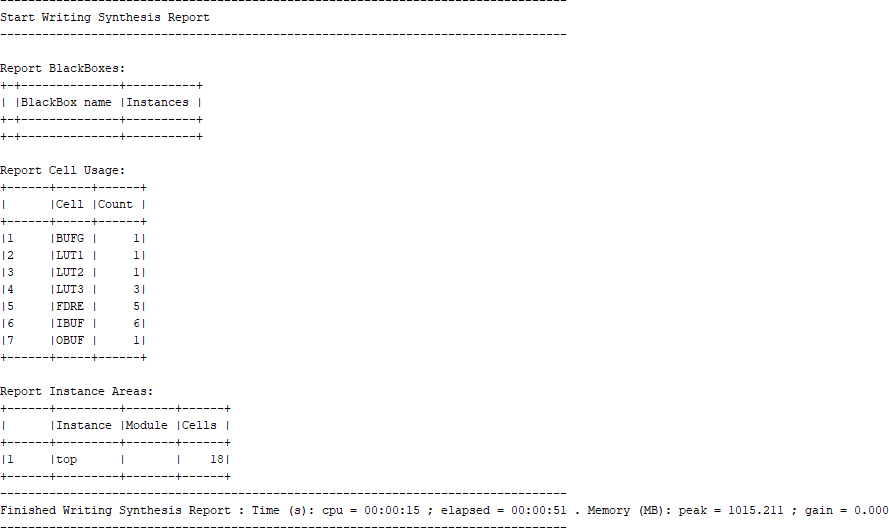


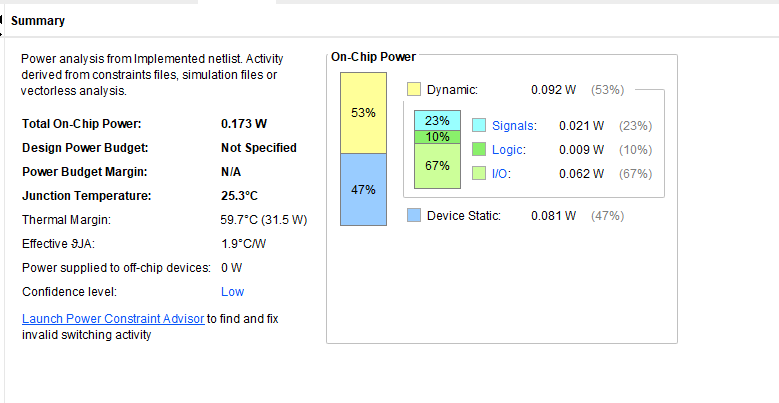
TEST BENCH:-



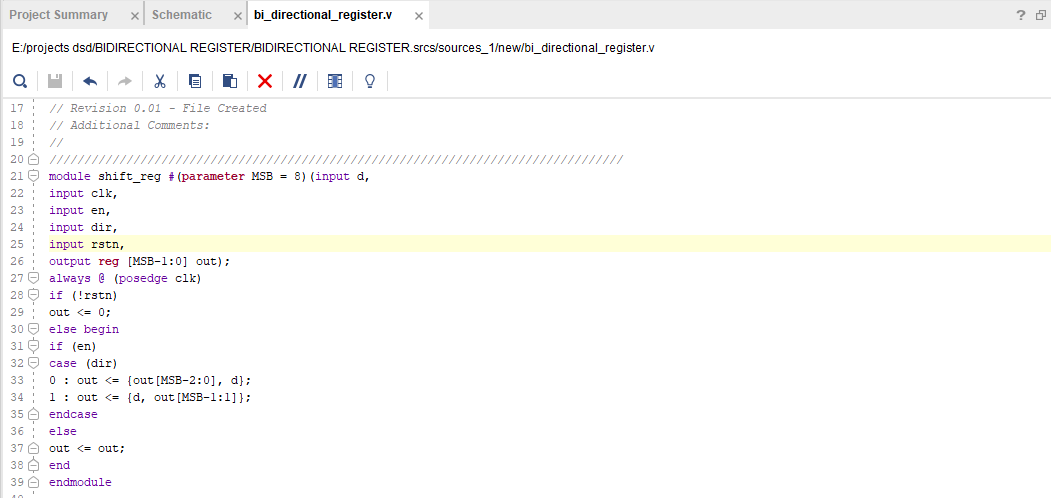


SYNTHESIS REPORT:-

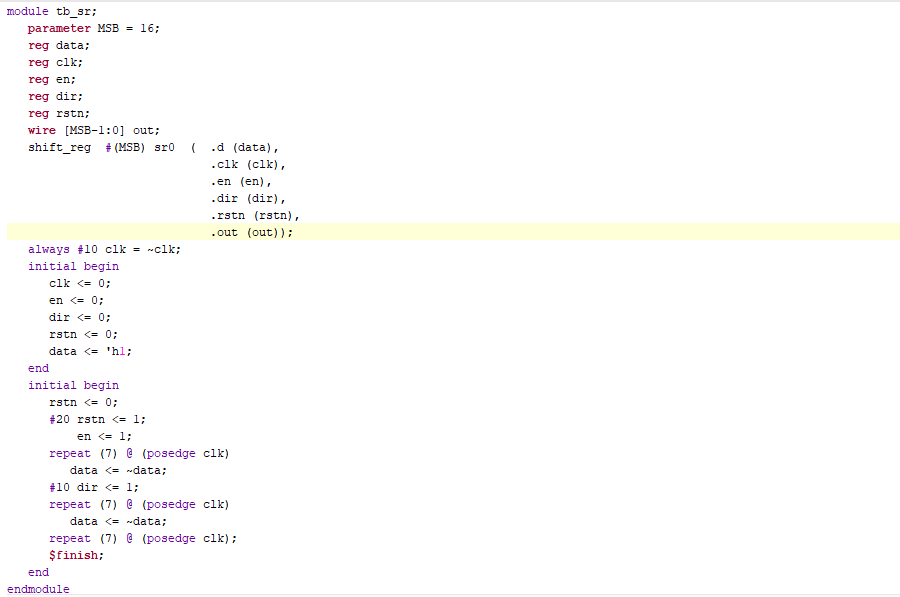


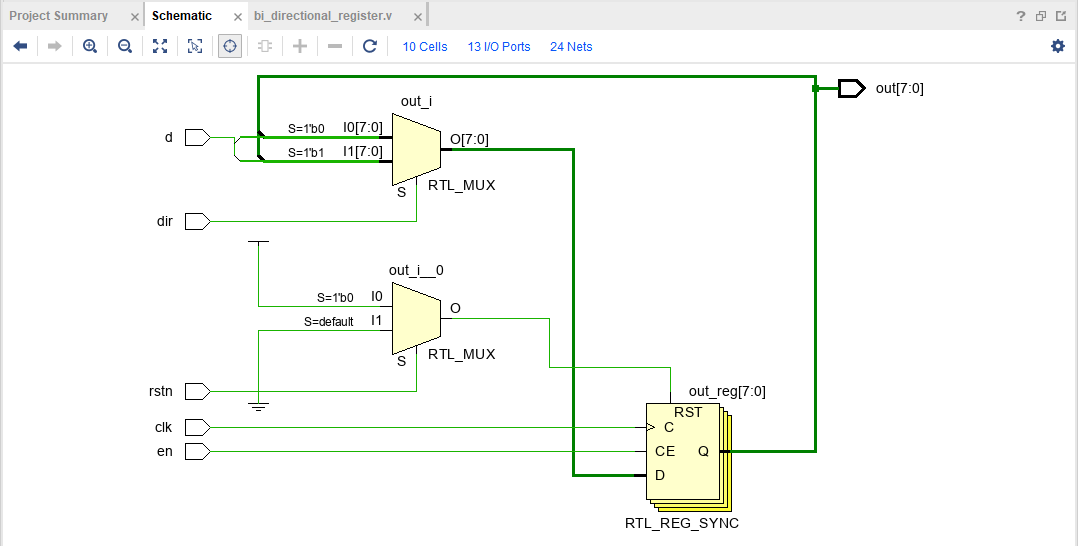


VERILOG CODE:-

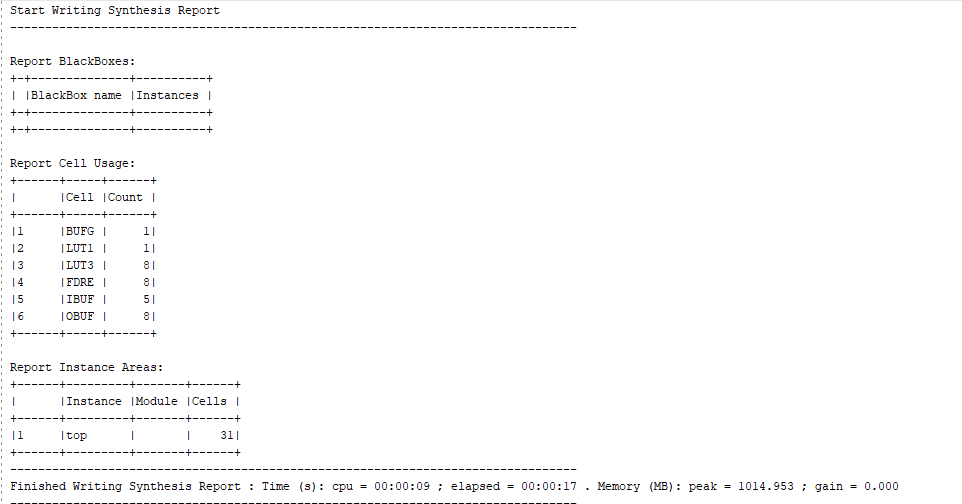


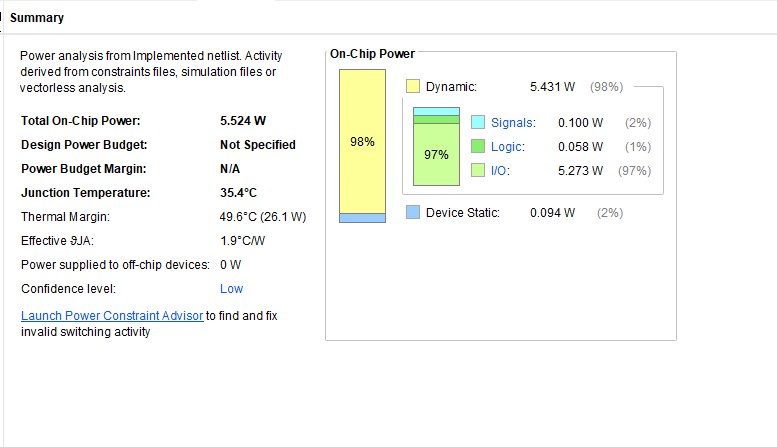
TEST BENCH:-



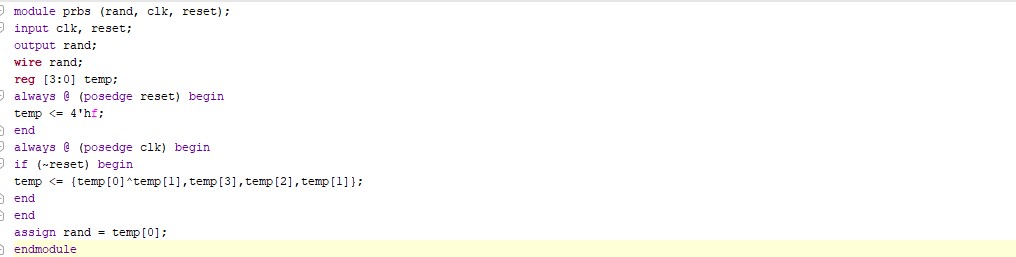


SYNTHESIS REPORT:-

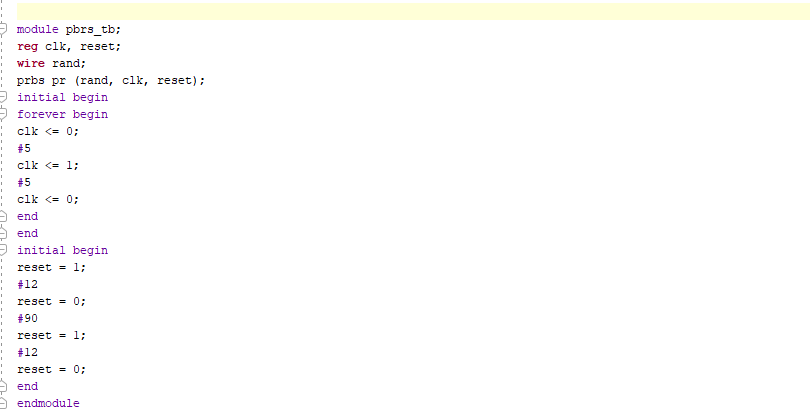


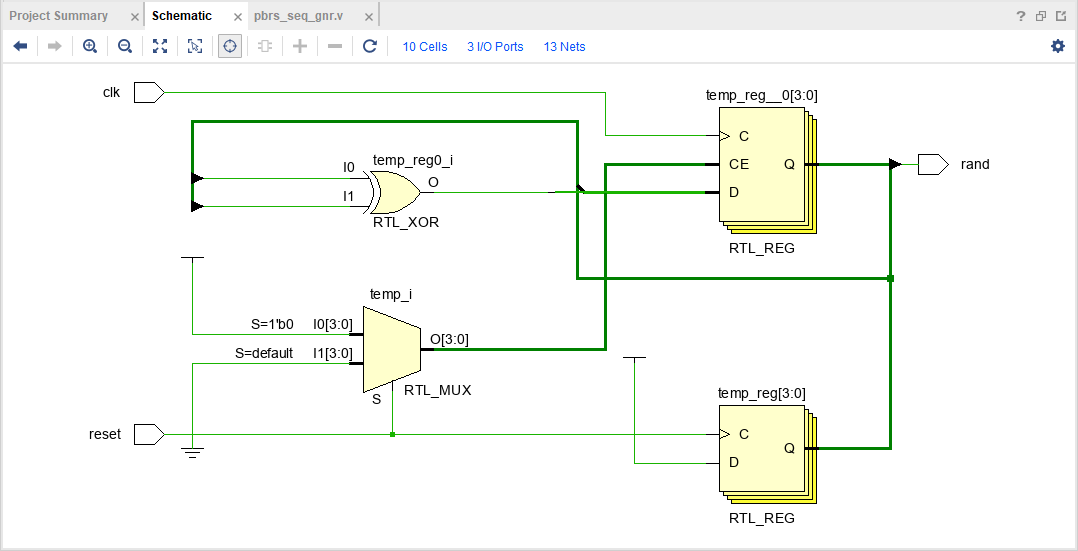


# VERILOG CODE:-

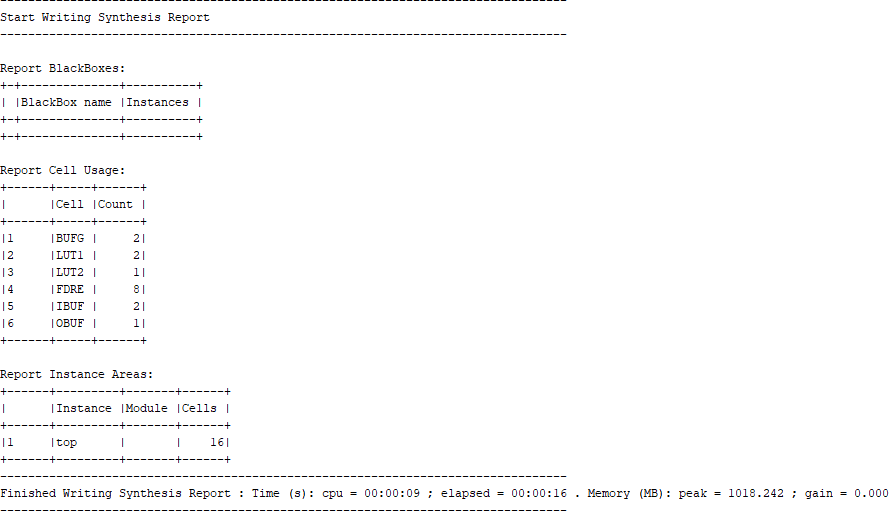


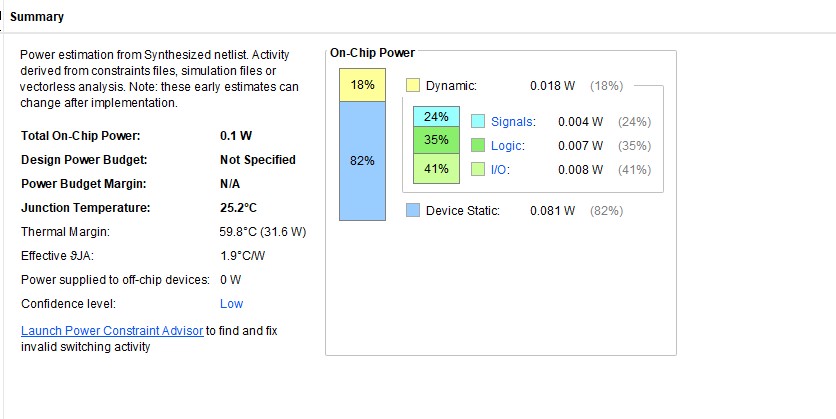
TEST BENCH:-





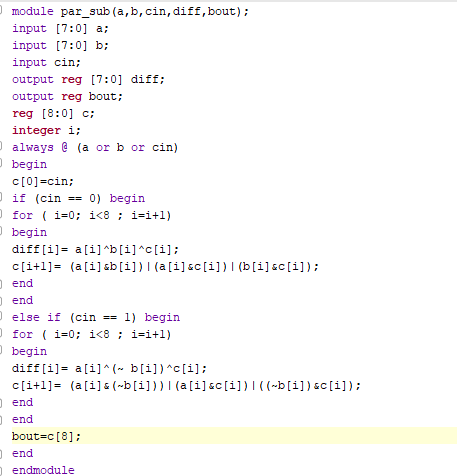
# SYNTHESIS REPORT:-





Q16 & 17. 8-BIT ADDER/SUBTRACTOR

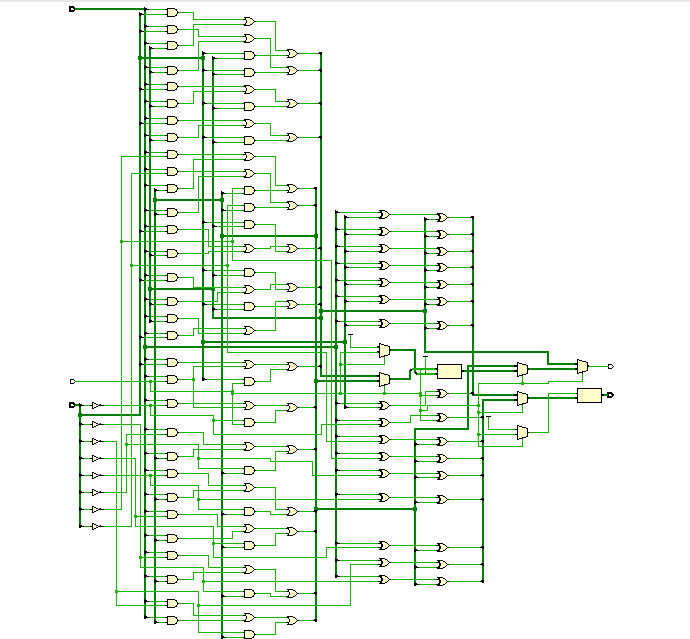
VERILOG CODE:-



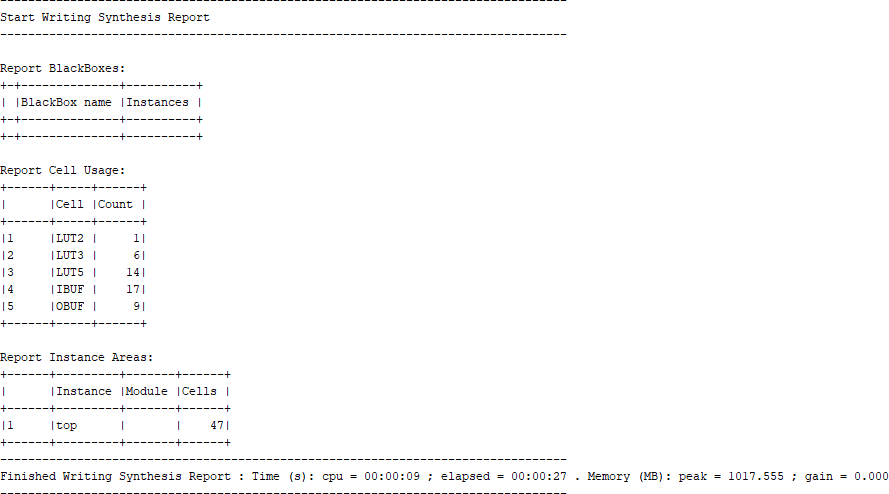
# TEST BENCH:-



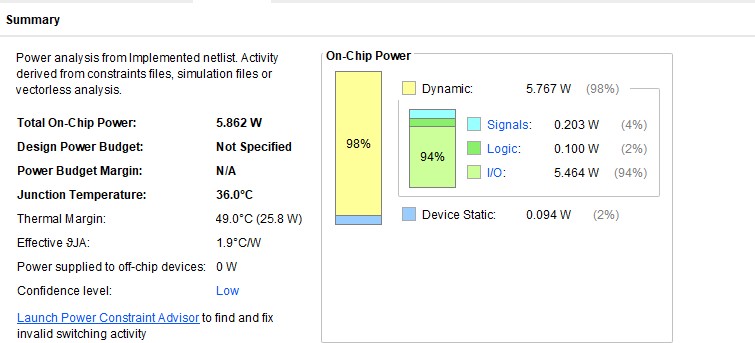
RTL SCHEMATIC:-

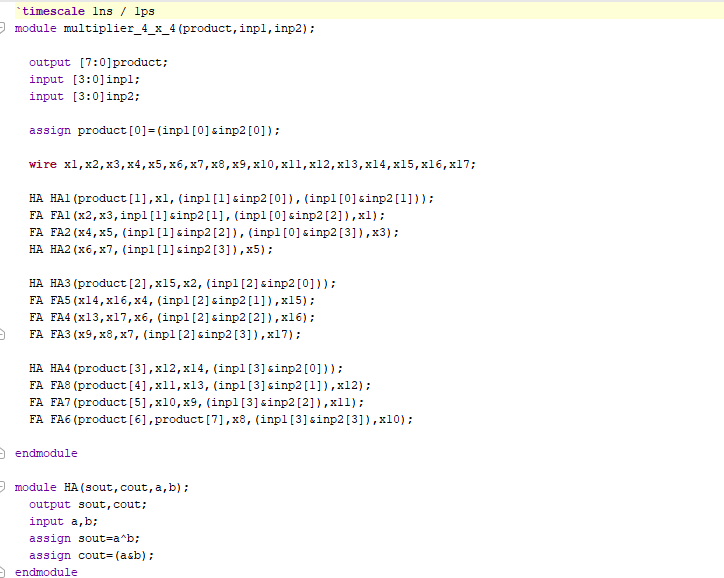


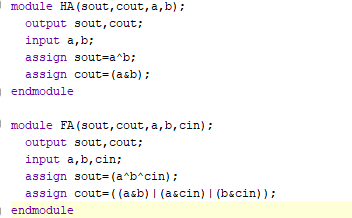
# SYNTHESIS REPORT:-

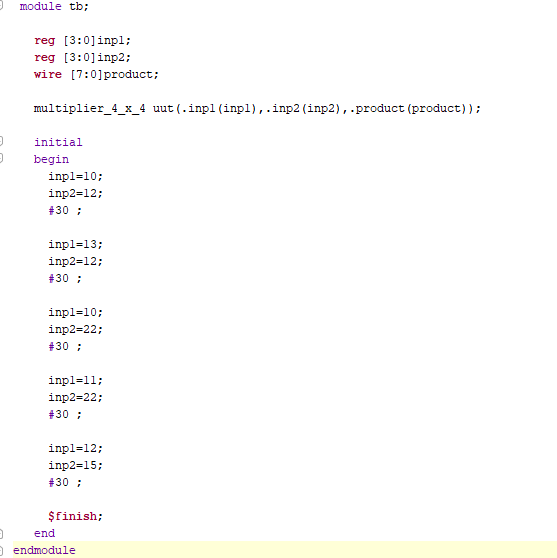


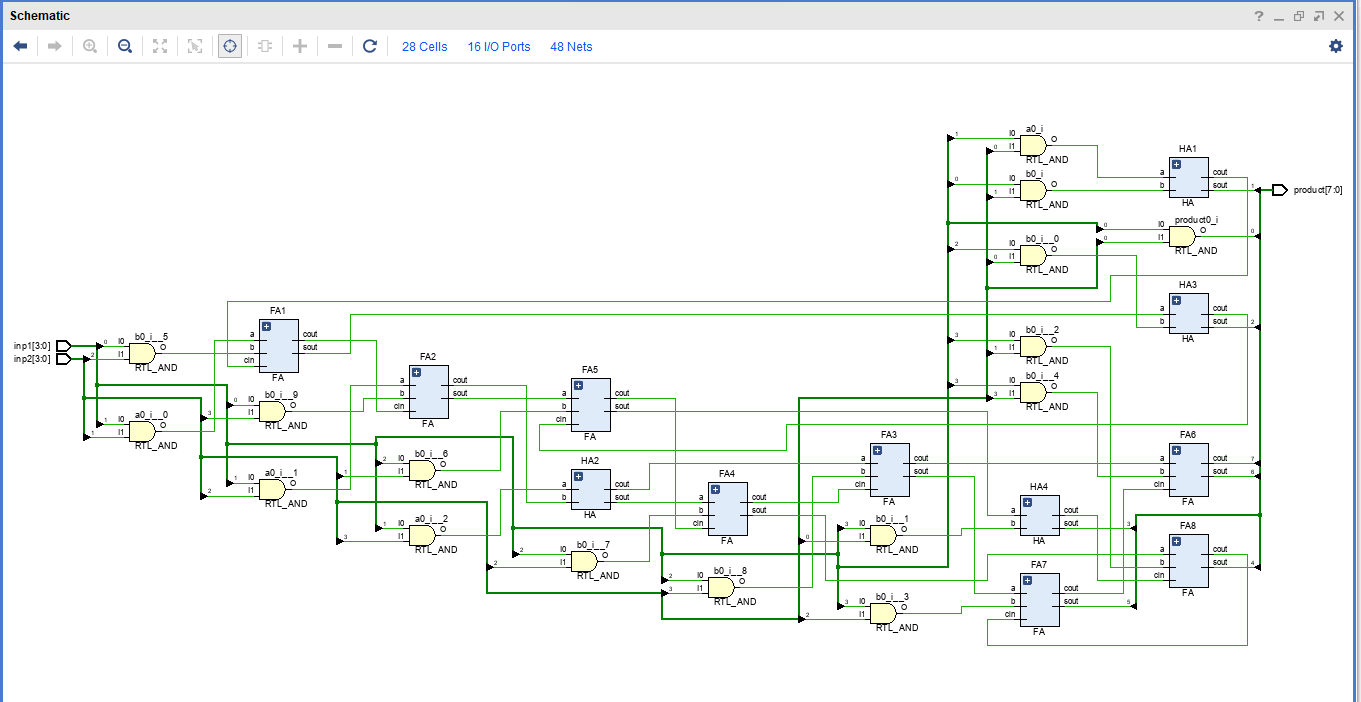
POWER REPORT:-



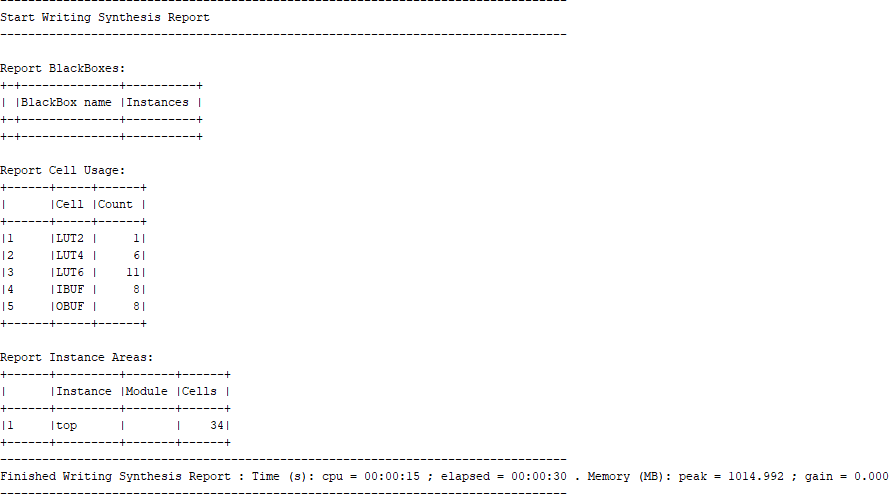
Q18. 4-BIT MULTIPLIER VERILOG CODE:-

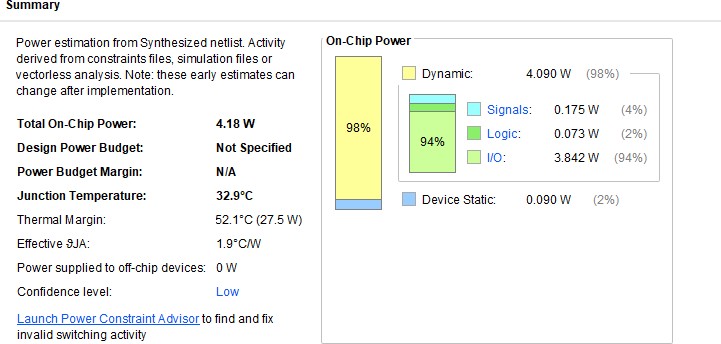




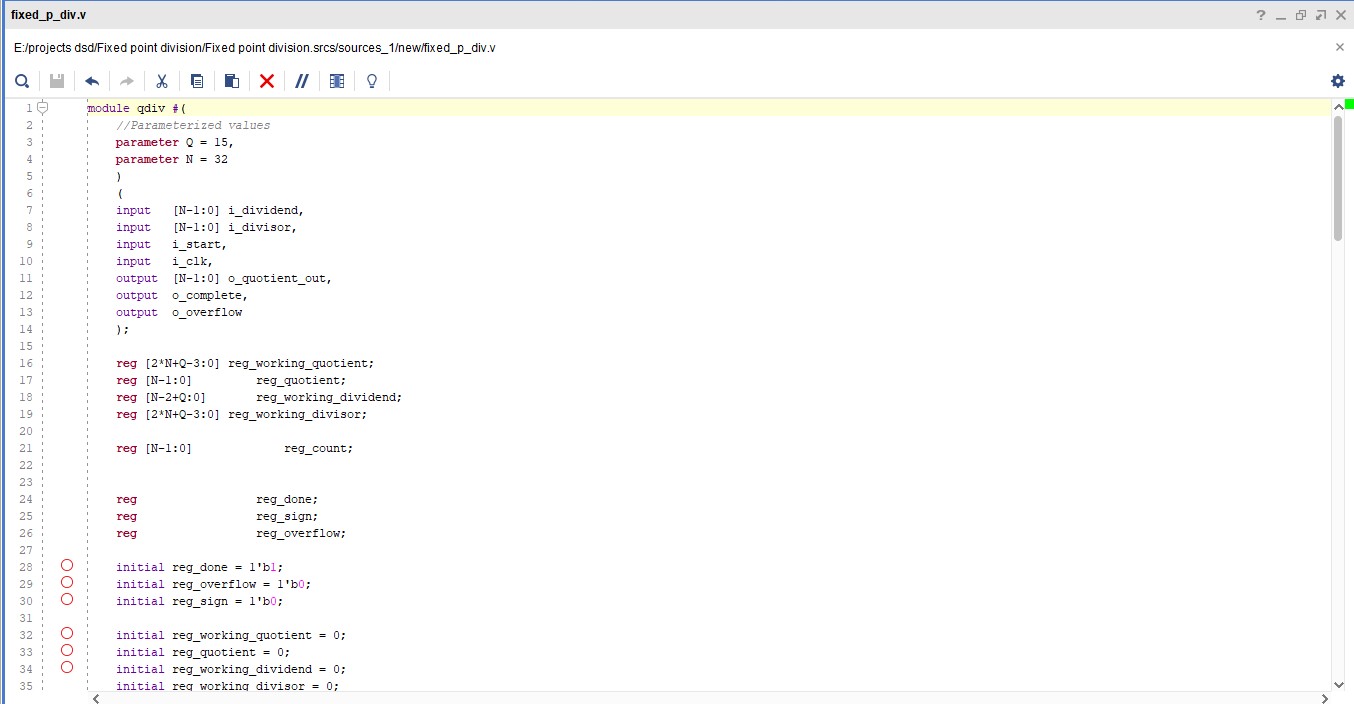


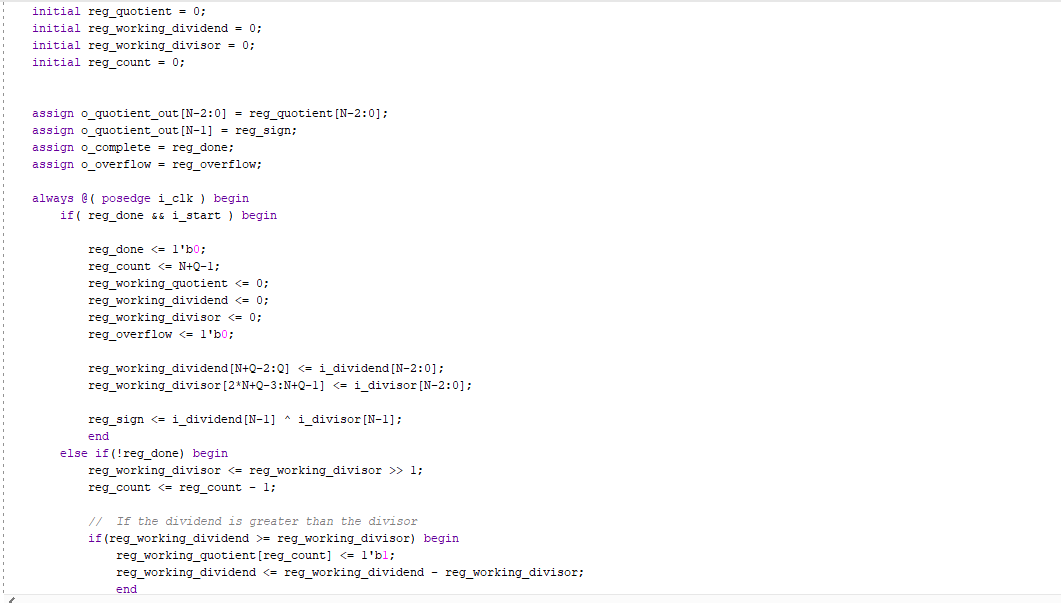
# SYNTHESIS REPORT:-

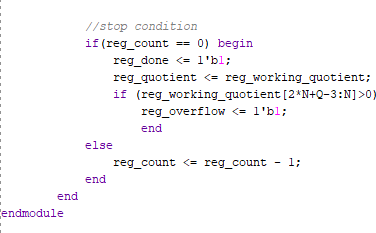




Q19. FIXED POINT DIVISION VERILOG CODE:-

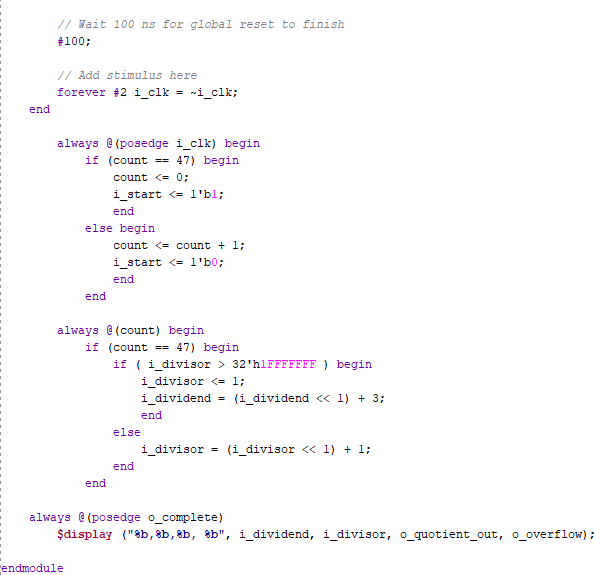




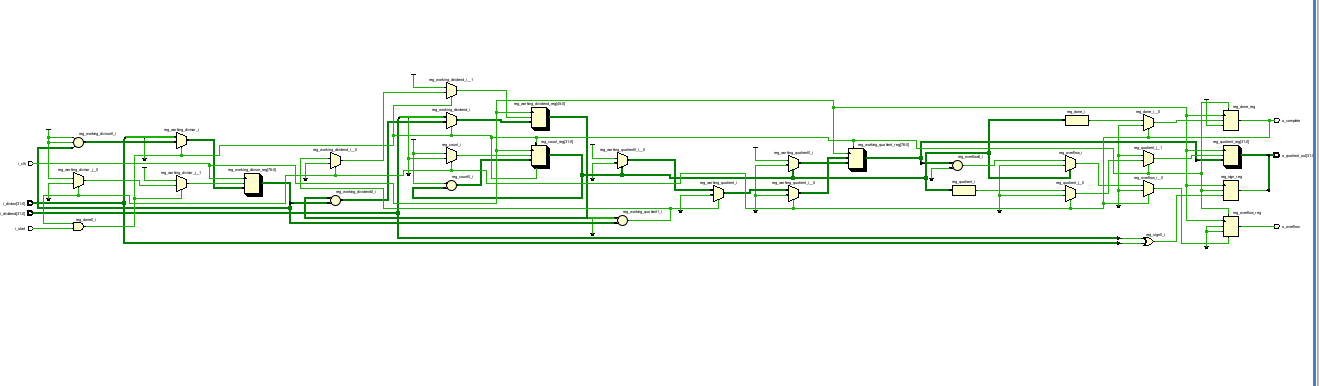


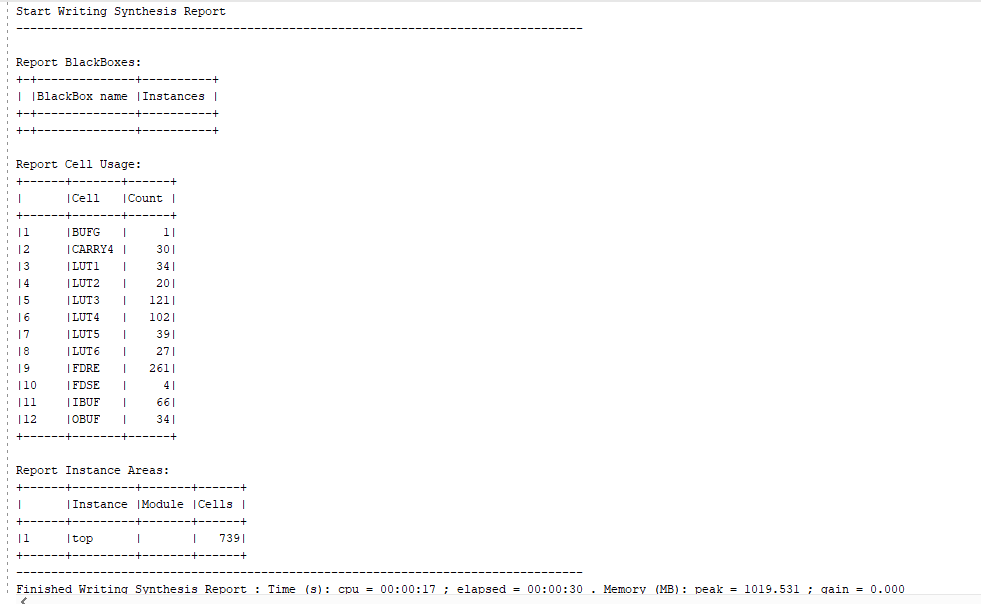
TEST BENCH:-



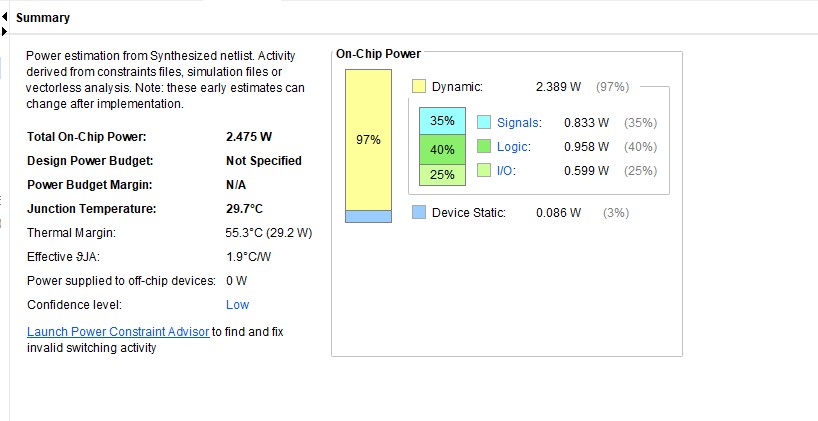


RTL SCHEMATIC:-

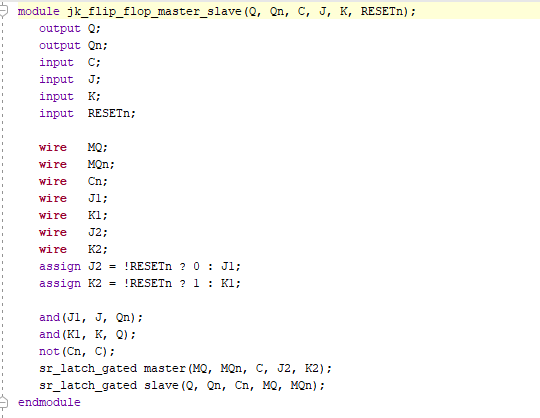


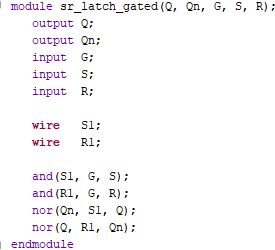


POWER REPORT:-

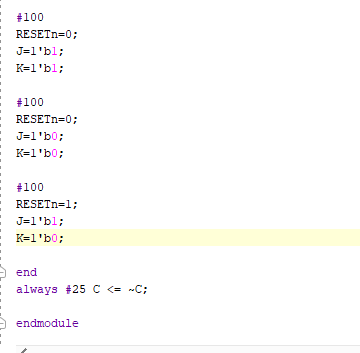


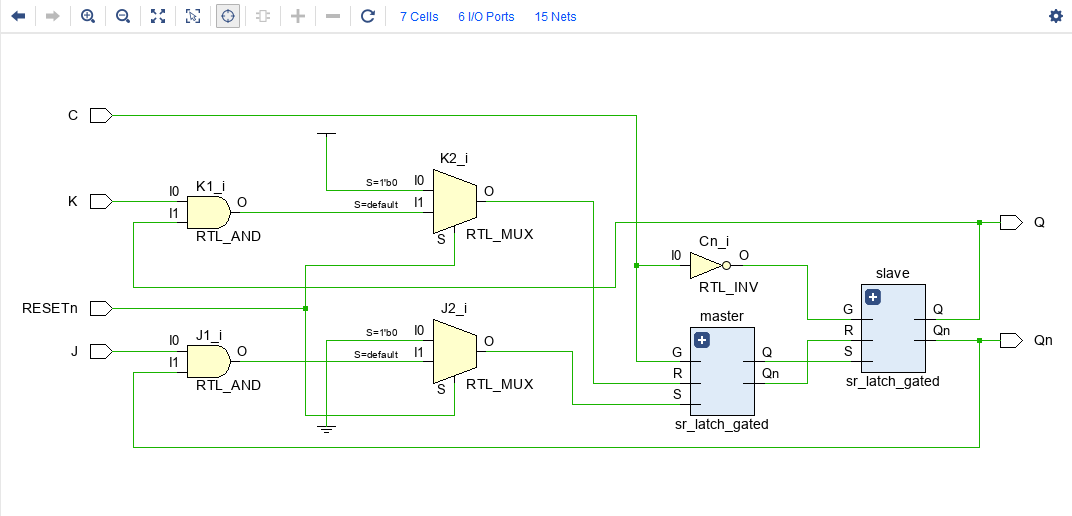
VERILOG CODE:-



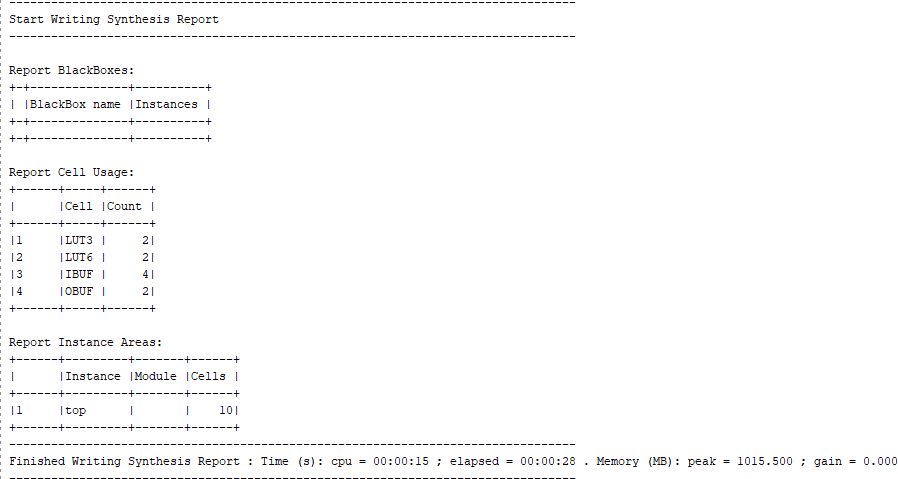


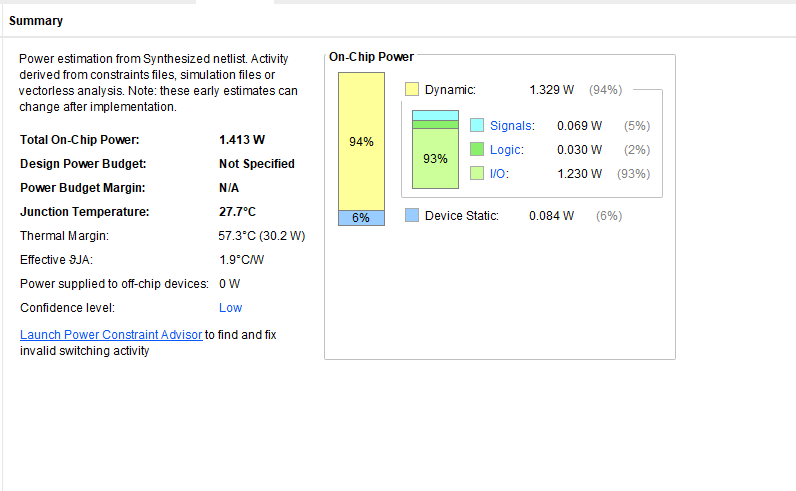




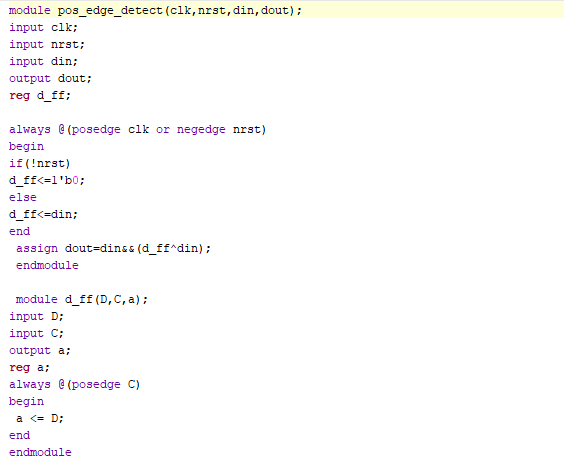


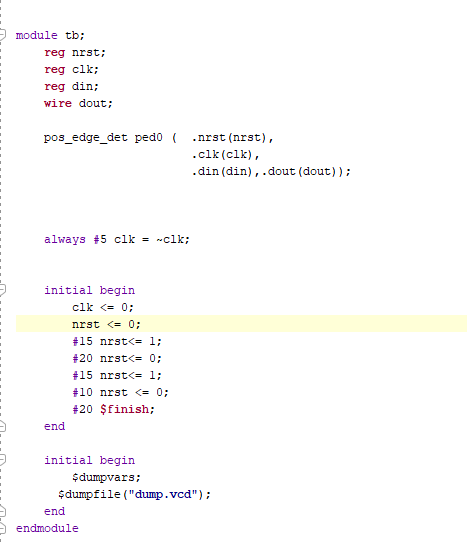
SYNTHESIS REPORT:-

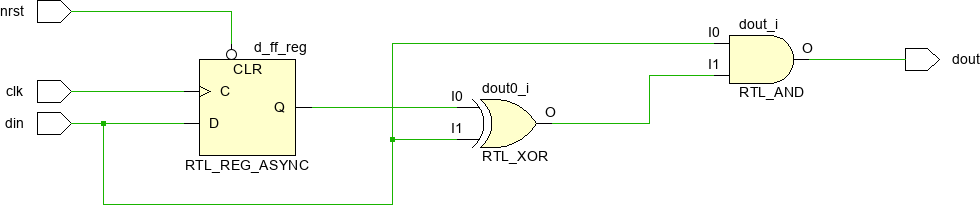




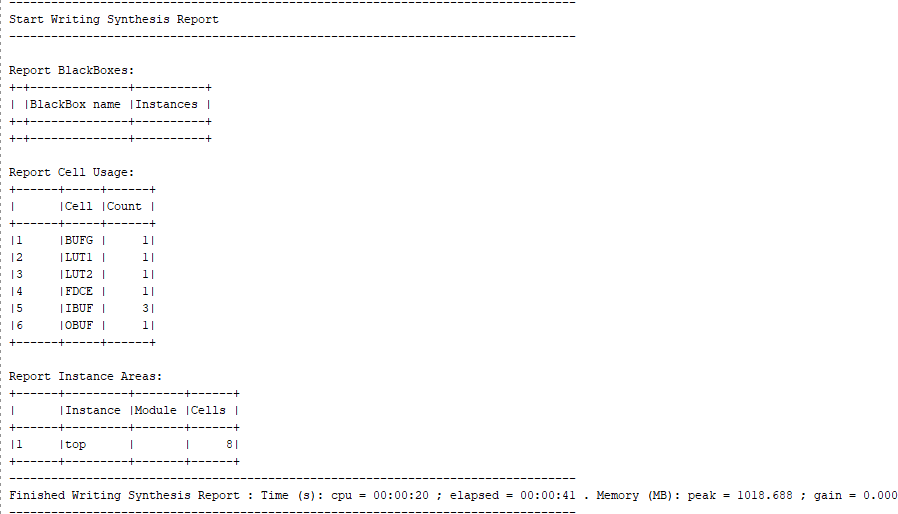
VERILOG CODE:-

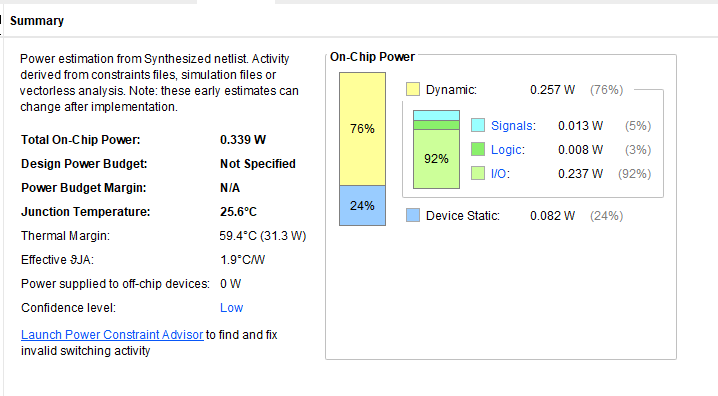




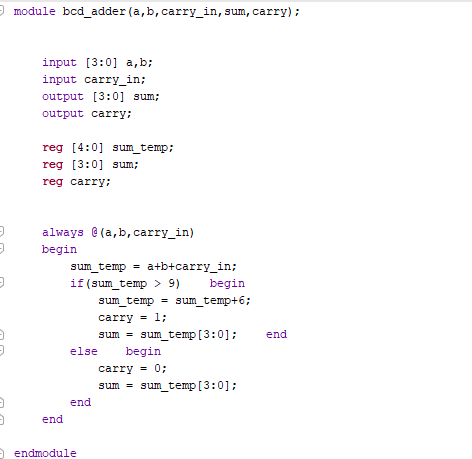


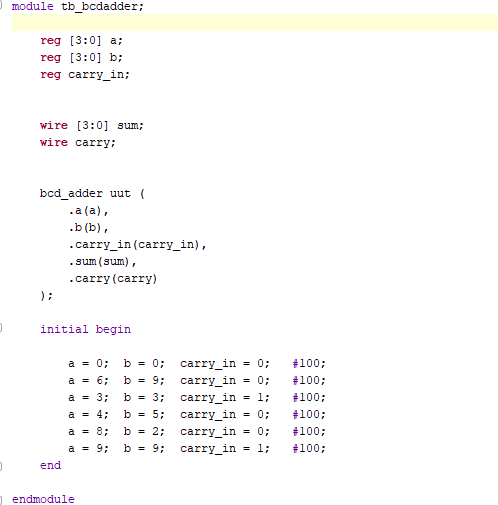
SYNTHESIS REPORT:-



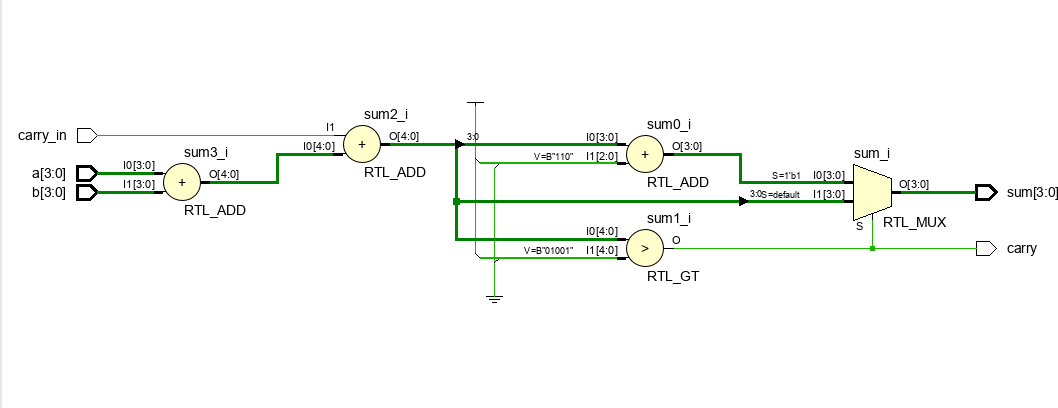


VERILOG CODE:-

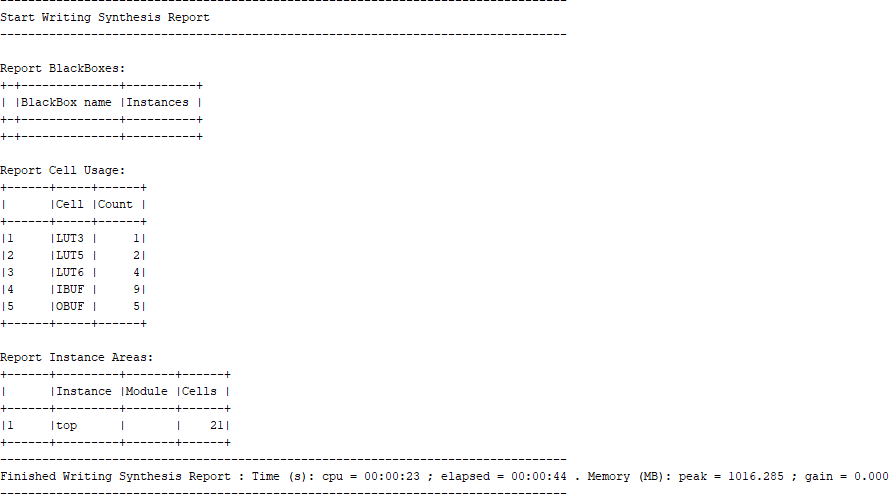




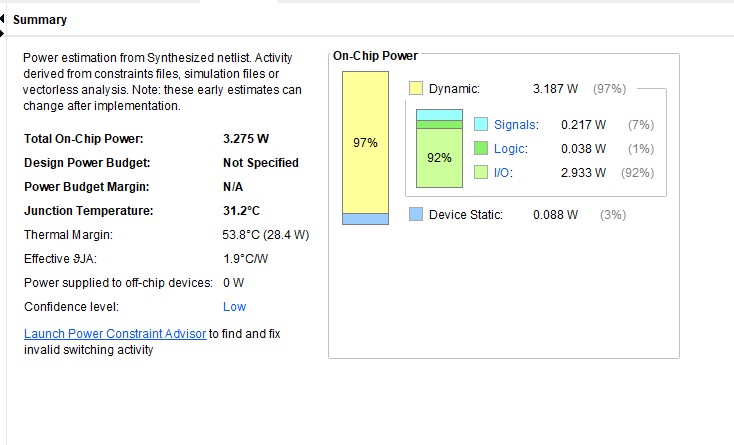
RTL SCHEMATIC:-



# SYNTHESIS REPORT:-

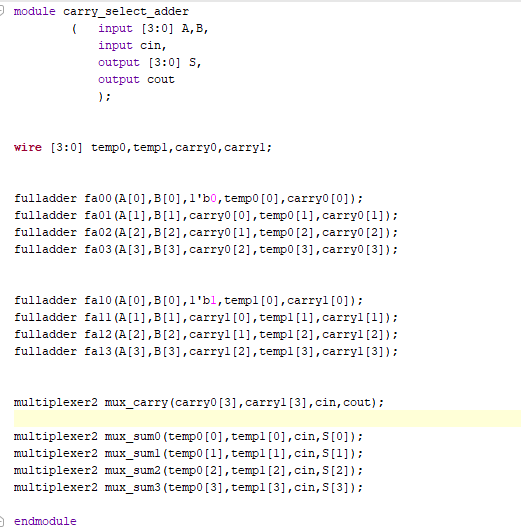


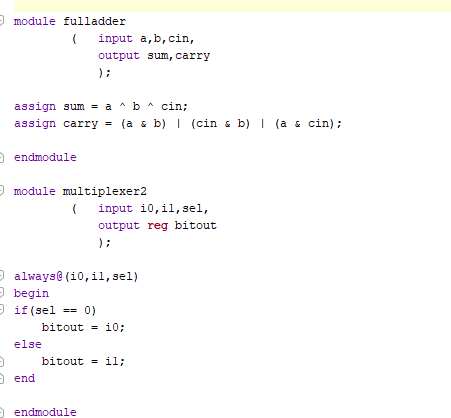
POWER REPORT:-



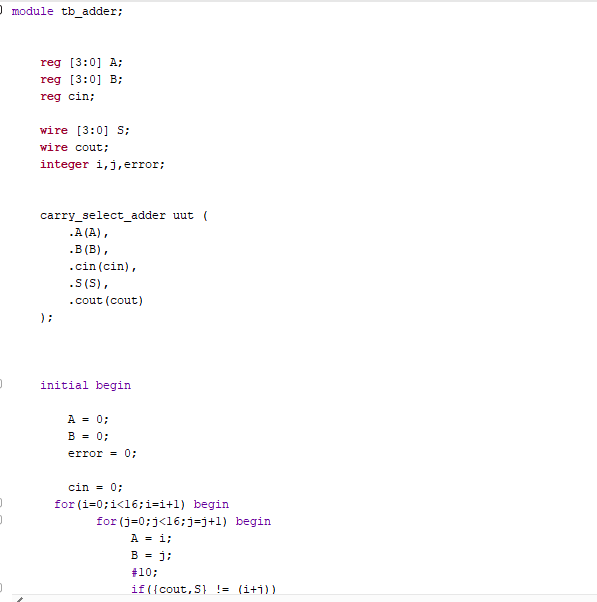
Q23. 4-BIT CARRY SELECT ADDER

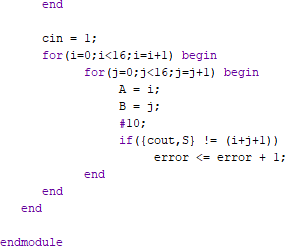
VERILOG CODE:-



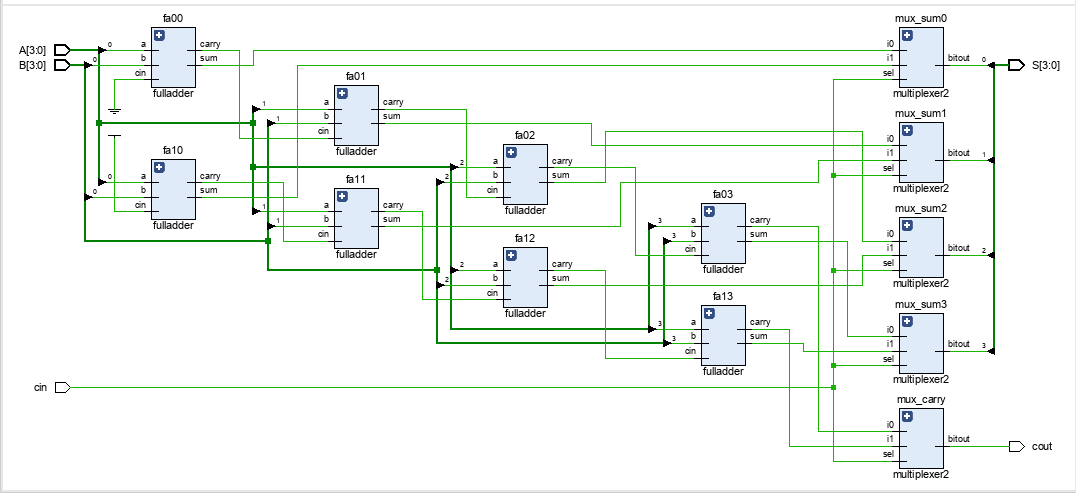


# TEST BENCH:-

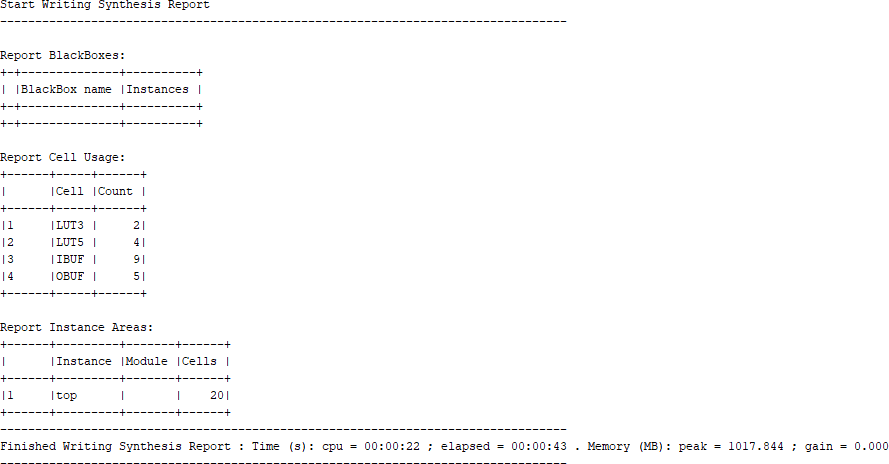




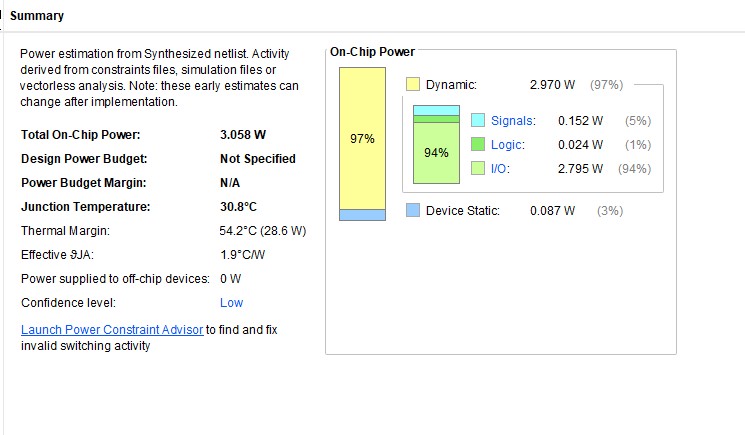
RTL SCHEMATIC:-

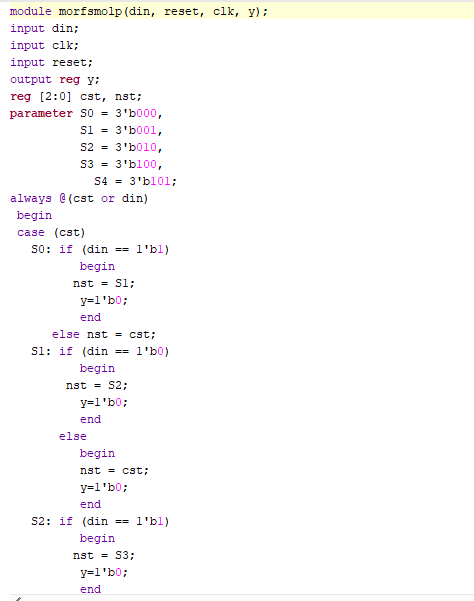


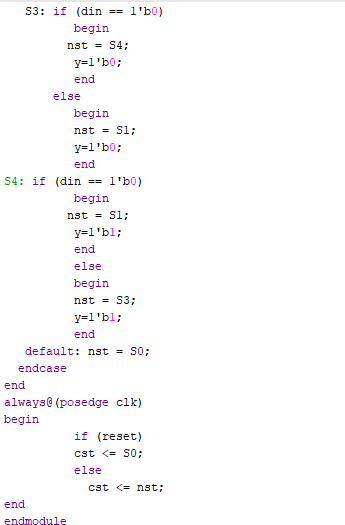
# SYNTHESIS REPORT:-

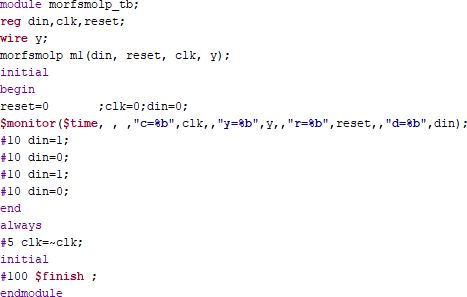


POWER REPORT:-

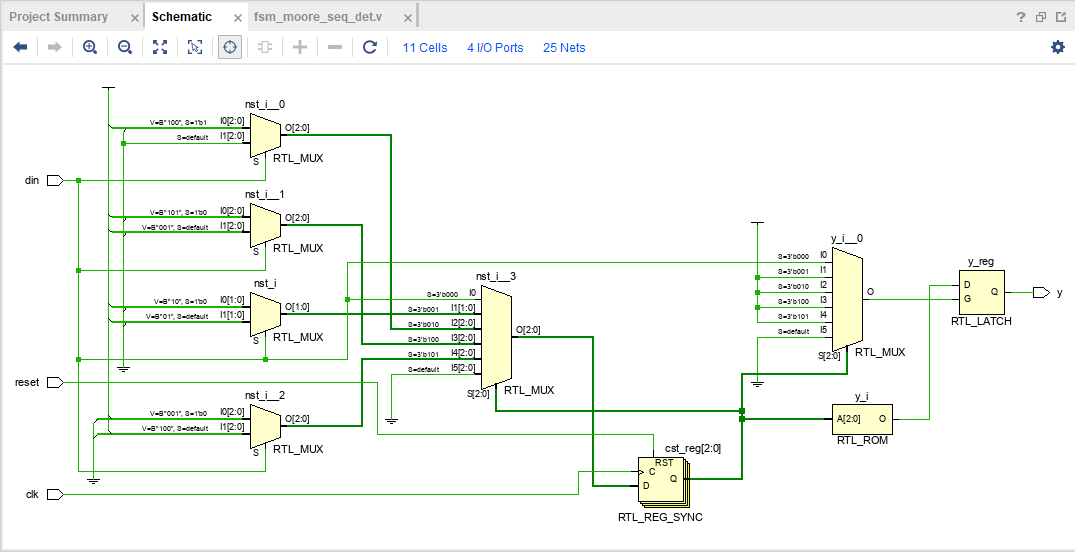


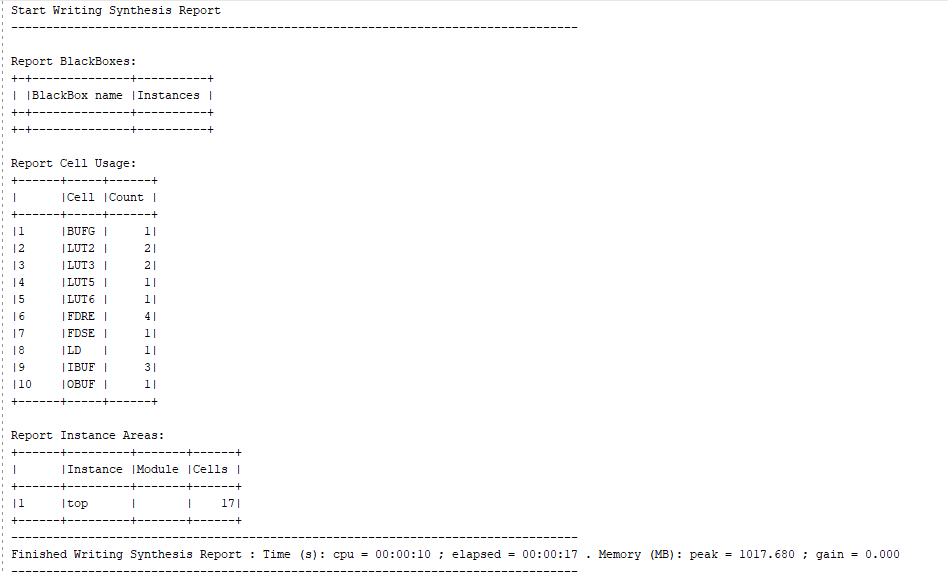
Q24. MOORE FSM 1010 SEQUENCE DETECTOR VERILOG CODE:-



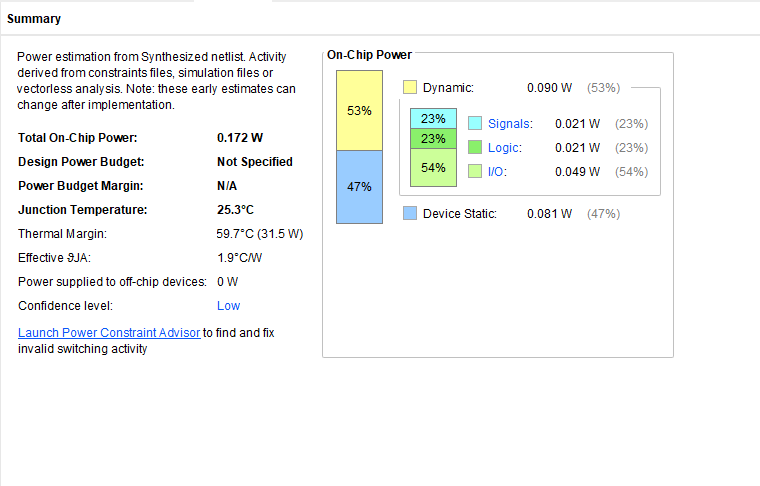


RTL SCHEMATIC:-

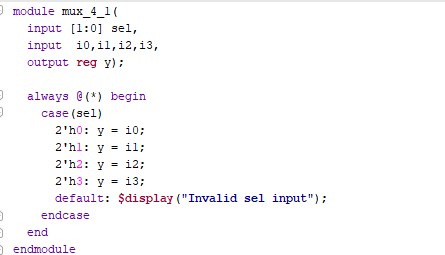




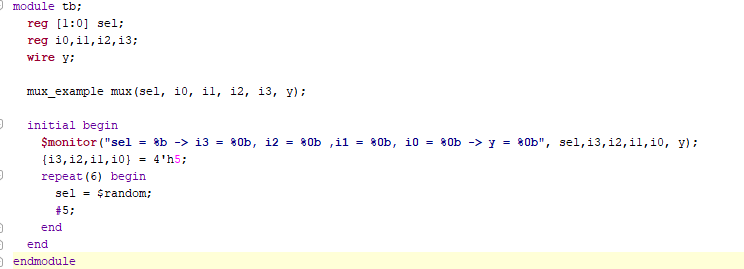
POWER REPORT:-

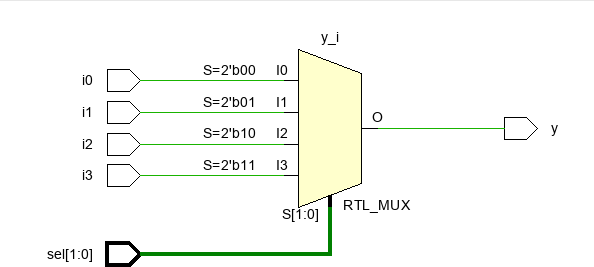


VERILOG CODE:-



TEST BENCH:-





SYNTHESIS REPORT:-

