Jason Tang

(626) 247-0009 | jason.tang@berkeley.edu | linkedin.com/in/jason-tang-berkeley | jaysoar.github.io

Education

University of California, Berkeley GPA: 3.97

Bachelor of Science in Electrical Engineering & Computer Sciences *Expected May 2027*

Relevant Coursework: Tapeout, Digital Design and Integrated Circuits w/ ASIC Lab, Computer Architecture, Operating Systems, Computer Security, Internet Architecture and Protocols, Data Structures

Experience

UC Berkeley Electrical Engineering & Computer Sciences Aug 2025 – Present

EECS 16B Lab TA *Berkeley, CA*

- Support 200+ students with circuit analysis, WaveForms, and LTSpice through office hours and an online forum
- Host weekly lab sections for 40+ students, guiding hands-on circuit construction and use of instrumentation tools
- Help develop weekly prelab and lab assignments, updating and adjusting course content for precision

UC Berkeley Electrical Engineering & Computer Sciences Jan 2026 – Present

EECS 151 Tutor *Berkeley, CA*

- Support ASIC labs by debugging RTL designs in Verilog/SystemVerilog and validating design correctness
- Guided students in analyzing DVE waveforms to verify correctness and diagnose timing-related issues

UC Berkeley Operations and Behavioral Analytics Lab Jan 2025 – May 2025

Undergraduate Research Assistant *Berkeley, CA*

- Conducted research in human-AI interaction to investigate non-compliance with artificial intelligence
- Discussed findings with students and professor in close discussions, resulting in an exploration of new directions for potential research and existing gaps of knowledge

UC Berkeley Engineers and Mentors Aug 2024 – Dec 2024

Primary School Mentor *Berkeley, CA*

- Taught Title 1 elementary students foundational STEM concepts such as human bone anatomy and physics forces (drag, thrust, lift, gravity) through creative demonstrations and hands-on activities
- Designed interactive lesson plans and experiments to engage students and spark early interests in science

Projects

TSMC 16nm IoT SoC Tapeout | *Chisel, Chipyard, Hammer* Jan 2026 – Present

- Contributed to a TSMC 16nm IoT SoC tapeout w/ Apple mentorship, owning a block and driving through signoff

Five Stage Pipelined RISC-V CPU with Caches | *Verilog* Aug 2025 – Dec 2025

- Awarded **1st Place** in the Apple NSI Design Contest for achieving the best performance and area metrics
- Implemented a 5-stage pipeline with hazard detection and data forwarding to increase frequency and reduce stalls
- Designed cache logic with one-cycle read hits, two-cycle write hits, and optimized write-back behavior

Pintos Operating System | *C, x86* Aug 2025 – Dec 2025

- Built and extended core components of an OS to support process control, multithreading, and UNIX FFS
- Implemented multithreading support and synchronization primitives (locks, semaphores, condition variables)
- Utilized GDB extensively to trace low-level kernel execution, inspect memory, and uncover subtle concurrency and synchronization bugs, demonstrating strong debugging and systems-level problem-solving skills

Secure File Sharing System | *Go* Jun 2025 – Aug 2025

- Utilized PBKDFs, symmetric, and public-key cryptography to design a secure file sharing system with user login
- Analyzed RFC security standards to confirm proper protocol usage and compliance with established practices
- Implemented with Go and golang/crypto library and wrote 2000+ lines of code to test said implementation for confidentiality, integrity, and authenticity of information, earning top 5 scoring design in a class of 140

Technical Skills

Languages: Verilog, SystemVerilog, C, x86, RISC-V, Go, Rust, Swift, Java, Python, SQL, JavaScript, HTML/CSS
Developer Tools & Frameworks: DVE, GDB, Docker, Makefile, Valgrind, WaveForms, LTSpice, SwiftUI, UIKit