Jack Ryan Bonfiglio

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EDUCATION

Binghamton University, State University of New York, Watson College of Engineering and Applied Science
Bachelor of Science in Computer Engineering | *Bachelor of Arts in Mathematical Science* *Expected May 2024*
Cumulative GPA: 3.47/4.00

Manhattan College, School of Engineering
Bachelor of Science in Computer Engineering *August 2020 – May 2021*
Cumulative GPA: 3.70/4.00 | **Dean's List**: Fall 2020 - Spring 2021

TECHNICAL SKILLS

Hardware Description: Verilog, VHDL, TCL, Vivado Design Suite, Xilinx Vitis IDE
Programming Languages: C, x86 Assembly, C++, Python, Java, Git, Node.js, YAML

PROJECT EXPERIENCE

Machine Learning Based Autonomous Car
Lead Hardware Developer *September 2023 - Ongoing*
- An autonomous vehicle built on an open-source AI/ML platform and RC car kit capable of speed throttling and object avoidance. Along with that platform, a test environment to train and develop the driving model
- The car uses the Jetson Nano Processor along with an IMU, CSI camera, and PWM servo driver to handle input data
- The Jupyter Notebook environment is used to compute and train models with libraries such as Jetcam, OpenCV, Pytorch, and torch2trt to support those training efforts
- Improvements made to the previous year's project include an upgrade to the Jetson Orin which provides more than three times the computational power vs the Nano. Also, the new inclusion of RPLiDAR A1M8 supports object detection efforts and various SLAM applications

Freestanding Metal Detector
Team Member *March 2023 – May 2023*
- Developed a bare-metal system using Verilog and C to detect, locate, and keep count of metal washers that have interacted with the magnetic field.
- Integrated custom IP modules using Vivado's block design feature to capture the peak voltage of each new digital sample from our Basys 3 PMOD ADC ports. This peak was then stored in a debounced output register for software
- Using Xilinx Vitis, our C program used the memory addresses from Vivado to read output register values to create a 100Hz loop delay to run functions to display the number of objects detected and the strength of the signal

Multi-Cycle ARM Processor
Team Member *November 2022 – December 2022*
- Implemented, with VHDL, the datapath and control unit derived from a high-level state machine for an RISC processor
- Designed to include a RAM unit for register data transfer operations and a custom 32-bit barrel shifter
- Successfully programmed onto the Digilent Bayes 3 FPGA board to perform instruction using various forms of I/O

PROFESSIONAL EXPERIENCE

Research Experience For Undergraduates (REU) **Binghamton, NY**
Undergraduate Researcher *Ongoing*
- Tasked with assisting a team with an autonomously radio-controlled racing car using AI research project
- My specific area of research is in regard to the car's Arduino Nano 33 BLE. I am researching Bluetooth and BLE protocols so that we can expand the Arduino's output buffer size to include additional data such as motor current, steering, and throttling data.
- Direct Memory Access (DMA) will also be implemented to reduce CPU bus monopolization along with limiting the amount of time needed to perform data operations from our Arduino Nano to our cars Jetson Xavier

Northwestern Mutual **Milwaukee, WI**
Software Engineer Intern *June 2023 – August 2023*
- Developed synthetic monitors for the company's in-house Customer Relationship Management platform that sends Slack notifications in the case of a platform outage
- Worked with AWS and EC2 instances refreshing to allow a more streamlined approach to launching and updating your application deployments running on EC2
- Exposed to general scrum methodology and worked closely with scrum masters and the Jira user interface