

Question 1.3: Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor.

a. Answer: We first program in a high-level language such as C. This code is then read by the compiler which converts the program into assembly language (in many cases for MIPS). The assembly code is then read by the assembler which converts the assembly into Binary Machine Language which is comprised of many 1s and 0s.

Question 1.4: Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280×1024 .

a. What is the minimum size in bytes of the frame buffer to store a frame?

i. Answer: Frame Size = $1280 \times 1024 = 1,310,720$ pixels. $1,310,720 \text{ Pixels} \times 3 \text{ bytes/color} = 3,932,160 \text{ bytes}$.

b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

i. Answer: $(3,932,160 \text{ bytes} \times 8 \text{ bits/byte}) / (100 \times 10^6) = 0.3146 \text{ seconds}$

Question 1.5: Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

i. P1: $(3 \times 10^9) / 1.5 = 2 \times 10^9 \text{ IPS}$

ii. P2: $(2.5 \times 10^9) / 1.0 = 2.5 \times 10^9 \text{ IPS}$

iii. P3: $(4.0 \times 10^9) / 2.2 = 1.818 \times 10^9 \text{ IPS}$

iv. Answer: P2 has the highest performance expressed in IPS

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

i. P1 Instructions: $2 \times 10^9 \times 10 = 20 \times 10^9 \text{ Instructions}$

ii. P1 Cycle Number: $20 \times 10^9 \times 1.5 = 30 \times 10^9 \text{ Cycles}$

iii. P2 Instructions: $2.5 \times 10^9 \times 10 = 25 \times 10^9 \text{ Instructions}$

iv. P2 Cycle Number: $25 \times 10^9 \times 1.0 = 25 \times 10^9 \text{ Cycles}$

v. P3 Instructions: $1.818 \times 10^9 \times 10 = 18.18 \times 10^9 \text{ Instructions}$

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vi. $P2 \text{ Cycle Number} = 18.18E9 * 2.2 = 40E9 \text{ Cycles}$

- c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

i. $\text{Execution Time} = \text{Number of Cycles} / \text{Clock Rate}$

ii. $T_{New} = T_0 * (1 - 0.30) = 0.70 * T_0$

iii. $CPI_{New} = CPI_0 * (1 + 0.20) = 1.20 * CPI_0$

iv. $T_{New} = \frac{\text{Number of Inst} * CPI_{New}}{\text{Clock Rate}_{New}}$

v. $0.70 * \frac{\text{Number of Inst} * CPI_0}{\text{Clock Rate}_0} = \frac{\text{Number of Inst} * CPI_{New}}{\text{Clock Rate}_{New}}$

vi. $0.70 * \frac{1}{\text{Clock Rate}_0} = \frac{1.20}{\text{Clock Rate}_{New}} \rightarrow \text{Clock Rate}_{New} = 1.20/0.7 * \text{Clock Rate}_0$

vii. **Answer: Roughly 1.714 Times the Original Clock Rate**

Question 1.6: Consider two different implementations of the same instruction set architecture.

The instructions can be divided into four classes according to their CPI (class A, B, C, and D).

P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

- a. What is the global CPI for each implementation?

i. $P1: \text{Global CPI} = (0.1 * 1) + (0.2 * 2) + (0.5 * 3) + (0.2 * 3) = 2.60$

ii. $P2: \text{Global CPI} = (0.1 * 2) + (0.2 * 2) + (0.5 * 2) + (0.2 * 2) = 2.0$

- b. Find the clock cycles required in both cases.

i. $P1: \text{Clock Cycles} = 2.60 * 1E6 = 2.6E6 \text{ Cycles}$

ii. $P2: \text{Clock Cycles} = 2.00 * 1E6 = 2.0E6 \text{ Cycles}$

- c. Which implementation is faster?

i. $P1: \text{Execution Time} = (2.6E6)/(2.5E9) = 1.04 * 10^{-3} = 1.04 \text{ ms}$

ii. $P2: \text{Execution Time} = (2.0E6)/(3.0E9) = 0.67 * 10^{-3} = 0.67 \text{ ms}$

iii. Answer: P2 is faster

Question 1.7: Compilers can have a profound impact on the performance of an application.

Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

- a. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

i.
$$CPI = \frac{\text{Clock rate} * \text{Execution time}}{\# \text{ of instructions}}$$

ii. Answer:
$$CPI_A = \frac{1\text{GHz} * 1.1}{1 * 10^9} = 1.1$$

iii. Answer:
$$CPI_B = \frac{1\text{GHz} * 1.5}{1.2 * 10^9} = 1.25$$

- b. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

i.
$$CPI = \frac{\text{Clock rate} * \text{Execution time}}{\# \text{ of instructions}}$$

ii.
$$\text{Execution Time} = \frac{CPI * \# \text{ of instructions}}{\text{Clock Rate}}$$

iii. Same Execution time
$$\frac{1.1 * 1 * 10^9}{\text{Clock Rate}_A} = \frac{1.25 * 1.2 * 10^9}{\text{Clock Rate}_B}$$

iv.
$$\frac{\text{Clock Rate}_A}{\text{Clock Rate}_B} \approx 0.733$$

v.
$$\frac{\text{Clock Rate}_B}{\text{Clock Rate}_A} \approx 1.364$$

vi. Answer: Therefore Compiler A is 1.364 times faster than Compiler B

- c. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

i.
$$\text{Execution Time} = \frac{\# \text{ of instructions} * CPI}{\text{Clock Rate}}$$

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$$\text{ii. } Execution\ Time_{New} = \frac{6 \cdot 10^8 \cdot 1.1}{1\ GHz} = 0.66s$$

$$\text{iii. } Execution\ Time_A = \frac{1 \cdot 10^9 \cdot 1.1}{1\ GHz} = 1.1s$$

$$\text{iv. } Execution\ Time_B = \frac{1.2 \cdot 10^9 \cdot 1.5}{1\ GHz} = 1.67s$$

$$\text{v. } \text{Answer: } Speedup_A = \frac{1.1}{0.66} \approx 1.67 \text{ faster}$$

$$\text{vi. } \text{Answer: } Speedup_B = \frac{1.5}{0.66} \approx 2.27 \text{ faster}$$

Question 1.11: The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2.389E12, an execution time of 750 s, and a reference time of 9650 s.

- a. Find the CPI if the clock cycle time is 0.333 ns.

$$CPI = \frac{(execution\ time)}{(instruction\ count) \cdot (clock\ cycle\ time)} = \frac{750}{2.389E12 \cdot 3.33E-10} = 0.94$$

- b. Find the SPECratio.

$$SPECratio = \frac{reference\ time}{execution\ time} = \frac{9650}{750} = 12.9$$

- c. Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% without affecting the CPI.

$$(execution\ time) \cdot 1.1 = 825.0$$

- d. Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% and the CPI is increased by 5%.

$$= \frac{previous}{1.05} = \frac{825}{1.05} = 785.7$$

- e. Find the change in the SPECratio for this change.

$$\frac{9650}{785.7} = 12.3$$

- f. Suppose that we are developing a new version of the AMD Barcelona processor with a 4 GHz clock rate. We have added some additional instructions to the instruction set in such a way that the number of instructions has been reduced by 15%. The execution time is reduced to 700 s and the new SPECratio is 13.7. Find the new CPI.

$$new\ instruction\ count = instruction\ count \cdot 0.85 = 2.03065E12$$

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$$\text{new clock cycle time} = \frac{1}{4 \times 10^9} = 0.250 \text{ ns}$$

$$\text{new CPI} = \frac{(\text{new execution time})}{(\text{new instruction count}) \times (\text{new clock cycle time})} = \frac{700}{2.03065 \times 10^{12} \times 2.5 \times 10^{-10}} = 1.379$$

- g. This CPI value is larger than obtained in 1.11.1 as the clock rate was increased from 3 GHz to 4 GHz. Determine whether the increase in the CPI is similar to that of the clock rate. If they are dissimilar, why?

The CPI increased by ~46% while the clock rate increased by ~33.3%. This dissimilarity can be explained by the decrease in instruction count.

- h. By how much has the CPU time been reduced?

CPU time has been reduced by ~7%

- i. For a second benchmark, libquantum, assume an execution time of 960 ns, CPI of 1.61, and clock rate of 3 GHz. If the execution time is reduced by an additional 10% without affecting to the CPI and with a clock rate of 4 GHz, determine the number of instructions.

$$\text{instructions}(3\text{GHz}) = \frac{960 \times 10^{-9}}{1.61 \times 3.33 \times 10^{-10}} = 1.791 \times 10^{12}$$

$$\text{instructions}(4\text{GHz}) = \text{instructions}(3\text{GHz}) \times \frac{4\text{GHz}}{3\text{GHz}} \times 90\% = 1.791 \times 10^{12} \times 1.33 \times 0.9 = 2.149 \times 10^{12}$$

- j. Determine the clock rate required to give a further 10% reduction in CPU time while maintaining the number of instructions and with the CPI unchanged.

$$\frac{\text{CPI} \times \text{instructions}}{\text{execution time}} = \frac{1.61 \times 2.149 \times 10^{12}}{960 \times 0.9^2} = 4.45 \text{ GHz}$$

- k. Determine the clock rate if the CPI is reduced by 15% and the CPU time by 20% while the number of instructions is unchanged.

$$\frac{\text{CPI} \times \text{instructions}}{\text{execution time}} = \frac{1.61 \times 0.85 \times 2.149 \times 10^{12}}{960 \times 0.9^2 \times 0.8} = 4.73 \text{ GHz}$$

Question 1.12: Section 1.10 cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4 GHz, an average CPI of 0.9, and requires the execution of 5.0×10^9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0×10^9 instructions.

- a. One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for P1 and P2

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i. $Execution\ Time_{P1} = 1.125s$

ii. $Execution\ Time_{P2} = 0.25s$

iii. **Answer:** The statement is false, P2 is faster than P1, due to fewer instructions and CPI

- b. Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of $1.0E9$ instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute at the same time that P1 needs to execute $1.0E9$ instructions.

i. $Execution\ Time_{P1} = \frac{1 \cdot 10^9 \cdot 0.9}{4GHz} = 0.225s$

ii. **Answer:** # of instructions_{P2} = $\frac{0.225s \cdot 3GHz}{0.75} = 9 \cdot 10^8$ instructions

- c. A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.

i. $MIPS = \frac{Clock\ Rate}{CPI \cdot 10^6}$

ii. $MIPS_{P1} = \frac{4GHz}{0.9 \cdot 10^6} \approx 4444.4$

iii. $MIPS_{P2} = \frac{3GHz}{0.75 \cdot 10^6} = 4000$

iv. **Answer:** Although P1 has the better MIPS value, P2 has the better overall performance and efficiency

- d. Another common performance figure is MFLOPS (millions of floating-point operations per second), defined as $MFLOPS = \text{No. FP operations} / (\text{execution time} \times 1E6)$ but this figure has the same problems as MIPS. Assume that 40% of the instructions executed on both P1 and P2 are floating-point instructions. Find the MFLOPS figures for the programs.

i. $MFLOPS = \frac{\# of\ floating\ point\ operations}{Execution\ Time \cdot 10^6}$

ii. For P1, $5 \cdot 10^9 \cdot 0.40 = 2 \cdot 10^9$ floating point operations

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iii. For P2, $1 * 10^9 * 0.40 = 4 * 10^8$ floating point operations

iv. Answer: $MFLOPS_{P1} = \frac{2 * 10^9}{1.125s * 10^6} \approx 1777.78$ MFLOPS

v. Answer: $MFLOPS_{P2} = \frac{4 * 10^9}{0.25s * 10^6} \approx 1600$ MFLOPS