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ECE 4300 Homework 1

1.3 Describe the steps that transform a program written in a high-level language such as C into a representation that a computer processor directly executes.

Compilation: The high-level C code is translated into assembly language by the compiler.
Assembly: The assembly code is converted into machine code (binary instructions) by the assembler.
Execution: After loading, the machine code is executed by the processor.

1.4 Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 x 1024.

a. What is the minimum size in bytes of the frame buffer to store a frame?
3 colors x 8 bits=24 bits (3 bytes)
1280x1024 = 1,310,720 pixels
1,310,720 pixels x 3 bytes/pixel= *3,932,160 bytes is the minimum size of the frame buffer*

b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?

Memory Size of the Frame (in bits) = 3, 932, 160 x 8 = 31,457,280 bits
Time = (Total bits) / (Network speed)

$31,457,280\ bits\ /10^{8}\ bits/second = 0.315\ secs$

1.5 Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2

a. Which processor has the highest performance expressed in instructions per second?
Instructions per second = (Clock Rate)/(CPI)

$P1 = \frac{3\ GHz}{1.5} = 2 \times 10^{9}$ IPS

$P2 = \frac{2.5\ GHz}{1} = 2.5 \times 10^{9}$ IPS

$P3 = \frac{4\ GHz}{2.2} = 1.82 \times 10^{9}$ IPS

P2 has the highest performance

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Clock Cycles = CPU time × Clock Rate
Instructions = IPS × CPU Time

$P1\ clock\ cycles = 10 \times 3\ GHz = 10 \times 3 \times 10^9 = 3 \times 10^{10}$

$P1\ instructions = 2 \times 10^9 \times 10 = 2 \times 10^{10}$

$P2\ clock\ cycles = 10 \times 2.5\ GHz = 10 \times 2.5 \times 10^9 = 2.5 \times 10^{10}$

$P2\ instructions = 2.5 \times 10^9 \times 10 = 2.5 \times 10^{10}$

$P3\ clock\ cycles = 10 \times 4\ GHz = 10 \times 4 \times 10^9 = 4 \times 10^{10}$

$P3\ instructions = 1.82 \times 10^9 \times 10 = 1.82 \times 10^{10}$

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

$Execution\ Time_{new} = 0.7\ Execution\ Time_i$

$\frac{instructions_{new} \times CPI_{new}}{clock\ rate_{new}} = 0.7 \times \frac{CPI_{old}}{clock\ rate_i}$ where $CPI_{new} = 1.2\ CPI_{old}$

$\frac{1.2}{clock\ rate_{new}} = \frac{0.7}{clock\ rate_i}$

$clock\ rate_{new} = \frac{1.2}{0.7} \times clock\ rate_i = 1.71 \times clock\ rate_i$

1.71 times faster

1.6 [5] Consider the table given next, which tracks several performance indicators for Intel desktop processors since 2010.
The "Tech" column shows the minimum feature size of each processor's fabrication process. Assume that the die size has remained relatively constant and the number of transistors that comprise each processor scales at $(1/t)^2$, where t = the minimum feature size.
For each performance indicator, calculate the average rate of improvement from 2010 to 2019, as well as the number of years required to double each at that corresponding rate.

Desktop processor	Year	Tech	Max. clock speed (GHz)	Integer IPC/core	Cores	Max. DRAM Bandwidth (GB/s)	SP floating point (Gflop/s)	L3 cache (MiB)
Westmere i7-620	2010	32	3.33	4	2	17.1	107	4
Ivy Bridge i7-3770K	2013	22	3.90	6	4	25.6	250	8
Broadwell i7-6700K	2015	14	4.20	8	4	34.1	269	8
Kaby Lake i7-7700K	2017	14	4.50	8	4	38.4	288	8
Coffee Lake i7-9700K	2019	14	4.90	8	8	42.7	627	12
Imp./year		__%	__%	__%	__%	__%	__%	__%
Doubles every		__years	__years	__years	__years	__years	__years	__years

Improvement per year=((New value)/(Old value)) $^{(1/(Number\ of\ years)}$) -1
Doubling time (in years)= log(2)/log(1+Improvement per year)

Final Results:

Metric	Improvement per year	Doubling time (years)
Max. Clock Speed	4.35%	16.44
Integer IPC/Core	8.08%	8.96
Cores	15.44%	4.62
Max. DRAM Bandwidth	10.69%	7.13

SP Floating Point	19.65%	3.82
L3 Cache	12.92%	5.51

1.7 Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?

CPU Clock Cycles = $\sum_{i=1}^{n}$ (CPIi)Ci

Class A: 10^6 x 10% = 10^5 instructions
Class B: 10^6 x 20% = 2x10^5 instructions
Class C: 10^6 x 50% = 5x10^5 instructions
Class D: 10^6 x 20% = 2x10^5 instructions

$$CPU\ clock\ cycles_{p1} = (1 \times 10^5) + (2 \times 2 \times 10^5) + (3 \times 5 \times 10^5) + (3 \times 2 \times 10^5) = 2.6 \times 10^6$$

$$CPU\ clock\ cycles_{p2} = (2 \times 10^5) + (2 \times 2 \times 10^5) + (2 \times 5 \times 10^5) + (2 \times 2 \times 10^5) = 2 \times 10^6$$

$$CPI_{p1} = \frac{CPU\ clock\ cycles_{p1}}{Number\ of\ instructions} = \frac{2.6 \times 10^6}{10^6} = 2.6$$

$$CPI_{p2} = \frac{CPU\ clock\ cycles_{p2}}{Number\ of\ instructions} = \frac{2 \times 10^6}{10^6} = 2$$

b. Find the clock cycles required in both cases.
Clock Cycles=Total Instructions×Global CPI
Clock CyclesP1=1,000,000instructions×2.6=*2,600,000cycles*
Clock CyclesP2=1,000,000 instructions×2.0=*2,000,000 cycles*

1.11 Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm2.

a. Find the yield for both wafers.
   Y (15cm)= 1/((1+0.02x2.1)^3)=1/13=*0.884*
   Y(20cm)=1/((1+0.031x3.14)^3)=1/1.295=*0.772*
b. Find the cost per die for both wafers.

Cost/die (15cm)= 12/(84x0.884)=*0.162*
Cost/die (20cm)= 15/(100x0.772)=*0.194*

c. If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.
15 cm:
New Number of Dies=84×1.10=92.4≈92dies
New Defects=0.020×1.15=0.023defects/cm^2
New area per die=176.71cm^2/92≈1.92cm^2
Yield=e^(−0.023×1.92)=e^(−0.04416)≈*0.957*

20 cm:
New Number of Dies=100×1.10=110dies
New Defects=0.031×1.15≈0.03565defects/cm^2
New area per die=314.16cm^2/110≈2.86cm^2
Yield=e^(−0.03565×2.86)=e^(−0.1011)≈*0.904*

d. Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm2.

0.92:
defects/cm^2=((1-0.92)^(⅓))/2=*0.0175 defects/cm^2*
0.95:
defects/cm^2=((1-0.95)^(⅓))/2=*0.0085 defects/cm^2*

1.12 The results of the SPEC CPU2006 bzip2 benchmark running on an AMD Barcelona has an instruction count of 2.389E12, an execution time of 750 s, and a reference time of 9650 s.

a. Find the CPI if the clock cycle time is 0.333 ns.
Clock Rate=1/Clock Cycle Time=1/0.333ns=1/(0.333×10−9s)≈3.00GHz
Total Cycles=3.00×10^9 cycles/s×750s=2.25×10^12 cycles
CPI=Total Cycles /Instruction Count
CPI=2.25×10^12cycles/2.389×10^12instructions≈*0.943*

b. Find the SPECratio.
SPEC ratio=9650s/750s≈*12.87*

c. Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% without affecting the CPI.
New Instruction Count=I×1.10=2.389×10^12×1.10≈2.628×10^12
New execution time=(New instruction count x CPI)/Clock rate= (2.6279x10^12 x 0.942)/(3.003x10^9)=824.42 secs
Increase by 74.42 secs

d. Find the increase in CPU time if the number of instructions of the benchmark is increased by 10% and the CPI is increased by 5%.
New CPI=CPI×1.05=0.943×1.05≈0.99015
New execution time= (2.6279x10^12 x 0.9891)/ (3.003x10^9)=864.75secs
Increased by 114.75 secs

e. Find the change in the SPECratio for this change.
New SPEC ratio=9650s/864.75≈11.16
Change in SPEC ratio=12.87−11.16≈*1.71*

f. Suppose that we are developing a new version of the AMD Barcelona processor with a 4 GHz clock rate. We have added some additional instructions to the instruction set in such a way that the number of instructions has been reduced by 15%. The execution time is reduced to 700 s and the new SPECratio is 13.7. Find the new CPI.
SPEC ratio=9650s/700s≈13.79
New Instruction Count=I×(1−0.15)=2.389×10^12×0.85≈2.03065×10^12
Clock Cycle Time=1/Clock Rate=1/(4×10^9)=0.25ns=0.25×10^−9s
CPI=700s/((2.03065×1012)×(0.25×10−9))=*1.376*

g. This CPI value is larger than obtained in 1.11.1 as the clock rate was increased from 3 GHz to 4 GHz. Determine whether the increase in the CPI is similar to that of the clock rate. If they are dissimilar, why?
Increase in CPI=1.376−0.943≈0.433
Percentage Increase in CPI=0.433./0.943×100%≈45.98%
Increase in Clock Rate=4GHz−3GHz=1GHz
Percentage Increase in Clock Rate=1GHz/3GHz×100%≈33.33%
The increase in CPI is greater than the increase in clock rate. The increase in CPI is dissimilar to the increase in clock rate due to changes in the instruction set and microarchitectural factors, leading to a more significant increase in the CPI relative to the increase in clock speed.

h. By how much has the CPU time been reduced?
Original CPU Time=2.389×10^12×0.943×(0.333×10^−9)≈743.07s
New CPU Time≈2.03065×1012×1.376×0.25×10−9≈700s
Reduction in CPU Time=743.07s−700s≈43.07s

i. For a second benchmark, libquantum, assume an execution time of 960 ns, CPI of 1.61, and clock rate of 3 GHz. If the execution time is reduced by an additional 10% without affecting to the CPI and with a clock rate of 4 GHz, determine the number of instructions.

Instruction count = (execution time x clock rate)/CPI = (960x10^-9 x 3x10^9)/1.61= *1788 instructions*

j. Determine the clock rate required to give a further 10% reduction in CPU time while maintaining the number of instructions and with the CPI unchanged.
New Execution Time=960ns×(1−0.10)=960ns×0.90=864ns
Clock Cycle Time=1788×1.61/864×10^−9s= *3.33 GHz*

k. Determine the clock rate if the CPI is reduced by 15% and the CPU time by 20% while the number of instructions is unchanged.
New CPI (15%)= 1.61 x 0.85 = 1.3685s
New CPI (20%)=960 x 0.8 = 768ns
Clock rate = (1788 x 1.3685)/(768x10^-9)=3