DATA SHEET

NVIDIA Jetson Xavier NX System-on-Module

Volta GPU + Carmel CPU + 8 GB LPDDR4x + 16 GB eMMC 5.1

AI Performance

Up to 21 TOPS (INT8)

Volta GPU

384 NVIDIA® CUDA® cores | 48 Tensor cores | End-to-end lossless compression | Tile Caching | OpenGL® 4.6 | OpenGL ES 3.2 | Vulkan™ 1.1◊ | CUDA 10 | Maximum Operating Frequency: 1100 MHz

Carmel CPU

ARMv8.2 (64-bit) heterogeneous multi-processing (HMP) CPU architecture | 3x dual-core CPU clusters (six NVIDIA Carmel processor cores) connected by a high-performance system coherency interconnect fabric | L3 Cache: 4 MB (shared across all clusters)

NVIDIA Carmel (Dual-Core) Processor: L1 Cache: 128 KB L1 instruction cache (I-cache) per core; 64 KB L1 data cache (D-cache) per core | L2 Unified Cache: 2 MB per cluster | Maximum Operating Frequency: 1900 MHz

Audio

Dedicated programmable audio processor | ARM Cortex A9 with NEON | PDM in/out | Industry-standard High-Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI® interface

Memory

8 GB 128-bit LPDDR4x DRAM | Secure External Memory Access Using TrustZone® Technology | System MMU | Maximum Operating Frequency: 1866 MHz

Storage

16 GB eMMC 5.1 Flash Storage | Bus Width: 8-bit | Maximum Bus Frequency: 200 MHz (HS400)

Networking

10/100/1000 Gigabit Ethernet | Media Access Controller (MAC)

Imaging

14 lanes (3 x4 or 6 x2) MIPI CSI-2 | D-PHY 1.2 (2.5 Gb/s per pair, total up to 30 Gbps)

Display Controller

Two multi-mode (eDP/DP/HDMI) Serial Output Resources (SOR) eDP 1.4a | DP 1.4 | HDMI 2.0a/b

Maximum Resolution (eDP/DP/HDMI): (up to) 3840x2160 at 60 Hz (up to 36 bpp)

Multi-Stream HD Video and JPEG

Video Decode:

- Standards supported: H.265, H.264, VP9, VP8, MPEG-4, MPEG-2, VC-1
  - 2x 1300 MP/sec (H.265)
  - 2x 8K30 (H.265)
  - 6x 4K60 (H.265)
  - 12x 4K30 (H.265)
  - 22x 1080p @ 60 (H.265)
  - 44x 1080p @ 30 (H.265)
  - 22x 1080p @ 30 (H.264)

Video Encode:

- Standards supported: H.265, H.264, VP9
  - 2x 700 MP/sec (H.265)
  - 2x 4K60 (H.265)
  - 4x 4K30 (H.265)
  - 10x 1080p @ 60 (H.265)
  - 22x 1080p @ 30 (H.265)

Peripheral Interfaces

xHCI host controller with integrated PHY (up to) 1x USB 3.1, 3x USB 2.0 | PCIe 1x1 (GEN3) + 1x4 (GEN4) | SD/MMC controller (supporting eMMC 5.1, SD 4.0, SDHOST 4.0 and SDIO 3.0) | 3x UART | 2x SPI | 4x I^2C | 1x CAN | 2x I^2S | GPIOs

Mechanical

Module Size: 69.6 mm x 45 mm | 260 pin SO-DIMM Connector

Operating Requirements

Temperature Range (T_J)*: -25°C – 90°C | Supported Power Modes: 10W |15W | 20W | Power Input: 5V

Note: Refer to the Software Features section of the latest L4T Development Guide for a list of supported features; all features may not be available.

◊ Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.

* See the *Jetson Xavier NX Thermal Design Guide* for details

Revision History

Version	Date	Description
V1.0	November 6, 2019	Initial release.
V1.1	February 1, 2020	Updated: • PCIE0_XXX pins from Ctrl #0 to Ctrl #5 under PCIe Pin description in Table 9: PCIe Pin Descriptions • PCIE1_XXX pins from Ctrl #1 to Ctrl #4 under PCIe Pin description in Table 9: PCIe Pin Descriptions • Pulse Width Modulator (PWM) to reflect four outputs instead of eight outputs • SHUTDOWN_REQ* and SYS_RESET* pull up information in Table 21: Power and System Control Pins • Table 29: Absolute Maximum Ratings to include the Mounting Force parameter. • Mechanical Drawing
V1.2	February 24, 2020	Added: • Tolerance information for Mechanical Drawing
V1.3	April 21, 2020	Added: • PMIC_BBAT to reflect RTC accuracy • SoC height for the Mechanical Drawing • Table 30: Jetson NX Reliability Report table • Gen4 information to PCI Express (PCIe) section
V1.4	June 25, 2020	Added: • Programmable Vision Accelerator (PVA) section to Functional Overview Updated: • Table 6: Video Decoder Standards table
V1.5	July 06, 2020	Added: • Overcurrent Throttling section to Power and System Management
V1.6	October 23, 2020	Updated: • SHUTDOWN_REQ* pin changed from Input to Output • Document number of data sheet Added: • SPI Slave Timing Parameters and Diagram
V1.7	July 29, 2021	Updated: • Video Decoder Standards Table • Video Encoder Standards Table • 20W information for GPU Operation, CPU Operation, DLA Clock, and PVA clock tables • Maximum DRAM frequency from 1600 to 1866

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1.0 Functional Overview

NVIDIA® Jetson Xavier™ NX brings AI supercomputer performance to the edge in a compact system-on-module (SOM) which is smaller than a credit card. Jetson Xavier NX is built around a low-power version of the NVIDIA Xavier SoC, combining the NVIDIA Volta™ GPU architecture with 64-bit operating capability, integrated advanced multi-function video and image processing, and NVIDIA Deep Learning Accelerators.

Compute performance up to 21 TOPs (at 15W and 20W) enables the Jetson Xavier NX to run multiple neural networks in parallel and process data from multiple high-resolution sensors simultaneously. It also offers a unique combination of performance and power advantages with a rich set of I/Os, from high-speed CSI and PCIe to low-speed I^2Cs and GPIOs, allowing embedded and edge computing devices that demand increased performance but are constrained by size, weight, and power budgets.

1.1 Volta GPU

The Graphics Processing Cluster (GPC) is a dedicated hardware block for computing, rasterization, shading, and texturing of most of the GPU's core graphics functions. The GPC is comprised of Texture Processing Clusters (TPC), with each TPC containing two Streaming Multiprocessor (SM) units, and a Raster Engine. The SM unit creates, manages, schedules, and executes instructions from many threads in parallel. Raster operators (ROPs) continue to be aligned with L2 cache slices and memory controllers. The SM geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces, while the efficiency of the Volta GPU enables this performance on devices with power-limited environments.

Each SM is partitioned into four separate processing blocks (referred to as SMPs), each SMP contains its own instruction buffer, scheduler, CUDA cores, and Tensor cores. Inside each SMP, CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations, and each Tensor core provides a 4x4x4 matrix processing array to perform mixed-precision fused multiply-add (FMA) mathematical operations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output.

Features:

- End-to-end lossless compression
- Tile Caching
- Support for OpenGL 4.6, OpenGL ES 3.2, Vulkan 1.1
- Adaptive Scalable Texture Compression (ASTC) LDR profile supported
- CUDA support
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power of 2D and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

Table 1: GPU Operation

Module	CUDA Cores	Tensor Cores	Power Mode	Operating Frequency per Core (up to)
Jetson Xavier NX	384	48	10W	800 MHz
			15W	1100 MHz

Module	CUDA Cores	Tensor Cores	Power Mode	Operating Frequency per Core (up to)
			20W	1100 MHz

1.2 Carmel CPU Complex

The CPU complex (CCPLEX) is comprised of three Carmel dual-core CPU clusters in a coherent multi-processor configuration. A high-performance System Coherency Fabric (SCF) connects all CPU clusters enabling simultaneous operation of all CPU cores (as needed) for a true heterogeneous multi-processing (HMP) environment.

Features include:

- NVIDIA Dynamic Code Optimization
- 10-wide Superscalar architecture
- Dynamic branch prediction with a Branch Target Buffer and Global History Buffer RAMs, a return stack buffer, and an indirect predictor
- Full implementation of ARMv8.2 ISA compliant architecture including:
  - ARMv8 TrustZone
  - ARMv8.0 Crypto ISA
  - Trusted Memory
  - ARMv8.2-FP16 support
- 128 KB 4-way-associative parity protected L1 instruction cache per core
- 64 KB 4-way-associative parity protected L1 data cache per core
- 2 MB 16-way-associative ECC protected L2 cache per CPU cluster
- 4 MB 16-way-associative ECC protected L3 cache (shared across all clusters)
- Performance Monitoring
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains

Table 2: CPU Operation

Module	Power Mode	CPU Cores	CPU Maximum Frequency
Jetson Xavier NX	10W	2-core	1.5 GHz
		4-core	1.2 GHz
	15W	2-core	1.9 GHz
		4/6-core	1.4 GHz
	20W	2-core	1.9 GHz
		4/6-core	1.4 GHz

1.3 Memory Subsystem

The Memory Subsystem (MSS) provides access to local DRAM, SysRAM, and provides a SyncPoint Interface for inter-processor signaling. The MSS supports full-speed I/O coherence by routing requests through a scalable coherence fabric. It also supports a comprehensive set of safety and security mechanisms.

Structurally, the MSS consists of:

1. MSS Data Backbone - routes requests from clients to the MSS Hub and responses from MSS Hub to the clients.
2. MSS Hub - receives and arbitrates among client requests, performs SMMU translation, and sends requests to MCF.
3. Memory Controller Fabric (MCF) - performs security checks, feeds I/O coherent requests to the Scalable Coherence Fabric (SCF), and directs requests to the multiple memory channels.
4. Memory Controller (MC) Channels - row sorter/arbiter and DRAM controllers.
5. DRAM I/O - channel-to-pad fabric, DRAM I/O pads, and PLLs.

Jetson Xavier NX integrates a 128-bit wide LPDDR4x memory interface implemented as four 32-bit channels with x16 sub-partitions. The memory controller provides a single read or write command, plus a row address to both sub-partitions in the channel to transfer 64 bytes. It also provides three independent column address bits to each sub-partition, allowing it access different 32-byte sectors of a GOB between the sub-partitions. It provides connections between a wide variety of clients, supporting their bandwidth, latency, quality-of-service needs, and any special ordering requirements that are needed. The MSS supports a variety of security and safety features and address translation for clients that use virtual addresses.

Features:

- LPDDR4x: x32 DRAM chips
- 128-bit wide data bus
- Low latency path and fast read/response path support for the CPU complex cluster
- Support for low-power modes:
  - Software controllable entry/exit from self-refresh, power down, and deep power down
  - Hardware dynamic entry/exit from power down, self-refresh
  - Pads use DPD mode during idle periods
- High-bandwidth interface to the integrated Volta GPU
- Full-speed I/O coherence with bypass for Isochronous (ISO) traffic
- System Memory-Management Unit (SMMU) for address translation based on the ARM SMMU-500
- High-bandwidth PCIe ordered writes
- AES-XTS encryption with 128-bit key

1.4 Memory

The Jetson Xavier NX integrates 8 GB 128-bit LPDDR4x DRAM. Maximum frequency of 1866 MHz has a theoretical peak memory bandwidth of 59.7 GB/s.

The Memory Controller (MC) maximizes memory utilization while providing minimum latency access for critical CPU requests. An arbiter is used to prioritize requests, optimizing memory access efficiency and utilization and minimizing system power consumption. The MC provides access to main memory for all internal devices. It provides an abstract view of memory to its clients via standardized interfaces, allowing the clients to ignore details of the memory hierarchy. It optimizes access to shared memory resources, balancing latency and efficiency to provide best system performance, based on programmable parameters.

Features:

- TrustZone (TZ) Secure and OS-protection regions
- System Memory Management Unit
- Dual CKE signals for dynamic power down per device
- Dynamic Entry/Exit from Self-Refresh and Power Down states

1.5 Video Input Interfaces

1.5.1 MIPI Camera Serial Interface (CSI)

Standard
MIPI CSI 2.0 Receiver specification
MIPI D-PHY® v1.2 Physical Layer specification

The NVIDIA Camera Serial Interface (NVCSI) works with the Video Input (VI) unit to capture an image from a sensor, where NVCSI is a source of pixel data to VI. NVCSI works in streaming mode while VI captures the required frames using a single-shot mode of operation. All sync point generation for software is handled at VI; the delay between NVCSI and VI is negligible in software terms. NVCSI does not have a direct memory port, instead it sends the pixel data to memory through the VI.

Fifth-generation NVIDIA camera solution (NVCSI 2.0, VI 5.0, and ISP 5.0) provides a combination host that supports enhanced MIPI D-PHY (with lane deskew support) physical layer options in three 4-lane or six 2-lane configurations; or combinations of these. Each lane can support up to 16 virtual channels (VC) and supports data type interleaving.

- Virtual Channel Interleaving: VCs are defined in the CSI-2 specification and are useful when supporting multiple camera sensors. With the VC capability, a one-pixel parser (PP) can de-interleave up to 16 image streams.
- Data Type Interleaving: In HDR line-by-line mode, the sensor can output long/short exposure lines using the same VC and a different programmable data type (DT).
- Frequency Target: The parallel pixel processing rate, measured in pixels-per-clock (PPC), is increased to allow higher throughput and lower clock speeds. To support higher bandwidth without increasing the operating frequency, the host processes multiple pixels in one clock. NVCSI is capable of processing four PPCs when bits-per-pixel (BPP) is greater than 16, and eight PPC when BPP is less than or equal to 16.
- With the new streaming mode in NVCSI, one PP can handle all traffic (embedded data and image data) from one camera device, including 16 VCs.

Features:

- Supports the MIPI D-PHY v1.2 physical layer option:
  - MIPI D-PHY supports up to 2.5 Gbits/sec per pair, for an aggregate bandwidth of 30 Gbps from 12 pairs
- Based on MIPI CSI-2 v2.0 protocol stack
- Includes six-pixel parsers (PP)
- Supports up to 16 virtual channels per active PP
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20
  - DPCM (predictor 1): 14-10-14, 14-8-14, 12-8-12, 12-7-12, 12-6-12, 12-10-12, 10-8-10, 10-7-10, 10-6-10 (Predictor 2 not supported)
- Data type interleave support

Table 3: CSI Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
10	CSI0_CLK_N	Camera, CSI 0 Clock–	Input	MIPI D-PHY
12	CSI0_CLK_P	Camera, CSI 0 Clock+	Input	MIPI D-PHY
4	CSI0_D0_N	Camera, CSI 0 Data 0–	Input	MIPI D-PHY
6	CSI0_D0_P	Camera, CSI 0 Data 0+	Input	MIPI D-PHY
16	CSI0_D1_N	Camera, CSI 0 Data 1–	Input	MIPI D-PHY
18	CSI0_D1_P	Camera, CSI 0 Data 1+	Input	MIPI D-PHY
9	CSI1_CLK_N	Camera, CSI 1 Clock–	Input	MIPI D-PHY
11	CSI1_CLK_P	Camera, CSI 1 Clock+	Input	MIPI D-PHY
3	CSI1_D0_N	Camera, CSI 1 Data 0–	Input	MIPI D-PHY
5	CSI1_D0_P	Camera, CSI 1 Data 0+	Input	MIPI D-PHY
15	CSI1_D1_N	Camera, CSI 1 Data 1–	Input	MIPI D-PHY
17	CSI1_D1_P	Camera, CSI 1 Data 1+	Input	MIPI D-PHY
28	CSI2_CLK_N	Camera, CSI 2 Clock–	Input	MIPI D-PHY
30	CSI2_CLK_P	Camera, CSI 2 Clock+	Input	MIPI D-PHY
22	CSI2_D0_N	Camera, CSI 2 Data 0–	Input	MIPI D-PHY

Pin #	Signal Name	Description	Direction	Pin Type
24	CSI2_D0_P	Camera, CSI 2 Data 0+	Input	MIPI D-PHY
34	CSI2_D1_N	Camera, CSI 2 Data 1–	Input	MIPI D-PHY
36	CSI2_D1_P	Camera, CSI 2 Data 1+	Input	MIPI D-PHY
27	CSI3_CLK_N	Camera, CSI 3 Clock–	Input	MIPI D-PHY
29	CSI3_CLK_P	Camera, CSI 3 Clock+	Input	MIPI D-PHY
21	CSI3_D0_N	Camera, CSI 3 Data 0–	Input	MIPI D-PHY
23	CSI3_D0_P	Camera, CSI 3 Data 0+	Input	MIPI D-PHY
33	CSI3_D1_N	Camera, CSI 3 Data 1–	Input	MIPI D-PHY
35	CSI3_D1_P	Camera, CSI 3 Data 1+	Input	MIPI D-PHY
52	CSI4_CLK_N	Camera, CSI 4 Clock–	Input	MIPI D-PHY
54	CSI4_CLK_P	Camera, CSI 4 Clock+	Input	MIPI D-PHY
46	CSI4_D0_N	Camera, CSI 4 Data 0–	Input	MIPI D-PHY
48	CSI4_D0_P	Camera, CSI 4 Data 0+	Input	MIPI D-PHY
58	CSI4_D1_N	Camera, CSI 4 Data 1–	Input	MIPI D-PHY
60	CSI4_D1_P	Camera, CSI 4 Data 1+	Input	MIPI D-PHY
40	CSI4_D2_N	Camera, CSI 4 Data 2–	Input	MIPI D-PHY
42	CSI4_D2_P	Camera, CSI 4 Data 2+	Input	MIPI D-PHY
64	CSI4_D3_N	Camera, CSI 4 Data 3–	Input	MIPI D-PHY
66	CSI4_D3_P	Camera, CSI 4 Data 3+	Input	MIPI D-PHY
76	DSI_CLK_N	Camera, CSI 5 Clock–	Input	MIPI D-PHY
78	DSI_CLK_P	Camera, CSI 5 Clock+	Input	MIPI D-PHY
70	DSI_D0_N	Camera, CSI 5 Data 0–	Input	MIPI D-PHY
72	DSI_D0_P	Camera, CSI 5 Data 0+	Input	MIPI D-PHY
82	DSI_D1_N	Camera, CSI 5 Data 1–	Input	MIPI D-PHY
84	DSI_D1_P	Camera, CSI 5 Data 1+	Input	MIPI D-PHY

Table 4: Camera Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
213	CAM_I2C_SCL	Camera I^2C Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	Camera I^2C Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
116	CAM0_MCLK	Camera 0 Reference Clock	Output	CMOS – 1.8V
114	CAM0_PWDN	Camera 0 Powerdown or GPIO	Output	CMOS – 1.8V
122	CAM1_MCLK	Camera 1 Reference Clock	Output	CMOS – 1.8V
120	CAM1_PWDN	Camera 1 Powerdown or GPIO	Output	CMOS – 1.8V

1.5.2 Video Input (VI)

The VI block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor execution resources. The VI block provides formatting for RGB, YCbCr, and raw Bayer data in support of several camera user models. These models include single and multi-camera systems, which may have up to six active streams. The input streams are obtained from MIPI compliant CMOS sensor camera modules.

1.5.3 Image Signal Processor (ISP)

The ISP module takes data from the VI/CSI module or memory in raw Bayer format and processes it to YUV output. The imaging subsystem supports raw (Bayer) image sensors up to 24 million pixels. Advanced image processing is used to convert input to YUV data and remove artifacts introduced by high-megapixel CMOS sensors and optics with up to 30-degree CRA.

Features:

- Flexible post-processing architecture for supporting custom computer vision and computational imaging operations
- Bayer domain hardware noise reduction
- Per-channel black-level compensation
- High-order lens-shading compensation
- 3x3 color transform
- Bad pixel correction
- Programmable coefficients for de-mosaic with color artifact reduction
  Color artifact reduction: a two-level (horizontal and vertical) low-pass filtering scheme that is used to reduce/remove any color artifacts that may result from Bayer signal processing and the effects of sampling an image.
- Enhanced down scaling quality
- Edge enhancement
- Color and gamma correction
- Programmable transfer function curve
- Color-space conversion (RGB to YUV)
- Image statistics gathering (per-channel)
  - Two 256-bin image histograms
  - Up to 4,096 local region averages
  - AC flicker detection (50 Hz and 60 Hz)
  - Focus metric block

1.6 Display Controller

The Jetson Xavier NX integrates a Unified Display Controller (based on the NVIDIA NVDisplay architecture) and two independent display outputs. The Display Controller includes a Pixel Processing Engine that fetches pixel data to be processed from DRAM and generates up to six windows of rasterized display-ready pixel data. The instructions for processing the pixel data are captured by the display controller's Front End (FE) logic, which then generates the individual controls for the various stages of pixel processing.

The pixel data to be processed are fetched in the Isochronous Memory Hub (IsoHub) then go through the specified pixel processing, including merging the cursor, in four pipe stages: Pre-Composition (Pre-comp); Composition (Comp); Post-Composition (Post-comp); and Raster Generation (RG). The rasterized display-ready pixel data are available for the separate panels/devices (referred to as display heads) and are fed through a multi-channel crossbar structure to the Serial Output Resources (SOR) in the Display Interface for the standard display output format, i.e., DP (Display Port) and High-Definition Multimedia Interface (HDMI).

Each of the display heads can be run at an independent clock rate and each can drive a different display resolution. Each of the six display windows (A, B, C, D, E, F) can be arbitrarily assigned to any of the display Heads as required, then connected to any one of the display heads for the desired output format.

Features:

- Integrated HDCP key storage, no external SecureROM required
- Six windows that can be assigned to any Head
- One special-purpose TrustZone protected window on Head0
- Maximum raster size: 32768 x 32768
- Maximum active region: 8192 x 8192
- Maximum input surface size: 32768 x 32768
- Maximum fetched size: 8192 x 8192
- Input surface color formats:
  - 16-bit RGB: R4G4B4A4, R5G6B5, A1R5G5B5, and R5G5B5A1
  - 24-bit RGB: A8R8G8B8, X8R8G8B8, A8B8G8R8, and X8B8G8R8
  - 32-bit RGB: A2R10G10B10, A2B10G10R10, X2BL10GL10RL10_XRBIAS, and X2BL10GL10RL10_XVYCC
  - 64-bit RGB: R16_G16_B16_A16_NVBIAS, and R16_G16_B16_A16
  - Packed YUV 422: Y8_U8_Y8_V8_N422, and U8_Y8_V8_Y8_N422
  - Semi Planar YUV 422 (8, 10, 12 bpc):
    - Y8_V8U8_N422, Y8_V8U8_N422R
    - Y10_V10U10_N422, Y10_V10U10_N422R
    - Y12_V12U12_N422, Y12_V12U12_N422R
  - Semi-planar YUV 420 (8, 10, 12 bpc):
    - Y8_V8U8_N420*
    - Y10_V10U10_N420*
    - Y12_V12U12_N420*
  - Semi-planar YUV 444 (8 ,10, 12 bpc):
    - Y8_V8U8_N444
    - Y10_V10U10_N444
    - Y12_V12U12_N444
  - Planar YUV 420 (8, 10, 12 bpc):
    - Y8_U8_V8_N420
    - Y10_U10_V10_N420
    - Y12_U12_V12_N420
  - Planar YUV 444 (8, 10, 12 bpc):
    - Y8_U8_V8_N444
    - Y10_U10_V10_N444
    - Y12_U12_V12_N444
- Pipeline depth
  - 16-bpc, [-1.5, 2.5] range (two range extension bits): De-gamma will clip to 0,1 immediately on the input
- Vsync (VCOUNTER) and immediate (HCOUNTER) flip modes
  - Immediate flip supported for RGB only
  - Immediate flips occur at the second 8-line boundary after the current line

Notes:

1. Cursor cannot be enabled on a Head unless the Head has at least one window group attached. The window group does not need to be enabled.
2. TrustZone cannot be enabled unless Head0 has at least one window group attached. This does not need to be enabled.
3. Color formats marked with an asterisk (*) are programmed as Y_UV in the display manuals, and then byte-swapped later to be Y_VU.
4. 10-bpc and 12-bpc YUV color formats are packed into 16-bpc containers. This effectively limits immediate flips to no faster than one every 16 lines.

1.6.1 HDMI and DisplayPort Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0a/b	Scrambling support Clock/4 support (1/40 bit-rate clock) HDMI 1.4 (up to 340 MHz pixel clock rate) HDMI 2.0 (up to 594 MHz pixel clock rate)
VESA DisplayPort Standard Version 1.4	

A standard DP 1.4 or High-Definition Multimedia Interface (HDMI) 2.0a/b interface is supported. These share the same set of interface pins, so either DisplayPort (DP) or HDMI can be supported natively. Each output collects the output of a display pipeline from the display controller, formats/encodes that output (to a desired format), and then streams it to an output device. Each output can provide an interface to an external device; each output can drive only a single output device at any given time. HDMI support provides a method of transferring both audio and video data; the SOR receives video from the display controller and audio from a separate high-definition audio (HDA) controller, it combines and transmits them as appropriate.

Note: A single CEC controller is shared between the two HDMI/DP interfaces. Both DP0 and DP1 support either DP or HDMI.

Features:

- DisplayPort
  - Multichannel audio from HDA controller, up to eight channels, 96 kHz, 24-bit
  - DP1.4 supports HBR3 at 8.1 Gbps
  - (up to) 540 MHz pixel clock rate (i.e., 1.62 GHz for RBR, 2.7 GHz for HBR, 5.4 GHz for HBR2, and 8.1 Gbps for HBR3.
  - 8b/10b encoding support
  - External dual-mode standard support
  - Audio streaming support
- HDMI
  - (up to) 594 MHz pixel clock
    - 8/12 bpc RGB and YUV444
    - 8/10/12 bpc YUV422
    - 8 bpc YUV420 (10/12 bpc YUV frame buffers should be output as YUV422)
  - HDMI Vendor-Specific Info frame (VSI) packet transmission
  - On HDMI, multichannel audio from HDA controller, up to eight channels, 192 kHz, 24-bit.
  - Fuse calibration information for HDMI analog parameter(s)
  - 1080i output on HDMI
- DP or HDMI connectors via appropriate external level shifting
- HDCP 2.2 and 1.4 over either DP or HDMI
  Note: refer to NVIDIA software release notes for detailed specifications.
- External Dual Mode standard (DP2HDMI passive or active adapters and adapter discovery)
- Generic info frame transmission
- Frame-packed 3D stereo mode

Table 5: HDMI/DisplayPort/eDP Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
39	DP0_TXD0_N	DisplayPort 0 Lane 0 or HDMI Lane 2–	Output	AC-Coupled on carrier board
41	DP0_TXD0_P	DisplayPort 0 Lane 0 or HDMI Lane 2+	Output	AC-Coupled on carrier board
45	DP0_TXD1_N	DisplayPort 0 or HDMI Lane 1–	Output	AC-Coupled on carrier board
47	DP0_TXD1_P	DisplayPort 0 or HDMI Lane 1+	Output	AC-Coupled on carrier board

Pin #	Signal Name	Description	Direction	Pin Type
51	DP0_TXD2_N	DisplayPort 0 Lane 2– or HDMI Lane 0–	Output	AC-Coupled on carrier board
53	DP0_TXD2_P	DisplayPort 0 Lane 2+ or HDMI Lane 0+	Output	AC-Coupled on carrier board
57	DP0_TXD3_N	DisplayPort 0 Lane 3– or HDMI Clk Lane–	Output	AC-Coupled on carrier board
59	DP0_TXD3_P	DisplayPort 0 Lane 3+ or HDMI Clk Lane+	Output	AC-Coupled on carrier board
90	DP0_AUX_N	Display Port 0 Aux– or HDMI DDC SDA	Bidir	AC-Coupled on Carrier Board (eDP/DP)
92	DP0_AUX_P	Display Port 0 Aux+ or HDMI DDC SCL	Bidir	AC-Coupled on Carrier Board (eDP/DP)
88	DP0_HPD	Display Port 0 or HDMI Hot Plug Detect	Input	CMOS – 1.8V
63	DP1_TXD0_N	DisplayPort 1 Lane 0 or HDMI Lane 2–	Output	AC-Coupled on carrier board
65	DP1_TXD0_P	DisplayPort 1 Lane 0 or HDMI Lane 2+	Output	AC-Coupled on carrier board
69	DP1_TXD1_N	DisplayPort 1 or HDMI Lane 1–	Output	AC-Coupled on carrier board
71	DP1_TXD1_P	DisplayPort 1 or HDMI Lane 1+	Output	AC-Coupled on carrier board
75	DP1_TXD2_N	DisplayPort 1 Lane 2– or HDMI Lane 0–	Output	AC-Coupled on carrier board
77	DP1_TXD2_P	DisplayPort 1 Lane 2+ or HDMI Lane 0+	Output	AC-Coupled on carrier board
81	DP1_TXD3_N	DisplayPort 1 Lane 3– or HDMI Clk Lane–	Output	AC-Coupled on carrier board
83	DP1_TXD3_P	DisplayPort 1 Lane 3+ or HDMI Clk Lane+	Output	AC-Coupled on carrier board
98	DP1_AUX_N	Display Port 1 Aux– or HDMI DDC SDA	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
100	DP1_AUX_P	Display Port 1 Aux+ or HDMI DDC SCL	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC
96	DP1_HPD	Display Port 1 or HDMI Hot Plug Detect	Input	CMOS – 1.8V
94	HDMI_CEC	HDMI CEC	Bidir	Open Drain, 1.8V

Note: (Resolution + Refresh Rate + Pixel Depth + Format) must be within specification limits to achieve support for desired pixel depth.

1.6.2 Embedded DisplayPort (eDP)

Standard
VESA Embedded DisplayPort Standard Version 1.4a

Embedded DisplayPort (eDP) is a mixed-signal interface consisting of four differential serial output lanes and one PLL. This PLL is used to generate a high-frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. eDP modes consist of 1.6 GHz for RBR; 2.16 GHz, 2.43 GHz, and 2.7 GHz for HBR; 3.24 GHz, 4.32 GHz, 5.4 GHz for HBR2, and 8.1 Gbps for HBR3.

Note:	eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

The eDP block collects pixels from the output of the display pipeline, formats/encodes them to the eDP format, and then streams them to various output devices. It drives local panels only (does not support an external DP port), and it includes a small test pattern generator and CRC generator.

Features:

- 1/2/4/ lane, single link
- Additional link rates (2.16, 2.43, 3.24, 4.32 Gbps)
- Enhanced framing
- Power sequencing
- Reduced auxiliary timing
- Reduced main voltage swing
- ASSR (alternate seed scrambler reset) for internal eDP panels

Note:	For eDP pin information, refer to Table 5 HDMI/DisplayPort/eDP Pin Descriptions.

1.7 High-Definition Audio-Video Subsystem

Standard
High-Definition Audio Specification Version 1.0a

The HD Audio-Video Subsystem uses a collection of functional blocks to off-load audio and video processing activities from the CPU complex, resulting in fast, fully concurrent, and highly efficient operation. This subsystem is comprised of the following:

- (2x) Multi-standard video decoder
- (2x) Multi-standard video encoder
- JPEG processing block
- Video Image Compositor (VIC)
- Audio Processing Engine (APE)
- High-Definition Audio (HDA)

1.7.1 Multi-Standard Video Decoder

The Jetson Xavier NX incorporates two instances of the NVIDIA Multi-Standard Video Decoder (NVDEC). This video decoder accelerates video decode, supporting low resolution mobile content, Standard Definition (SD), High Definition (HD), and UltraHD (8K, 4K, etc.) video profiles. The video decoder is designed to be extremely power efficient without sacrificing performance. The video decoder communicates with the memory controller through the video DMA which supports a variety of memory format output options. For low power operations, the video decoder can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques.

Table 6: Video Decoder Standards

Standard	Profile(s)	Resolution (Max Number of Streams)	Throughput (up to)
H.264	Baseline, Main, High,	2x 2160p60 | 6x 2160p30 | 10x 1080p60 | 22x 1080p30	2x 740 MP/s
	MVC (per view considering two views)*	2x 2160p30 | 4x 1080p60 | 10x 1080p30	2x 370 MP/s
			(Max Throughput half for YUV444 as compared to YUV420)
HEVC	Main, Main 10, Main 12	2x 4320p30 | 6x 2160p60 | 12x 2160p30 | 22x 1080p60 | 44x 1080p30	2x 1300 MP/s
	Main 444 12, MV*	2x 2160p60 | 6x 2160p30 | 10x 1080p60 | 22x 1080p30	2x 650 MP/s
			(Max Throughput half for YUV444 as compared to YUV420)
VP9	Profile 0. Profile 2	2x 4320p30 | 4x 2160p60 | 8x 2160p30 | 14x 1080p60 | 30x 1080p30	2x 1000 MP/s

Supported Video Standards - Decode

- Bitrates: 5-10 Mbps for 1080p | Less than 20 Mbps for 2160p
- *Maximum throughput is half for YUV444 compared to YUV420
- Supports HEVC Main 12 (without monochrome)
- Supports Main 444 12 (without YUV422/YUV400)
- 2x 8K30, 6x 4K60, 12x 4K30 - Subject to memory availability

1.7.2 Multi-Standard Video Encoder

The Jetson Xavier NX incorporates two instances of the NVIDIA Multi-Standard Video Encoder (NVENC). This multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high-quality video encoding operations for mobile applications such as video recording and video conferencing. The encode processor is designed to be extremely power efficient without sacrificing performance.

Table 7: Video Encoder Standards

Standard	Profile(s)	Resolution (Max Number of Streams)	Throughput (up to)
H264	HP	2x 2160p30 | 4x 1080p60 | 10x 1080p30	(2x) 370 MP/s
	UHP	2x 2160p60 | 4x 2160p30 | 10x 1080p60 | 20x 1080p30	(2x) 660 MP/s
HEVC	HP	2x 2160p30 | 4x 1080p60 | 10x 1080p30	(2x) 350 MP/s
	UHP	2x 2160p60 | 4x 2160p30 | 10x 1080p60 | 22x 1080p30	(2x) 700 MP/s
VP9	HP	2x 2160p30 | 6x 1080p60 | 12x 1080p30	(2x) 410 MP/s
	UHP	2x 2160p30 | 6x 1080p60 | 14x 1080p30	(2x) 445 MP/s

Supported Video Standards - Encode

- Bitrates: 5-10 Mbps for 1080p | Less than 20 Mbps for 2160p
- Maximum throughput is half for YUV444 compared to YUV420

Note:	A/V codec, post-processing, and containers support are subject to software support; refer to NVIDIA software release notes for detailed specifications. Additional audio codecs may be supported using 3rd parties.

Features:

- Timestamp for Audio/Video Sync
- CBR and VBR rate control (supported in firmware)
- Programmable intra-refresh for error resiliency
- Macro-block based and bit based packetization (multiple slice)
- Motion estimation (ME) only mode

1.7.3 JPEG Processing Block

The JPEG processing block is responsible for JPEG (de)compression calculations (based on JPEG still image standard), image scaling, decoding (YUV420, YUV422H/V, YUV444, YUV400), and color space conversion (RGB to YUV; decode only).

Input (encode) formats:

- Pixel width: 8 bpc
- Subsample format: YUV420
- Resolution up to 16K x 16K
- Pixel pack format
  - Semi-planar/planar for 420

Output (decode) formats:

- Pixel width 8 bpc
- Resolution up to 16K x 16K
- Pixel pack format
  - Semi-planar/planar for YUV420
  - YUY2/planar for 422H/422V
  - Planar for YUV444
  - Interleave for RGBA

1.7.4 Video Image Compositor (VIC)

VIC implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending, and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features:

- Color Decompression
- High-quality Deinterlacing
- Inverse Teleciné
- Temporal Noise Reduction
  - New Bilateral Filter as spatial filter
  - Improved TNR3 algorithm
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation
- Geometry transform processing
  - Programmable nine-points controlled warp patch for distortion correction
  - Real-time on-the-fly position generation from sparse warp map surface
  - Pincushion/barrel/moustache distortion correction
  - Distortion correction of 180- and 360-degree wide FOV lens
  - Scene perspective orientation adjustment with IPT
  - Full warp map capability

- Non-fixed Patch size with 4x4 regions
- External Mask bit map surface

1.7.5 Audio Processing Engine (APE)

The Audio Processing Engine (APE) is a self-contained unit with dedicated audio clocking that enables Ultra Low Power (ULP) audio processing. Software based post processing effects enable the ability to implement custom audio algorithms.

Features:

- 96 KB Audio RAM
- Audio Hub (AHUB) I/O Modules
  - 2xI2S/3xDMIC/2xDSPK Audio Hub (AHUB) Internal Modules
- Sample Rate converter
- Mixer
- Audio Multiplexer
- Audio De-multiplexer
- Master Volume Controller
- Multi-Channel IN/OUT
  - Digital Audio Mixer: 10-in/5-out
    - Up to eight channels per stream
    - Simultaneous Multi-streams
    - Flexible stream routing
  - Parametric equalizer: up to 12 bands
  - Low latency sample rate conversion (SRC) and high-quality asynchronous sample rate conversion (ASRC)

1.7.6 High-Definition Audio (HDA)

Standard
Intel High-Definition Audio Specification Revision 1.0a

The Jetson Xavier NX implements an industry-standard High-Definition Audio (HDA) controller. This controller provides a multi-channel audio path to the HDMI interface. The HDA block also provides an HDA-compliant serial interface to an audio codec. Multiple input and output streams are supported.

Features:

- Supports HDMI 2.0 and DP1.4
- Support up to two audio streams for use with HDMI/DP
- Supports striping of audio out across 1,2,4[a] SDO lines
- Supports DVFS with maximum latency up to 208 µs for eight channels
- Supports two internal audio codecs
- Audio Format Support
  - Uncompressed Audio (LPCM): 16/20/24 bits at 32/44.1/48/88.2/96/176.4/192[b] kHz
  - Compressed Audio format: AC3, DTS5.1, MPEG1, MPEG2, MP3, DD+, MPEG2/4 AAC, TrueHD, DTS-HD

[a] Four SDO lines: cannot support one stream, 48 kHz, 16-bits, two channels; for this case, use a one or two SDO line configuration.
[b] DP protocol sample frequency limitation: cannot support >96 kHz; i.e., does not support 176.4 kHz and 196 kHz.

1.8 Interface Descriptions

The following sections outline the interfaces available on the Jetson Xavier NX module and details the module pins used to interact with and control each interface. See the *Jetson Xavier NX Product Design Guide* for complete functional descriptions, programming guidelines, and register listings for each of these blocks.

1.8.1 SD/eMMC

Standard	Notes
SD Specifications, Part A2, SD Host Controller Standard Specification, Version 4.1	
SD Specifications, Part 1, Physical Layer Specification, Version 4.2	
SD Specifications, Part 1, eSD (Embedded SD) Addendum, Version 2.10	
SD Specifications, Part E1, SDIO Specification Version, 4.1	Support for SD 4.0 Spec without UHS-II
JEDEC Standard, Embedded Multimedia Card (eMMC) Electrical Standard 5.1	JESD84-B51

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to an external SD card or SDIO device and provides the interface for the on-module eMMC. It has a direct memory controller interface and is capable of initiating data transfers between system memory and an external card or device. It also has an AMBA Peripheral Bus (APB) slave interface to access its configuration registers. To access the on-system RAM for MicroBoot, the SD/MMC controller relies on the path to System RAM in the memory controller.

Features:

- 8-bit data interface to on-module eMMC
- 4-bit data interface for SD cards/SDIO
- Supports card interrupts for SD cards (4-bit SD modes) and SDIO devices
- Supports read wait control and suspend/resume operation for SD cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB

Table 8: SD/SDIO Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
229	SDMMC_CLK	SD Card or SDIO Clock	Output	CMOS – 1.8V/3.3V
227	SDMMC_CMD	SD Card or SDIO Command	Bidir	CMOS – 1.8V/3.3V
219	SDMMC_DAT0	SD Card or SDIO Data 0	Bidir	CMOS – 1.8V/3.3V
221	SDMMC_DAT1	SD Card or SDIO Data 1	Bidir	CMOS – 1.8V/3.3V
223	SDMMC_DAT2	SD Card or SDIO Data 2	Bidir	CMOS – 1.8V/3.3V
225	SDMMC_DAT3	SD Card or SDIO Data 3	Bidir	CMOS – 1.8V/3.3V

1.8.2 Universal Serial Bus (USB)

Standard	Notes
Universal Serial Bus Specification Revision 3.1	Host mode only
Universal Serial Bus Specification Revision 3.0	Device mode only
Universal Serial Bus Specification Revision 2.0	USB Battery Charging Specification, version 1.2; including Data Contact Detect protocol Modes: Host and Device Speeds: Low, Full, and High
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	

An xHCI/Device controller (named XUSB) supports the xHCI programming model for scheduling transactions and interface managements as a host that natively supports USB 3.1, USB 2.0, and USB 1.1 transactions with its USB 3.1 and USB 2.0 interfaces. The XUSB controller supports USB 2.0 L1 and L2 (suspend) link power management and USB 3.1 U1, U2, and U3 (suspend) link power managements. The XUSB controller supports remote wakeup, wake on connect, wake on disconnect, and wake on overcurrent in all power states, including sleep mode.

1.8.2.1 USB 2.0 Operation

Each USB 2.0 port (3x) operates in USB 2.0 high-speed mode when connecting directly to a USB 2.0 peripheral and operates in USB 1.1 full- and low-speed modes when connecting directly to a USB 1.1 peripheral. When operating in High-Speed mode, each USB 2.0 port is allocated with one High-Speed unit bandwidth. Approximately a 480 Mb/s bandwidth is allocated to each USB 2.0 port. All USB 2.0 ports operating in full- or low-speed modes share one full- and low-speed bus instance, which means 12 Mb/s theoretical bandwidth is distributed across these ports.

Table 9: USB 2.0 Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
109	USB0_D_N	USB 2.0 Port 0 Data–	Bidir	USB PHY
111	USB0_D_P	USB 2.0 Port 0 Data+	Bidir	USB PHY
115	USB1_D_N	USB 2.0 Port 1 Data–	Bidir	USB PHY
117	USB1_D_P	USB 2.0 Port 1 Data+	Bidir	USB PHY
121	USB2_D_N	USB 2.0 Port 2 Data–	Bidir	USB PHY
123	USB2_D_P	USB 2.0 Port 2 Data+	Bidir	USB PHY

1.8.2.2 USB 3.1 Operation

The USB 3.1 port supports:

- Generation 1 - SuperSpeed USB (5 Gbps transfer rates)
- Generation 2 - SuperSpeed USB (10 Gbps transfer rates)

Table 10: USB 3.1 Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
161	USBSS_RX_N	USB SS Receive– (USB 3.1 Ctrl #0)	Input	USB SS PHY, AC-Coupled (off the module)
163	USBSS_RX_P	USB SS Receive+ (USB 3.1 Ctrl #0)	Input	USB SS PHY, AC-Coupled (off the module)
166	USBSS_TX_N	USB SS Transmit– (USB 3.1 Ctrl #0)	Output	USB SS PHY, AC-Coupled on carrier board
168	USBSS_TX_P	USB SS Transmit+ (USB 3.1 Ctrl #0)	Output	USB SS PHY, AC-Coupled on carrier board

1.8.3 PCI Express (PCIe)

Standard	Notes
PCI Express Base Specification Revision 3.0	Jetson Xavier NX meets the timing requirements for the Gen3 (8.0 GT/s) for x1 and Gen4 (16.0 GT/s) for x4 data rates. Refer to specification for complete interface timing details.

Standard	Notes
	Although NVIDIA validates that the design complies with the PCIe specification, PCIe software support may be limited.

The Jetson Xavier NX module integrates two PCIe controllers supporting:

- Connections to two interfaces (1x1 + 1x4).
- x1 (supports Root Port only), x4 (supports Root Port or Endpoint modes) Upstream and downstream AXI interfaces that serve as the control path from the Jetson Xavier NX to the external PCIe device
- Gen3 (8 GT/s), supported on x1
- Gen4 (16 GT/s) supported on x4
- Two PCIe controllers, five lanes for a total of 144 GT/s. One controller operates in x1 mode only. The second controller can operate in x1 or x2 or x4 mode.

Table 11: PCIe Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
131	PCIE0_RX0_N	PCIe #0 Receive 0– (PCIe Ctrl #5 Lane 0)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
133	PCIE0_RX0_P	PCIe #0 Receive 0+ (PCIe Ctrl #5 Lane 0)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
137	PCIE0_RX1_N	PCIe #0 Receive 1– (PCIe Ctrl #5 Lane 1)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
139	PCIE0_RX1_P	PCIe #0 Receive 1+ (PCIe Ctrl #5 Lane 1)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
149	PCIE0_RX2_N	PCIe #0 Receive 2– (PCIe Ctrl #5 Lane 2)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
151	PCIE0_RX2_P	PCIe #0 Receive 2+ (PCIe Ctrl #5 Lane 2)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
155	PCIE0_RX3_N	PCIe #0 Receive 3– (PCIe Ctrl #5 Lane 3)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
157	PCIE0_RX3_P	PCIe #0 Receive 3+ (PCIe Ctrl #5 Lane 3)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect
134	PCIE0_TX0_N	PCIe #0 Transmit 0– (PCIe Ctrl #5 Lane 0)	Output	PCIe PHY, AC-Coupled on carrier board
136	PCIE0_TX0_P	PCIe #0 Transmit 0+ (PCIe Ctrl #5 Lane 0)	Output	PCIe PHY, AC-Coupled on carrier board
140	PCIE0_TX1_N	PCIe #0 Transmit 1– PCIe Ctrl #5 Lane 1)	Output	PCIe PHY, AC-Coupled on carrier board
142	PCIE0_TX1_P	PCIe #0 Transmit 1+ (PCIe Ctrl #5 Lane 1)	Output	PCIe PHY, AC-Coupled on carrier board
148	PCIE0_TX2_N	PCIe #0 Transmit 2– (PCIe Ctrl #5 Lane 2)	Output	PCIe PHY, AC-Coupled on carrier board
150	PCIE0_TX2_P	PCIe #0 Transmit 2+ (PCIe Ctrl #5 Lane 2)	Output	PCIe PHY, AC-Coupled on carrier board
154	PCIE0_TX3_N	PCIe #0 Transmit 3– (PCIe Ctrl #5 Lane 3)	Output	PCIe PHY, AC-Coupled on carrier board
156	PCIE0_TX3_P	PCIe #0 Transmit 3+ (PCIe Ctrl #5Lane 3)	Output	PCIe PHY, AC-Coupled on carrier board

Pin #	Signal Name	Description	Direction	Pin Type
181	PCIE0_RST*	PCIe #0 Reset (PCIe Ctrl #5). 4.7kΩ pull-up to 3.3V on the module.	Bidir	Open Drain 3.3V, Pull-up on the module
180	PCIE0_CLKREQ*	PCIe #0 Clock Request (PCIe Ctrl #5). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain 3.3V, Pull-up on the module
160	PCIE0_CLK_N	PCIe #0 Reference Clock– Mux controlled by GPIO	Bidir	PCIe PHY
162	PCIE0_CLK_P	PCIe #0 Reference Clock+ Mux controlled by GPIO	Output	PCIe PHY
167	PCIE1_RX0_N	PCIe #1 Receive 0– (PCIe Ctrl #4 Lane 0)	Input	PCIe PHY, AC-Coupled on carrier board if direct connect.
169	PCIE1_RX0_P	PCIe #1 Receive 0+ (PCIe Ctrl #4 Lane 0)	Input	PCIe PHY, AC-Coupled on carrier board if direct connect.
172	PCIE1_TX0_N	PCIe #1 Transmit 0– (PCIe Ctrl #4 Lane 0)	Output	PCIe PHY, AC-Coupled on carrier board
174	PCIE1_TX0_P	PCIe #1 Transmit 0+ (PCIe Ctrl #4 Lane 0)	Output	PCIe PHY, AC-Coupled on carrier board
183	PCIE1_RST*	PCIe #1 Reset (PCIe Ctrl #4). 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain 3.3V, Pull-up on the module
182	PCIE1_CLKREQ*	PCIe #1 Clock Request (PCIe Ctrl #4). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain 3.3V, Pull-up on the module
173	PCIE1_CLK_N	PCIe #1 Reference Clock– (PCIe Ctrl #4)	Output	PCIe PHY
175	PCIE1_CLK_P	PCIe #1 Reference Clock+ (PCIe Ctrl #4)	Output	PCIe PHY
179	PCIE_WAKE*	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	Input	Open Drain 3.3V, Pull-up on the module

Note: Upstream Type 1 Vendor Defined Messages (VDM) should be sent by the Endpoint Port if the Root Port also belongs to same vendor/partner; otherwise, the VDM is silently discarded.

See the *Jetson Xavier NX Product Design Guide* for supported USB 3.1/PCIe configuration and connection examples.

1.8.4 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) controller allows a duplex, synchronous, serial communication between the controller and external peripheral devices; it supports both Master and Slave modes of operation on the SPI bus. See the *Jetson Xavier NX Product Design Guide* for more information.

Features:

- 2x SPI Interface
- Maximum data rate: 65 Mbps in Master Mode, 50 Mbps in Slave Mode
- Master mode operation
  - All transfer modes (Mode 0, Mode 1, Mode 2, Mode 3) supported for both transmit and receive transactions
- FIFO Size: 64 x 32 bits
- Programmable packet sizes of 4 to 32 bits
- Programmable clock phase and polarity
- Programmable delay between consecutive transfers
- Chip select controllable by software or generated by hardware on packet boundaries

Table 12: SPI Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
91	SPI0_SCK	SPI 0 Clock	Bidir	CMOS – 1.8V
89	SPI0_MOSI	SPI 0 Master Out / Slave In	Bidir	CMOS – 1.8V
93	SPI0_MISO	SPI 0 Master In / Slave Out	Bidir	CMOS – 1.8V
95	SPI0_CS0*	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V
97	SPI0_CS1*	SPI 0 Chip Select 1	Bidir	CMOS – 1.8V
106	SPI1_SCK	SPI 1 Clock	Bidir	CMOS – 1.8V
104	SPI1_MOSI	SPI 1 Master Out / Slave In	Bidir	CMOS – 1.8V
108	SPI1_MISO	SPI 1 Master In / Slave Out	Bidir	CMOS – 1.8V
110	SPI1_CS0*	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V
112	SPI1_CS1*	SPI 1 Chip Select 1	Bidir	CMOS – 1.8V

Figure 1: SPI Master Timing Diagram

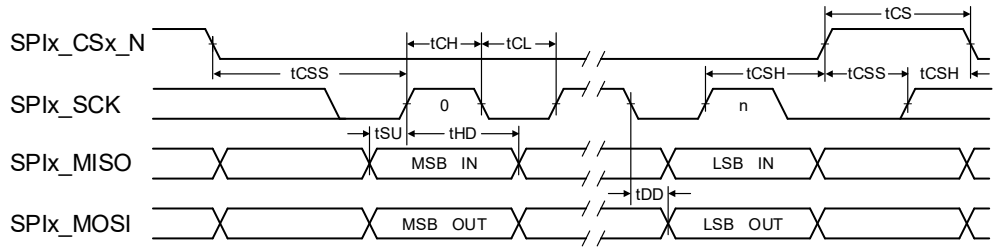


Table 13: SPI Master Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Fsck	SPIx_SCK clock frequency	–	65	MHz
Psck	SPIx_SCK period	1/Fsck	–	ns
t_{CH}	SPIx_SCK high time	50%Psck -10%	50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%	50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1	–	V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1	–	V/ns
t_{SU}	SPIx_MISO setup to SPIx_SCK rising edge	2	–	ns
t_{HD}	SPIx_MISO hold from SPIx_SCK rising edge	3	–	ns
t_{DD}	Active Clock edge to MOSI data output valid	–	6	
t_{CSS}	SPIx_CSx setup time	2	–	ns
t_{CSH}	SPIx_CSx hold time	3	–	ns
t_{CS}	SPIx_CSx high time	10	–	ns

Figure 2: SPI Slave Timing Diagram

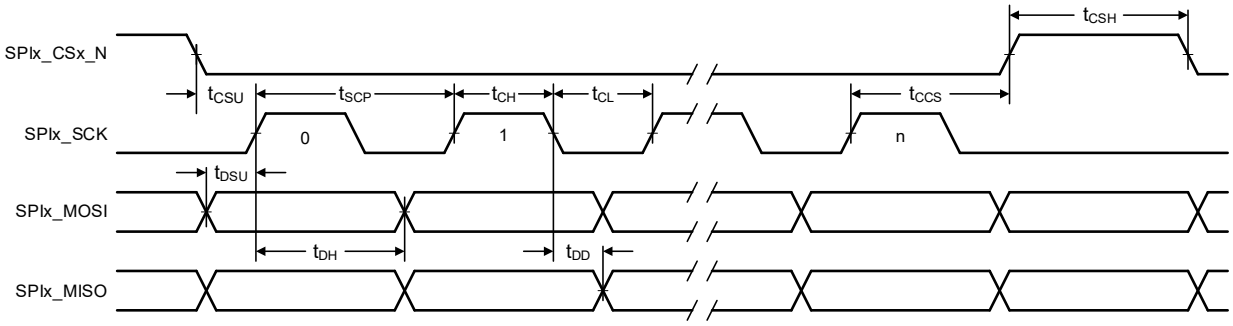


Table 14: SPI Slave Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
T_{SCP}	SPIx_SCK period	2*(t_{SDD}+ t_{MSU}[1])		ns
T_{SCH}	SPIx_SCK high time	t_{SDD} + t_{MSU}[1]		ns
T_{SCL}	SPIx_SCK low time	t_{SDD} + t_{MSU}[1]		ns
T_{SCSU}	SPIx_CSx_n setup time	1		t_{SCP}
T_{SCSH}	SPIx_CSx_n high time	1		t_{SCP}
T_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1	1	t_{SCP}
T_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1	1	ns
T_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2	11	ns
T_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge	3.5	16	ns
T_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge	3	13	ns

1. t_{MSU} is the setup time required by the external master

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

1.8.5 Universal Asynchronous Receiver/Transmitter (UART)

The UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

Note: The UART receiver input has low baud rate tolerance in 1-stop bit mode. External devices must use two stop bits.

In 1-stop bit mode, the UART receiver can lose sync between the receiver and the external transmitter resulting in data errors/corruption. In 2-stop bit mode, the extra stop bit allows the UART receiver logic to align properly with the UART transmitter.

Features:

- 3x UART Interface
- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200 MHz, baud rate of 12.5 Mbits/second
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped

- Priority interrupts mechanism
- Flow control support on RTS and CTS
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 15: UART Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
99	UART0_TXD	UART #0 Transmit	Output	CMOS – 1.8V
101	UART0_RXD	UART #0 Receive	Input	CMOS – 1.8V
103	UART0_RTS*	UART #0 Request to Send	Output	CMOS – 1.8V
105	UART0_CTS*	UART #0 Clear to Send	Input	CMOS – 1.8V
203	UART1_TXD	UART #1 Transmit	Output	CMOS – 1.8V
205	UART1_RXD	UART #1 Receive	Input	CMOS – 1.8V
207	UART1_RTS*	UART #1 Request to Send	Output	CMOS – 1.8V
209	UART1_CTS*	UART #1 Clear to Send	Input	CMOS – 1.8V
236	UART2_TXD	UART #2 Transmit	Output	CMOS – 1.8V
238	UART2_RXD	UART #2 Receive	Input	CMOS – 1.8V

1.8.6 Controller Area Network (CAN)

Standard	Notes
ISO/DIS 16845-2	CAN conformance test
ISO 11898-1:2015	Data link layer and physical signaling; CAN FD Frame formats
ISO 11898-4:2004	Time-triggered communication

The Jetson Xavier NX integrates the Bosch Time-Triggered Controller Area Network (M_TTCAN) controller version 3.2.0. One independent CAN port/channel supports connectivity to one CAN network. Each port instantiates the Bosch M_TTCAN module, a message RAM module, an APB slave interface module, interrupt aggregator, time-triggered control module, and a wake detect module. All M_TTCAN external modules have direct connections to M_TTCAN except for the wake detect module.

Features:

- Standard frame and extended frame transmission/reception enable
- Transfer rate: programmable bit rates up to 15 Mbps
- 0 – 8-byte data length, with the ability to receive the first 8 bytes when data length coding is > 8 Bytes
- 32 message buffers per channel
- Prioritization of transmit buffers
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receives block function
- Flexible maskable identifier filter support for two 32-bit, or four 16-bit, or eight 8-bit filters for each channel
- Programmable data bit time, communication baud rate, and sample point.
  - As an example, the following sample-point configurations can be configured: 66.7%, 70.0%, 75.0%, 80.0%, 81.3%, 85.0%, and 87.5%
  - Baud rates in the range of 10 kbps up to 1000 kbps can be configured
- Enhanced features:
  - Each message buffer can be configured to operate as a transmit or a receive message buffer
  - Transmission priority is controlled by the identifier or by mailbox number (selectable)

  - A transmission request can be aborted by clearing the dedicated Transmit-Request flag of the concerned message buffer.
  - Automatic block transmission (ABT) operation mode
  - Time stamp function for CAN channels 0 to *n* in collaboration with timers
- Release from bus-off state by software
- Wake-up with integrated low-pass filter (debounce) option to prevent short glitches on CAN bus, through CAN receive signal toggling from CAN transceiver
  - For normal operation (after wake) there is a digital filter in the CAN controller
- Listen-only mode to monitor CAN bus
- Wake-up signal to both internal and external (either interrupt signal or GPIO) to initiate power up if needed.
  - Ready to receive the first CAN message within 10ms of wake event generated by the CAN master.
  - Ready to transmit the first CAN message within 50ms of wake event generated by the CAN master.
- Loop back for self-test

Table 16: CAN Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
145	CAN_TX	CAN PHY	Output	CMOS – 3.3V
143	CAN_RX	CAN PHY	Input	CMOS – 3.3V

1.8.7 Inter-Chip Communication (I^2C)

Standard	Notes
NXP inter-IC-bus (I^2C) specification	https://i2c.info/i2c-bus-specification

This general purpose I^2C controller allows system expansion for I^2C-based devices as defined in the NXP inter-IC-bus (I^2C) specification. The I^2C bus supports serial device communications to multiple devices. (4x I^2C) The I^2C controller handles clock source negotiation, speed negotiation for standard and fast devices, 7-bit slave address support according to the I^2C protocol and supports master and slave modes of operation.

The I^2C controller supports the following operating modes:

- Master – Standard-mode (up to 100 Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1 Mbit/s).
- Slave – Standard-mode (up to 100 Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1 Mbit/s).

Table 17: I2C Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
185	I2C0_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	Bidir	Open Drain – 3.3V
187	I2C0_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
189	I2C1_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
191	I2C1_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.	Bidir	Open Drain – 3.3V
232	I2C2_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
234	I2C2_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V

1.8.8 Inter-IC Sound (I^2S)

Standard
Inter-IC Sound (I^2S) specification

The I^2S controller transports streaming audio data between system memory and an audio codec. The I^2S controller supports I^2S format, left-justified mode format, right-justified mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I^2S) bus specification.

The I^2S and PCM (master and slave modes) interfaces support clock rates up to 24.5760 MHz.

The I^2S controller supports point-to-point serial interfaces for the I^2S digital audio streams. I^2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, and those with digital TV sound may be directly connected to the I^2S controller. The controller also supports the PCM and telephony mode of data-transfer. Pulse-Code-Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. The Telephony mode is used to transmit and receive data to and from an external mono CODEC in a slot-based scheme of time-division multiplexing (TDM). The I^2S controller supports Bidirectional audio streams and can operate in half-duplex or full-duplex mode.

Features:

- Basic I^2S modes to be supported (I^2S, RJM, LJM, and DSP) in both master and slave modes
- PCM mode with short (one bit-clock wide) and long-fsync (two bit-clock wide) in both master and slave modes
- NW-mode with independent slot-selection for both transmit and receive
- TDM mode with flexibility in number of slots and slot(s) selection
- Capability to drive-out a high-z outside the prescribed slot for transmission
- Flow control for the external input/output stream

Table 18: TDM Timing Parameters (Slave Mode)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
F_{SCK}	Frequency	–	24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$	–	ns	
T_{FDLY}	I2Sx_LRCK delay	0	4.5	ns	
t_{DDLY}	I2Sx_SDOUT delay	0	4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	ns	
t_{DH}	I2Sx_SDIN hold time	2	–	ns	
t_{RT}	I2Sx_SCLK rise time	–	5% * T_{CYL}	ns	
t_{FT}	I2Sx_SCLK fall time	–	5% * T_{CYL}	ns	
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}	–	ns	
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}	–	ns	

Table 19: TDM Timing Parameters (Master Mode)

Symbol	Parameter	Minimum	Maximum	Unit	Notes
F_{SCK}	Frequency	–	24.576	MHz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$	–	ns	
t_{DDLY}	I2Sx_SDOUT delay	0	4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	ns	

Symbol	Parameter	Minimum	Maximum	Unit	Notes
t_{DH}	I2Sx_SDIN hold time	2	–	ns	
t_{FSU}	I2Sx_LRCK setup	2	45% * T_{CYL} - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	55% T_{CYL} + 2	–	ns	2
t_{RT}	I2Sx_SCLK rise time	–	5% * T_{CYL}	ns	
t_{FT}	I2Sx_SCLK fall time	–	5% * T_{CYL}	ns	
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}	–	ns	
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}	–	ns	

1. Maximum t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Minimum t_{FSH} (55% TCYL + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Minimum t_{FSH} is 2ns.

Table 20: I2S Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
199	I2S0_SCLK	I2S Audio Port 0 Clock	Bidir	CMOS – 1.8V
197	I2S0_FS	I2S Audio Port 0 Left/Right Clock	Bidir	CMOS – 1.8V
193	I2S0_DOUT	I2S Audio Port 0 Data Out	Output	CMOS – 1.8V
195	I2S0_DIN	I2S Audio Port 0 Data In	Input	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V

1.8.9 Gigabit Ethernet

Standard	Notes
Gigabit Ethernet (GbE)	IEEE 802.3ab

The Jetson Xavier NX integrates a Realtek RTL8211FDI Gigabit Ethernet controller. The on-module Ethernet controller supports:

- 10/100/1000 Gigabit Ethernet
- IEEE 802.3u Media Access Controller (MAC)

Table 21: Gigabit Ethernet Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
184	GBE_MDI0_N	GbE Transformer Data 0–	Bidir	MDI
186	GBE_MDI0_P	GbE Transformer Data 0+	Bidir	MDI
190	GBE_MDI1_N	GbE Transformer Data 1–	Bidir	MDI
192	GBE_MDI1_P	GbE Transformer Data 1+	Bidir	MDI
196	GBE_MDI2_N	GbE Transformer Data 2–	Bidir	MDI
198	GBE_MDI2_P	GbE Transformer Data 2+	Bidir	MDI

Pin #	Signal Name	Description	Direction	Pin Type
202	GBE_MDI3_N	GbE Transformer Data 3–	Bidir	MDI
204	GBE_MDI3_P	GbE Transformer Data 3+	Bidir	MDI
188	GBE_LED_LINK	Ethernet Link LED (Green)	Output	
194	GBE_LED_ACT	Ethernet Activity LED (Yellow)	Output	

1.8.10 Fan

The Jetson Xavier NX includes a Pulse Width Modulator (PWM) and Tachometer functionality to enable fan control as part of a thermal solution. The PWM controller is a frequency divider with a varying pulse width. The PWM runs off a device clock programmed in the Clock and Reset controller and can be any frequency up to the device clock maximum speed of 48 MHz. The PWM gets divided by 256 before being subdivided based on a programmable value.

1.8.11 Pulse Width Modulator (PWM)

Jetson Xavier NX has four PWM outputs. Each PWM output is based on a frequency divider whose pulse width varies. Each has a programmable frequency divider and a programmable pulse width generator. The PWM controller supports one PWM output for each of its four instances. Each instance is allocated a 64 KB independent address space.

Frequency division is a 13-bit programmable value, and pulse division is an 8-bit value. The PWM can run at a maximum frequency of up to 408 MHz. The PWM controller can source its clock from either CLK_M or PLLP. CLK_M (19.2 MHz) is derived from the OSC clock (38.4 MHz). PLLP operates at 408 MHz.

The PWM clock frequency is divided by 256 before subdividing it based on the programmable frequency division value to generate the required frequency for the PWM output. The maximum output frequency that can be achieved from this configuration is 408 MHz/256 = 1.6 MHz. This 1.6 MHz frequency can be further divided using the frequency divisor in PWM.

The OSC clock is the primary/default source for the PWM IP clock. For higher PWM output frequency requirements, PLLP is the clock source (up to 408 MHz).

Table 22: PWM Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
206	GPIO07	Pulse Width Modulator or GPIO #7	Bidir	CMOS – 1.8V
218	GPIO12	Pulse Width Modulator or GPIO #12	Bidir	CMOS – 1.8V
228	GPIO13	Pulse Width Modulator or GPIO #13	Bidir	CMOS – 1.8V
230	GPIO14	Pulse Width Modulator or GPIO #14	Bidir	CMOS – 1.8V

1.9 Deep Learning Accelerator (DLA)

The Deep Learning Accelerator (DLA) is a new fixed function engine used to accelerate inference operations on convolution neural networks (CNNs). The DLA supports accelerating some or all desired CNN layers such as convolution, activation, pooling, local response normalization, and full-connected layers.

Table 23: **DLA Clock**

Module	Power Mode	Max Frequency
Jetson Xavier NX	10W	900 MHz
	15W	1100 MHz
	20W	1100 MHz

DLA hardware is comprised of the following components:

1. Convolution Core – optimized high-performance convolution engine.
   Convolution operations work on two sets of data: one set of offline-trained “weights” (which remain constant between each run of inference), and one set of input “feature” data (which varies with the network’s input). The convolutional engine exposes parameters to map many different sizes of convolutions onto the hardware with high efficiency.
2. Single Data Point Processor – single-point lookup engine for activation functions.
   The Single Data Point Processor (SDP) allows for the application of both linear and non-linear functions onto individual data points. This is commonly used immediately after convolution in CNN systems. The SDP has a lookup table to implement non-linear functions, or for linear functions it supports simple bias and scaling. This combination can support most common activation functions, as well as other element-wise operations, including ReLU, PReLU, precision scaling, batch normalization, bias addition, or other complex non-linear functions, such as a sigmoid or a hyperbolic tangent.
3. Planar Data Processor – planar averaging engine for pooling.
   The Planar Data Processor (PDP) supports specific spatial operations that are common in CNN applications. It is configurable at runtime to support different pool group sizes, and supports three pooling functions: maximum-pooling, minimum-pooling, and average-pooling.
4. Cross-Channel Data Processor – multi-channel averaging engine for advanced normalization functions.
   The Cross-channel Data Processor (CDP) is a specialized unit built to apply the local response normalization (LRN) function – a special normalization function that operates on channel dimensions, as opposed to the spatial dimensions.
5. Data Reshape Engines – memory-to-memory transformation acceleration for tensor reshape and copy operations.
   The data reshape engine performs data format transformations (e.g., splitting or slicing, merging, contraction, reshape-transpose). Data in memory often needs to be reconfigured or reshaped in the process of performing inferencing on a convolutional network. For example, slice operations may be used to separate out different features or spatial regions of an image, while reshape-transpose operations (common in deconvolutional networks) create output data with larger dimensions than the input dataset.
6. Bridge DMA – accelerated path to move data between two non-connected memory systems.
   The bridge DMA (BDMA) module provides a data copy engine to move data between the system DRAM and the dedicated memory interface.

1.10 Programmable Vision Accelerator (PVA)

The Programmable Vision Accelerator (PVA) is an application-specific instruction vector processor that implements some of the common filter loops and other common computer vision algorithms such as Harris corners, stereo disparity, and more. Each PVA cluster consists of a Cortex-R5 core along with two dedicated vector processing units, each with its own memory and DMA. The PVA can be programmed to perform several pre-defined functions using the NVIDIA Vision Programming Interface (VPI) software library.

Table 24: PVA Clock Operation

Description	Power Mode	Operating Frequency
PVA_VPS Fmax	10W	550.4 MHz
	15W	819.2 MHz
	20W	819.2 MHz

2.0 Power and System Management

VIN must be supplied by the carrier board that the module is designed to connect to. All interfaces are referenced to on-module voltage rails, additional I/O voltage is not required to be supplied to the module. See the *Jetson Xavier NX Product Design Guide* for details on connecting to each of the interfaces.

Table 25: Power and System Control Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
251 252 253 254 255 256 257 258 259 260	VDD_IN	Main power – Supplies PMIC and other registers	Input	5.0V
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	1.65V-5.5V
233	SHUTDOWN_REQ*	Used by the module to request a shutdown from the carrier board. Pull up to VDD_IN with ~5kΩ (4.02k + 1k) on the module.	Output	CMOS – 5.0V
237	POWER_EN	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 100kΩ pulldown is also on the module.	Input	CMOS – 5.0V
239	SYS_RESET*	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. Pull up to 1.8V with 1kΩ resistor on the module.	Bidir	Open Drain, 1.8V
178	MOD_SLEEP*	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	Output	CMOS – 1.8V
210	CLK_32K_OUT	Sleep/Suspend clock	Output	CMOS – 1.8V
214	FORCE_RECOVERY*	Force Recovery strap pin	Input	CMOS – 1.8V
240	SLEEP/WAKE*	Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	Input	CMOS – 5.0V

2.1 Power Rails

VDD_IN must be supplied by the carrier board that the Jetson Xavier NX is designed to connect to. All Jetson Xavier NX interfaces are referenced to on-module voltage rails and no I/O voltage is required to be supplied to the module. See the *Jetson Xavier NX Product Design Guide* for details of connecting to each of the interfaces.

2.2 Power Domains/Islands

Jetson Xavier NX has a single three-channel INA that can measure power of CPU_GPU_CV combined rail, Core, and module input power.

2.3 Power Management Controller (PMC)

The PMC power management features enable both high speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the SoC as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC, USB) which can wake the system from deep sleep state. The PMC enables aggressive power-gating capabilities on idle modules and integrates specific logic to maintain defined states and control power domains during sleep and deep sleep modes.

2.4 Resets

If you assert reset, then the Jetson Xavier NX and onboard storage will be reset. This signal is also used for baseboard power sequencing.

2.5 PMIC_BBATT

An optional back up battery can be attached to the VCC_RTC module input to maintain the module real-time clock (RTC) when VIN is not present. This pin is connected directly to the onboard PMIC. Details of the types of backup cells that optionally can be connected are found in the PMIC manufacturer's data sheet. When a backup cell is connected to the PMIC, the RTC retains its contents and can be configured to charge the backup cell as well. RTC accuracy is 2 seconds/day.

The following backup cells may be attached to this pin:

- Super capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells

The backup cells must provide a voltage in the range 2.5V to 3.5V. These are charged with a constant current, and a constant voltage charger that can be configured between 2.5V and 3.5V (constant voltage) output and 50 uA to 800 uA (constant current).

Table 26: PMIC_BBAT Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
235	PMIC_BBAT	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	1.65V-5.5V

2.6 Power Sequencing

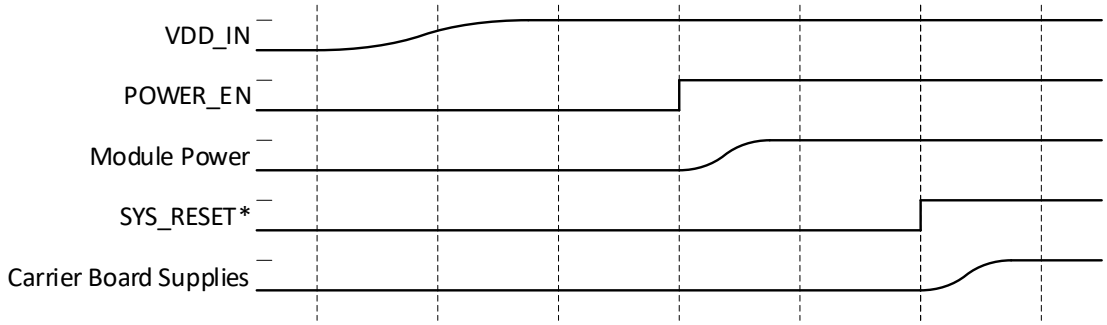
The Jetson Xavier NX is required to be powered on and off in a known sequence. Sequencing is determined through a set of control signals; the SYS_RESET* signal (when deasserted) is used to indicate when the carrier board can power on. The following sections provide an overview of the power sequencing steps between the carrier board and Jetson Xavier NX. Refer to the *Jetson Xavier NX Product Design Guide* for system level details on the application of power, power sequencing, and monitoring. The Jetson Xavier NX and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system.

2.6.1 Power Up

During power up, the carrier board must wait until the signal SYS_RESET* is deasserted from the Jetson module before enabling its power; the Jetson module will deassert the SYS_RESET* signal to enable the complete system to boot.

Note: I/O pins cannot be high (>0.5V) before SYS_RESET* goes high. When SYS_RESET* is low, the maximum voltage applied to any I/O pin is 0.5V.

Figure 3: Power-up Sequence

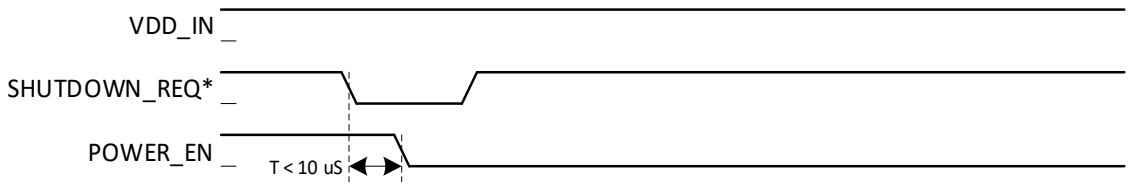


2.6.2 Power Down

Shutdown events can be triggered by either the module or the baseboard, but the shutdown event will always be serviced by the baseboard. To do so, the baseboard deasserts POWER_EN, which begins the shutdown power sequence on the module. If the module needs to request a shutdown event in the case of thermal, software, or under-voltage events, it will assert SHUTDOWN_REQ*. When the baseboard sees low SHUTDOWN_REQ*, it should deassert POWER_EN as soon as possible.

Once POWER_EN is deasserted, the module will assert SYS_RESET*, and the baseboard may shut down. SoC 3.3V I/O must reach 0.5V or lower at most 1.5ms after SYS_RESET* is asserted. SoC 1.8V I/O must reach 0.5V or lower at most 4ms after SYS_RESET* is asserted.

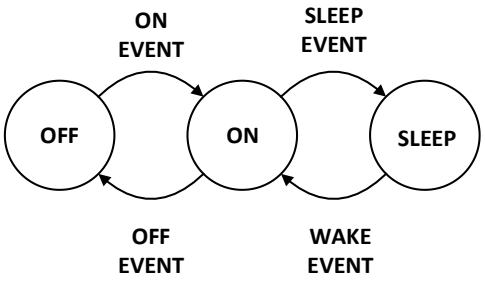
Figure 4: Power Down Sequence



2.7 Power States

The Jetson Xavier NX operates in three main power modes: OFF, ON, and SLEEP. The module transitions between these states are based on various events from hardware or software. Figure 5 shows the transitions between these three states.

Figure 5: Power State Transition Diagram



2.7.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state, the Jetson Xavier NX module is fully functional and operates normally. An ON event must occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_EN pin. This must occur with VDD_IN connected to a power rail and POWER_EN is asserted (at a logic1). The POWER_EN control is the carrier board indication to the Jetson module that the VDD_IN power is good. The carrier board should assert this high only when VDD_IN has reached its required voltage level and is stable. This prevents the Jetson Xavier NX Module from powering up until the VDD_IN power is stable.

2.7.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state, through an OFF event. OFF events are listed in the table below.

Table 27: OFF State Events

Event	Details	Preconditions
HW Shutdown	Set POWER_EN pin to zero for at least 100 µs, the internal PMIC starts the shutdown sequence.	In ON State
SW Shutdown	Software initiated shutdown	ON state, software operational
Thermal Shutdown	If the internal temperature of the Jetson Xavier NX module reaches an unsafe temperature, the hardware is designed to initiate a shutdown.	Any power state

Note: HW shutdown, SW shutdown, and Thermal shutdown will all assert SHUTDOWN_REQ* low. System on Module will not initiate power supply shutdown sequence until POWER_EN is deasserted. POWER_EN debounce is 1ms on Jetson Xavier NX.

2.7.3 SLEEP State

The SLEEP state can only be entered from the ON state. This state allows the module to quickly resume to an operational state without performing a full boot sequence. The SLEEP state also includes a low power mode SC7 (deep sleep) where the module operates only with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state the output signals from the module are maintained at their logic level prior to entering the state (i.e., they do not change to a 0V level). To exit the SLEEP state a WAKE event must occur; WAKE events can occur from within the module or from external devices through various pins on the module connector.

Table 28: SLEEP and WAKE Events

Event	Details
RTC WAKE up	Timers within the module can be programmed, on SLEEP entry. When these expire, they create a WAKE event to exit the SLEEP state.
Thermal Condition	If the module internal temperature exceeds programmed hot and cold limits the system is forced to wake up, so it can report and take appropriate action (shut down for example).
USB VBUS detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate.
SD Card detect	The card detect pin may be configured to enable the system to wake.
Module connector Interface WAKE signal	Programmable signals on the module connector.

2.8 Thermal and Power Monitoring

The Jetson Xavier NX is designed to operate under various workloads and environmental conditions. It has been designed so that an active or passive heat sink solution can be attached. The module contains various methods through hardware and software to limit the internal temperature to within operating limits. See the *Jetson Xavier NX Thermal Design Guide* for more details.

2.9 Overcurrent Throttling

The power monitor triggers CPU/GPU hardware throttling to keep power within budget.

- INA warning signals lite GPU throttling (50%) when VDD_IN average power (512 samples) exceeds 15W
- INA critical signal triggers lite CPU+GPU throttling (50%) when VDD_IN instantaneous power exceeds 18W

3.0 Pin Definitions

The function(s) for each pin on the module is fixed to a single Special-Function I/O (SFIO) or software-controlled General Purpose I/O (GPIO). The Jetson Xavier NX has multiple dedicated GPIOs and each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls. SFIO and GPIO functionality is configured using Multi-Purpose I/O (MPIO) pads with each MPIO pad consisting of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either Schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pads are partitioned into multiple pad control groups with controls being configured for the group. During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the *Jetson Xavier NX Product Design Guide* for more information.

3.1 Power-on Reset Behavior

Each MPIO pad has a deterministic power-on reset (PoR) state. The reset state for each pad is chosen to minimize the need of additional on-board components; for example, on-chip weak pull-ups are enabled during PoR for pads which are usually used to drive active-low chip selects eliminating the need for additional pull-up resistors.

The following list is a simplified description of the Jetson Xavier NX boot process focusing on those aspects which relate to the MPIO pins:

- System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET_N.
- The boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device (QSPI).
- The boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
- If the BCT and boot loader are fetched successfully, the boot ROM transfers control to the boot loader.
- Otherwise, the boot ROM enters USB recovery mode.

3.2 Sleep Behavior

Sleep is an ultra-low-power standby state in which the module maintains much of its I/O state while most of the chip is powered off. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering DPD is same across pads.

MPIO pads can vary during deep sleep. They differ regarding:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a GPIO wake event, OR
  - Enabled for some other purpose (e.g., a clock request pin)
- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Pads that do not enter deep sleep
  - Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep any time.

3.3 GPIO

The Jetson Xavier NX has multiple dedicated GPIOs. Each GPIO can be individually configurable as an Output, Input, or Interrupt source with level/edge controls. The pins listed in the following table are dedicated GPIOs; some with alternate SFIO functionality. Many other pins not included in this list are capable of being configured as GPIOs instead of the SFIO functionality the pin name suggests (e.g., UART, SPI, I^2S, etc.). All pins that can support GPIO functionality have this exposed in the Pinmux.

Table 29: GPIO Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
87	GPIO00	GPIO #0 or USB 0 VBUS Enable #0	Bidir	CMOS – 1.8V
118	GPIO01	GPIO #1 or Generic Clocks	Bidir	CMOS – 1.8V
124	GPIO02	GPIO #2	Bidir	CMOS – 1.8V
126	GPIO03	GPIO #3	Bidir	CMOS – 1.8V
127	GPIO04	GPIO #4	Bidir	CMOS – 1.8V
128	GPIO05	GPIO #5	Bidir	CMOS – 1.8V
130	GPIO06	GPIO #6	Bidir	CMOS – 1.8V
206	GPIO07	GPIO #7 or Pulse Width Modulator	Bidir	CMOS – 1.8V
208	GPIO08	GPIO #8 or Fan Tachometer	Bidir	CMOS – 1.8V
211	GPIO09	GPIO #9 or Audio Codec Master Clock	Bidir	CMOS – 1.8V
212	GPIO10	GPIO #10	Bidir	CMOS – 1.8V
216	GPIO11	GPIO #11 or Generic Clocks	Bidir	CMOS – 1.8V
218	GPIO12	GPIO #12 or Pulse Width Modulator	Bidir	CMOS – 1.8V
228	GPIO13	GPIO #13 or Pulse Width Modulator	Bidir	CMOS – 1.8V
230	GPIO14	GPIO #14 or Pulse Width Modulator	Bidir	CMOS – 1.8V

3.4 Pin List

Signal Name	Pin # Top Odd		Pin # Bottom Even	Signal Name
GND	1		2	GND
CSI1_D0_N	3		4	CSI0_D0_N
CSI1_D0_P	5		6	CSI0_D0_P
GND	7		8	GND
CSI1_CLK_N	9		10	CSI0_CLK_N
CSI1_CLK_P	11		12	CSI0_CLK_P
GND	13		14	GND
CSI1_D1_N	15		16	CSI0_D1_N
CSI1_D1_P	17		18	CSI0_D1_P
GND	19		20	GND
CSI3_D0_N	21		22	CSI2_D0_N
CSI3_D0_P	23		24	CSI2_D0_P
GND	25		26	GND
CSI3_CLK_N	27		28	CSI2_CLK_N
CSI3_CLK_P	29		30	CSI2_CLK_P
GND	31		32	GND
CSI3_D1_N	33		34	CSI2_D1_N
CSI3_D1_P	35		36	CSI2_D1_P
GND	37		38	GND
DP0_TXD0_N	39		40	CSI4_D2_N
DP0_TXD0_P	41		42	CSI4_D2_P
GND	43		44	GND
DP0_TXD1_N	45		46	CSI4_D0_N
DP0_TXD1_P	47		48	CSI4_D0_P
GND	49		50	GND
DP0_TXD2_N	51		52	CSI4_CLK_N
DP0_TXD2_P	53		54	CSI4_CLK_P
GND	55		56	GND
DP0_TXD3_N	57		58	CSI4_D1_N
DP0_TXD3_P	59		60	CSI4_D1_P
GND	61		62	GND
DP1_TXD0_N	63		64	CSI4_D3_N
DP1_TXD0_P	65		66	CSI4_D3_P
GND	67		68	GND
DP1_TXD1_N	69		70	DSI_D0_N
DP1_TXD1_P	71		72	DSI_D0_P
GND	73		74	GND
DP1_TXD2_N	75		76	DSI_CLK_N
DP1_TXD2_P	77		78	DSI_CLK_P
GND	79		80	GND
DP1_TXD3_N	81		82	DSI_D1_N
DP1_TXD3_P	83		84	DSI_D1_P
GND	85		86	GND
GPIO00	87		88	DP0_HPD
SPI0_MOSI	89		90	DP0_AUX_N
SPI0_SCK	91		92	DP0_AUX_P
SPI0_MISO	93		94	HDMI_CEC
SPI0_CS0*	95		96	DP1_HPD
SPI0_CS1*	97		98	DP1_AUX_N
UART0_TXD	99		100	DP1_AUX_P
UART0_RXD	101		102	GND
UART0_RTS*	103		104	SPI1_MOSI
UART0_CTS*	105		106	SPI1_SCK
GND	107		108	SPI1_MISO
USB0_D_N	109		110	SPI1_CS0*
USB0_D_P	111		112	SPI1_CS1*
GND	113		114	CAM0_PWDN
USB1_D_N	115		116	CAM0_MCLK
USB1_D_P	117		118	GPIO01
GND	119		120	CAM1_PWDN
USB2_D_N	121		122	CAM1_MCLK
USB2_D_P	123		124	GPIO02
GND	125		126	GPIO03
GPIO04	127		128	GPIO05
GND	129		130	GPIO06
PCIE0_RX0_N	131		132	GND

Signal Name	Pin # Top Odd		Pin # Bottom Even	Signal Name
PCIE0_RX0_P	133		134	PCIE0_TX0_N
GND	135		136	PCIE0_TX0_P
PCIE0_RX1_N	137		138	GND
PCIE0_RX1_P	139		140	PCIE0_TX1_N
GND	141		142	PCIE0_TX1_P
CAN_RX	143		144	GND
CAN_TX	145		146	GND
GND	147		148	PCIE0_TX2_N
PCIE0_RX2_N	149		150	PCIE0_TX2_P
PCIE0_RX2_P	151		152	GND
GND	153		154	PCIE0_TX3_N
PCIE0_RX3_N	155		156	PCIE0_TX3_P
PCIE0_RX3_P	157		158	GND
GND	159		160	PCIE0_CLK_N
USBSS_RX_N	161		162	PCIE0_CLK_P
USBSS_RX_P	163		164	GND
GND	165		166	USBSS_TX_N
PCIE1_RX0_N	167		168	USBSS_TX_P
PCIE1_RX0_P	169		170	GND
GND	171		172	PCIE1_TX0_N
PCIE1_CLK_N	173		174	PCIE1_TX0_P
PCIE1_CLK_P	175		176	GND
GND	177		178	MOD_SLEEP*
PCIE_WAKE*	179		180	PCIE0_CLKREQ*
PCIE0_RST*	181		182	PCIE1_CLKREQ*
PCIE1_RST*	183		184	GBE_MDI0_N
I2C0_SCL	185		186	GBE_MDI0_P
I2C0_SDA	187		188	GBE_LED_LINK
I2C1_SCL	189		190	GBE_MDI1_N
I2C1_SDA	191		192	GBE_MDI1_P
I2S0_DOUT	193		194	GBE_LED_ACT
I2S0_DIN	195		196	GBE_MDI2_N
I2S0_FS	197		198	GBE_MDI2_P
I2S0_SCLK	199		200	GND
GND	201		202	GBE_MDI3_N
UART1_TXD	203		204	GBE_MDI3_P
UART1_RXD	205		206	GPIO07
UART1_RTS*	207		208	GPIO08
UART1_CTS*	209		210	CLK_32K_OUT
GPIO09	211		212	GPIO10
CAM_I2C_SCL	213		214	FORCE_RECOVERY*
CAM_I2C_SDA	215		216	GPIO11
GND	217		218	GPIO12
SDMMC_DAT0	219		220	I2S1_DOUT
SDMMC_DAT1	221		222	I2S1_DIN
SDMMC_DAT2	223		224	I2S1_FS
SDMMC_DAT3	225		226	I2S1_SCLK
SDMMC_CMD	227		228	GPIO13
SDMMC_CLK	229		230	GPIO14
GND	231		232	I2C2_SCL
SHUTDOWN_REQ*	233		234	I2C2_SDA
PMIC_BBAT	235		236	UART2_TXD
POWER_EN	237		238	UART2_RXD
SYS_RESET*	239		240	SLEEP/WAKE*
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VDD_IN	251		252	VDD_IN
VDD_IN	253		254	VDD_IN
VDD_IN	255		256	VDD_IN
VDD_IN	257		258	VDD_IN
VDD_IN	259		260	VDD_IN

4.0 DC Characteristics

4.1 Operating and Absolute Maximum Ratings

The parameters listed in following table are specific to a temperature range and operating voltage. Operating the Jetson Xavier NX beyond these parameters is not recommended.

WARNING: Exceeding the listed conditions may damage and/or affect long-term reliability of the part. The Jetson Xavier NX module should never be subjected to conditions extending beyond the ratings listed below.

Table 30: Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_{DC}	VDD_IN	4.75	5.0	5.25	V
	PMIC_BBAT	1.65	-	5.5	V

Absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, performance is not guaranteed, and device reliability may be affected. It is not recommended to operate the Jetson Xavier NX module under these conditions.

Table 31: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
VDD_{MAX}	VDD_IN	-0.5	5.5	V	
	PMIC_BBAT	-0.3	6.0	V	
IDD_{MAX}	VDD_IN I_{max}	-	5	A	
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	VDD + 0.5V when CARRIER_PWR_ON high and associated I/O rail powered. I/O pins cannot be high (>0.5V) before CARRIER_PWR_ON goes high. When CARRIER_PWR_ON is low, the maximum voltage applied to any I/O pin is 0.5V
	DD pins configured as open drain	-0.5	3.63	V	The pin's output-driver must be set to open-drain mode
T_{OP}	Operating Temperature	-25	See Note	°C	See the *Jetson Xavier NX Thermal Design Guide* for details.
T_{STG}	Storage Temperature (ambient)	-40	80	°C	
M_{MAX}	Mounting Force	-	8.2	kgf[1]	Maximum force applied to PCB. See the *Jetson Xavier NX Thermal Design Guide* for additional details on mounting a thermal solution.

Note: kgf stands for kilogram-force.

Table 32: Jetson NX Reliability Report

Test	Conditions	Reference Standard	Results
Temperature Humidity Biased	85°C / 85% RH, 168 hours, Power ON	JESD22-A101	PASS
Temperature Cycling	-40°C to 105°C, 250 cycles, non-operational	JESD22-A104, IPC9701	PASS
Temp/Humidity Cycle	25°C to 65°C, 93% RH, six cycles	NV Standard	PASS
Mechanical Shock – 140G Non-Op	140G, half sine, one shock/orientation, six orientations total, non-operational	JESD22-B110	PASS
Mechanical Shock – 50G Op	50G, half sine, three shocks/orientation, six orientations total, operational	IEC 600068 2-27	PASS
Connector Insertion Cycling	Insert/Withdraw Connector, 30 cycles	EIA-364	PASS
Sine Vibration – 3G	3G, 10-500 Hz, two sweep/axis, three axes total, non-operational	IEC60068-2-6	PASS
Random Vibration – 2G Non-Op	10-500 Hz, two Grms, one hour/axis, non-operational	IEC60068-2-64	PASS
Random Vibration – 1G Op	10-500 Hz, 1 Grms, 30 min/axis, operational	IEC60068-2-64	PASS
Hard Boot	Power ON/OFF, ON for 150 sec OFF for 30 sec 2000 cycles at 25°C 1000 cycles at -5°C 1000 cycles at 45°C	NV Standard	PASS
Operational Low Temp	-5°C, 24 hours, operational	NV Standard	PASS
Operational High Temp	45°C, 90%RH, 336 hours, operational	NV Standard	PASS
MTBF / Failure Rate	Controlled Environment (GB), T = 35°C, CL = 90%	Telcordia SR-332, ISSUE 3 Parts Count (Method I)	2,629,471 hours
MTBF / Failure Rate	Uncontrolled Environment (GF) T = 35°C, CL = 90%	Telcordia SR-332, ISSUE 3 Parts Count (Method I)	1,493,890 hours

4.2 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 33: CMOS Pin Type DC Characteristics

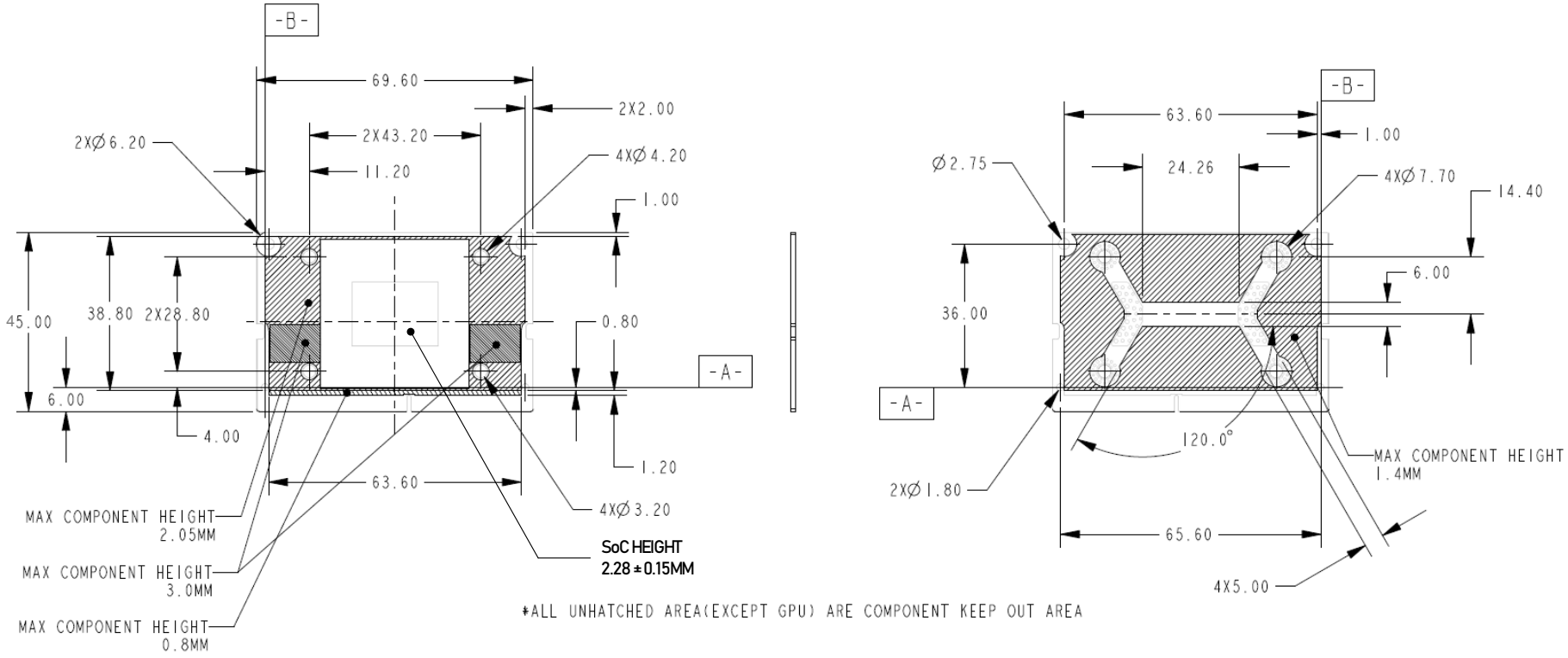
Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	-	V

Table 34: Open Drain Pin Type DC Characteristics

Symbol	Description	Minimum	Maximum	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	-	0.15 x VDD	V
	I^2C [1,0] Output Low Voltage (I_{OL} = 2mA) (see note)	-	0.3 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	-	V

Note: I2C[1,0]_[SCL, SDA] pins pull-up to 3.3V through on module 2.2kΩ resistor. I2C2_[SCL, SDA] pins pull-up to 1.8V through on module 2.2kΩ resistor.

5.0 Package Drawing and Dimensions



Note:

- All dimensions are in millimeters unless otherwise specified.
- Tolerances are: .X ± 0.25, .XX ± is 0.1, Angle ± is 1°

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