NVIDIA Jetson Xavier NX

Design Guide

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Document History

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Version	Date	Description of Change
0.9	November 6, 2019	Preliminary Information
0.91	February 7, 2020	• Updated Table 2-2 • Removed >1 min recommendation for power rail charging • Updated Table 3-1 • Added PCIe x1 interface support for Root Port operation • Updated Table 4-1 • Corrected controller # for PCIE0 pins, updated x1 PCIe to come from Xavier PEX Lane 11, and updated PEX lane changes in Table 4-2 • Updated Table 4-3 • Updated USB2 pin numbers and removed 4.7uF cap on VDD_5V_USB to match P3509 implementation in Figure 4-1 • Moved PCIe x1 to Lane 11, corrected PCIE0_TX3 and RX0 pin numbers, corrected x4 controller, and removed AC cap values on TX lines in Figure 4-8 • Corrected controller # or x4 PCIe I/F, removed AC cap values on TX lines, and corrected PCIE0_TX3 and RX0 pin numbers in Figure 4-9 • Updated PCIe controller numbers in Table 4-10 • Changed pull ups on RST and INT to go to 3.3V and added level shifter to INT to SoC in Figure 4-10 • Updated ethernet connections in Table 4-13 • Updated DP_AUX_CH0_N and DP_AUX_CH0_N pin type since the interface can be used for HDMI in Table 5-1 • Updated with 100Kohm PD and series resistors on DPx_HPD on connector side of level shifter in Figure 5-1 • Updated DPx_HPD pin termination description in Table 5-4 • Updated notes to Table 7-1 • Updated notes to Table 8-1 • Updated Figure 8-1 with Jetson module • Corrected PM3_PWM3 to GP_PWM6 in the fan section, Section 9.5 • Corrected the Xavier signal connected GPIO14 pin in Table 9-12 and Figure 9-7 • Updated TX and RX to match module name in Table 9-13 • Updated checklist Table 12-1 • Updated Table 13-1 • Updated Table 13-2
0.92	March 23, 2020	• Removed PMIC part # from Figure 2-1 • Added new chapter on module connector (Chapter 3) • Added note to Section 5.1 "USB"

Version	Date	Description of Change
		• Updated Section 5.2 "PCIe" • Updated Figure 5-9 and the note to include open-drain buffers on the control signals when NX is an Endpoint • Updated the notes to Table 5-9 • Updated Table 5-10 • Updated eDP and DP pin descriptions in Table 6-1 • Removed series resistor after the level shifter and added related note to Figure 6-1 • Removed resistor divider on HPD in Figure 6-7 • Removed GPIO08 for card select mention in Table 8-1 • Updated Figure 8-1 with the following: moved load switch enable to GPIO, moved card detect to generic GPIO, and removed series resistor on card detect line • Updated Table 8-3 with generic GPIO • Replaced FET circuit used for level shifters with generic level shifter blocks in Figure 10-7 • Removed design checklist and pin descriptions tables and made them separate attachments to this design guide
1.0	April 21, 2020	• Added note to Table 4-1 regarding direction of CLK_32K_OUT signal • Added note to Table 5-2 regarding PEX_L4_RST* and PCIE_WAKE* signals • Updated Section 5.2 on PCIe • Added Table 5-10 on PCIe Gen4 routing requirements • Added note to Table 6-1 regarding DP_AUX_CH[1:0]_HPD direction • Added note to Table 7-2 regarding CAM[1:0]_MCLK and CAM[1:0]_PWDN direction • Added note to Table 8-1 regarding SDMMC_CLK direction • Added note to Table 9-1 regarding I2S[1:0]_DOUT and _DIN direction • Added note to Table 10-7 regarding UART pins • Updated Figure 10-5 to show on module buffers and added related note • Added note to Table 10-9 regarding CAN signals • Added note to Table 10-12 regarding GPIO014 and GPIO008 direction • Updated attachments
1.1	May 7, 2020	• Updated Table 5-5 with the following: Updated Gen1 and Gen2 values Removed redundant GND via reference requirement and accompanying note Added Gen2 specific requirements to ESD • Updated Table 6-5 with max trace lengths (more relaxed) and PTH vias (more restrictive) • Updated Table 7-4 with the following: Removed max loading spec

Version	Date	Description of Change
		Removed "loosely coupled diff pair" comment from Intra pair requirement note Updated max trace delays and added max trace lengths Added max insertion loss Changed max DQ to CLK skew for 1 Gbps
1.2	August 13, 2020	• Added new chapter on developer kit feature considerations (Chapter 3) • Removed note related to CLK_32K_OUT in Table 5-1 • Updated length/skew in Table 6-9 and Table 6-10 • Added Figure 6-10 and Figure 6-11 on s-parameter plots (SDD21 and SD11) • Updated Figure 9-1 and notes related to the VDD supply enable and current limiting • Removed reference to CAM_I2C used for on module power monitor in Section 11.1.1 • Removed mention of SPI2 pins in Table 11-6 • Added bring-up checklist attachment (See reference in Chapter 14) • Updated design checklist and full pin description attachments
1.3	November 4, 2020	• Updated USB SS hub design with publicly available part number in Section 3.2 • Added to note to clarify PCIe clock output and REFCLK input signaling type to Figure 6-8 and Figure 6-9 • Removed note under Figure 8-3 about CAM_I2C connection to on-module power monitor • Updated Table 8-4 based on new guidelines from IOSI after they used improved model • Updated Figure 10-1 with simpler more generic example of audio codec connection • Added Section 11.7 on USB recovery mode
1.4	August 12, 2021	• Updated block diagram Figure 2-1 • Added notes to Table 5-1 • Updated power supply and sequencing information in Section 5.1 • Updated Section 6.1 on USB • Updated USB 2.0 signal connections in Table 6-7 • Made "Gigabit Ethernet" section its own chapter (Chapter 7) • Added section on test points for high-speed interfaces (Section 17.6) • Updated pin description attachment

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow to create a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson™ Xavier™ NX System-on-Module (SOM).

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

1.1 References

Refer to the following list of documents or models for more information. Use the latest revision of all documents.

- Jetson Xavier NX Data Sheet
- Xavier (SoC) Technical Reference Manual
- Jetson Xavier NX Module Pinmux
- Jetson Xavier NX Thermal Design Guide
- Jetson Xavier NX SCL (Supported Component List)

1.2 Abbreviations and Definitions

Table 1-1 lists the abbreviations that may be used throughout this design and guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CAN	Controller Area Network
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
DP	DisplayPort

Abbreviation	Definition
eDP	Embedded DisplayPort
ESD	Electrostatic Discharge
eMMC	Embedded MMC
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LPDDR4x	Low Power Double Data Rate DRAM, Fourth generation
MDI	Medium-Dependent Interface
MIL	1/1000th of an inch
MIPI	Mobile Industry Processor Interface
mm	Millimeter
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
ps	Pico-Seconds
PMIC	Power Management Integrated Circuit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock
SD Card	Secure Digital Card
SDIO	Secure Digital I/O Interface
SE	Single-Ended
SPI	Serial Peripheral Interface
TMDS	Transition-Minimized Differential Signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Chapter 2. Jetson Xavier NX

The Jetson Xavier NX resides at the center of the embedded system solution and includes:

- Power (PMIC/Regulators, etc.)
- DRAM (8 GB, 128-bit LPDDR4x)
- eMMC (16 GB)
- Gigabit Ethernet Controller
- Power Monitor
- QSPI NOR (32 MB – Boot device)

In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown in Table 2-1 and Figure 2-1.

Table 2-1. Jetson Xavier NX Interfaces

Category	Function		Category	Function
USB	USB 2.0 interface (3x)		LAN	Gigabit ethernet
	USB 3.1 (1x)		I2C	4x
PCIe	PCIe (x1 and x4)		UART	3x
Camera	CSI (14 lanes 3 x4 + 1 x2 or 6 x2)		SPI	2x
	Control, clock		CAN	1x
Display	HDMI/eDP/DP (2x)		Wi-Fi/BT/Modem	PCIe/UART/I2S, control/handshake
	DP_AUX/HPD (2x), CEC (1x)		Fan	FAN PWM and tach input
Audio	I2S interface (2x) and clock		Debug	UART
	Master clock		System	Power control, reset, alerts
SD Card/SDIO	SD Card or SDIO interface (1x)		Power	Main input and battery back-up for RTC

Figure 2-1. Jetson Xavier NX Block Diagram

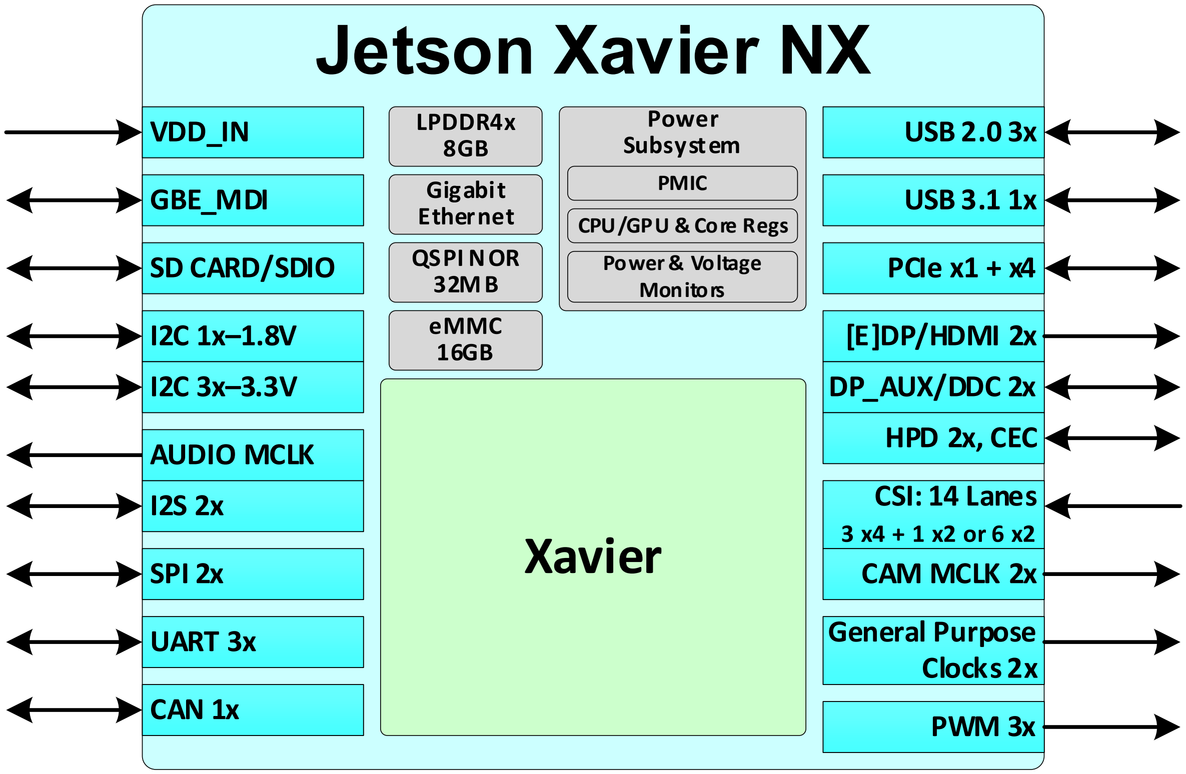


Table 2-2. Jetson Xavier NX Connector (260-Pin SO-DIMM) Pin Out Matrix

Module Signal Name	Pin #		Pin #	Module Signal Name
GND	1		2	GND
CSI1_D0_N	3		4	CSI0_D0_N
CSI1_D0_P	5		6	CSI0_D0_P
GND	7		8	GND
CSI1_CLK_N	9		10	CSI0_CLK_N
CSI1_CLK_P	11		12	CSI0_CLK_P
GND	13		14	GND
CSI1_D1_N	15		16	CSI0_D1_N
CSI1_D1_P	17		18	CSI0_D1_P
GND	19		20	GND
CSI3_D0_N	21		22	CSI2_D0_N
CSI3_D0_P	23		24	CSI2_D0_P
GND	25		26	GND
CSI3_CLK_N	27		28	CSI2_CLK_N
CSI3_CLK_P	29		30	CSI2_CLK_P
GND	31		32	GND
CSI3_D1_N	33		34	CSI2_D1_N
CSI3_D1_P	35		36	CSI2_D1_P
GND	37		38	GND
DP0_TXD0_N	39		40	CSI4_D2_N
DP0_TXD0_P	41		42	CSI4_D2_P
GND	43		44	GND
DP0_TXD1_N	45		46	CSI4_D0_N
DP0_TXD1_P	47		48	CSI4_D0_P
GND	49		50	GND
DP0_TXD2_N	51		52	CSI4_CLK_N
DP0_TXD2_P	53		54	CSI4_CLK_P
GND	55		56	GND
DP0_TXD3_N	57		58	CSI4_D1_N
DP0_TXD3_P	59		60	CSI4_D1_P
GND	61		62	GND
DP1_TXD0_N	63		64	CSI4_D3_N
DP1_TXD0_P	65		66	CSI4_D3_P
GND	67		68	GND
DP1_TXD1_N	69		70	DSI_D0_N
DP1_TXD1_P	71		72	DSI_D0_P
GND	73		74	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
PCIE0_RX0_P	133		134	PCIE0_TX0_N
GND	135		136	PCIE0_TX0_P
PCIE0_RX1_N	137		138	GND
PCIE0_RX1_P	139		140	PCIE0_TX1_N
GND	141		142	PCIE0_TX1_P
CAN_RX	143		144	GND
KEY	KEY		KEY	KEY
CAN_TX	145		146	GND
GND	147		148	PCIE0_TX2_N
PCIE0_RX2_N	149		150	PCIE0_TX2_P
PCIE0_RX2_P	151		152	GND
GND	153		154	PCIE0_TX3_N
PCIE0_RX3_N	155		156	PCIE0_TX3_P
PCIE0_RX3_P	157		158	GND
GND	159		160	PCIE0_CLK_N
USBSS_RX_N	161		162	PCIE0_CLK_P
USBSS_RX_P	163		164	GND
GND	165		166	USBSS_TX_N
PCIE1_RX0_N	167		168	USBSS_TX_P
PCIE1_RX0_P	169		170	GND
GND	171		172	PCIE1_TX0_N
PCIE1_CLK_N	173		174	PCIE1_TX0_P
PCIE1_CLK_P	175		176	GND
GND	177		178	MOD_SLEEP*
PCIE_WAKE*	179		180	PCIE0_CLKREQ*
PCIE0_RST*	181		182	PCIE1_CLKREQ*
PCIE1_RST*	183		184	GBE_MDI0_N
I2C0_SCL	185		186	GBE_MDI0_P
I2C0_SDA	187		188	GBE_LED_LINK
I2C1_SCL	189		190	GBE_MDI1_N
I2C1_SDA	191		192	GBE_MDI1_P
I2S0_DOUT	193		194	GBE_LED_ACT
I2S0_DIN	195		196	GBE_MDI2_N
I2S0_FS	197		198	GBE_MDI2_P
I2S0_SCLK	199		200	GND
GND	201		202	GBE_MDI3_N
UART1_TXD	203		204	GBE_MDI3_P

Module Signal Name	Pin #		Pin #	Module Signal Name
DP1_TXD2_N	75		76	DSI_CLK_N
DP1_TXD2_P	77		78	DSI_CLK_P
GND	79		80	GND
DP1_TXD3_N	81		82	DSI_D1_N
DP1_TXD3_P	83		84	DSI_D1_P
GND	85		86	GND
GPIO00	87		88	DP0_HPD
SPI0_MOSI	89		90	DP0_AUX_N
SPI0_SCK	91		92	DP0_AUX_P
SPI0_MISO	93		94	HDMI_CEC
SPI0_CS0*	95		96	DP1_HPD
SPI0_CS1*	97		98	DP1_AUX_N
UART0_TXD	99		100	DP1_AUX_P
UART0_RXD	101		102	GND
UART0_RTS*	103		104	SPI1_MOSI
UART0_CTS*	105		106	SPI1_SCK
GND	107		108	SPI1_MISO
USB0_D_N	109		110	SPI1_CS0*
USB0_D_P	111		112	SPI1_CS1*
GND	113		114	CAM0_PWDN
USB1_D_N	115		116	CAM0_MCLK
USB1_D_P	117		118	GPIO01
GND	119		120	CAM1_PWDN
USB2_D_N	121		122	CAM1_MCLK
USB2_D_P	123		124	GPIO02
GND	125		126	GPIO03
GPIO04	127		128	GPIO05
GND	129		130	GPIO06
PCIE0_RX0_N	131		132	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
UART1_RXD	205		206	GPIO07
UART1_RTS*	207		208	GPIO08
UART1_CTS*	209		210	CLK_32K_OUT
GPIO09	211		212	GPIO10
CAM_I2C_SCL	213		214	FORCE_RECOVERY*
CAM_I2C_SDA	215		216	GPIO11
GND	217		218	GPIO12
SDMMC_DAT0	219		220	I2S1_DOUT
SDMMC_DAT1	221		222	I2S1_DIN
SDMMC_DAT2	223		224	I2S1_FS
SDMMC_DAT3	225		226	I2S1_SCLK
SDMMC_CMD	227		228	GPIO13
SDMMC_CLK	229		230	GPIO14
GND	231		232	I2C2_SCL
SHUTDOWN_REQ*	233		234	I2C2_SDA
PMIC_BBAT	235		236	UART2_TXD
POWER_EN	237		238	UART2_RXD
SYS_RESET*	239		240	SLEEP/WAKE*
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VDD_IN	251		252	VDD_IN
VDD_IN	253		254	VDD_IN
VDD_IN	255		256	VDD_IN
VDD_IN	257		258	VDD_IN
VDD_IN	259		260	VDD_IN

Legend		
	Ground	Power

Chapter 3. Developer Kit Feature Considerations

The Jetson Xavier NX Developer Kit Carrier Board design files are provided as a reference design. This chapter describes details necessary for designers to know to replicate certain features if desired. In addition, aspects of the design that are specific to the NVIDIA Developer Kit usage but not useful or supported on a custom carrier board are also identified.

Most of the features implemented on the Jetson Xavier NX Developer Kit carrier board design can be duplicated by copying the connections from the P3509 carrier board reference design. Some of the following features have aspects that would require additional information.

- Button Power MCU (EFM8SB10F2G)
- USB SuperSpeed Hub (Realtek RTS5489)
- Power over Ethernet (PoE)
- TI TXB0108 level shifters
- ID EEPROM (Not to be copied from reference design)

3.1 Button Power MCU

The Developer Kit carrier board implements a button power MCU (EFM8SB10F2G). This device is programmed with firmware that is available on the Jetson Download Center. The posting is titled "Jetson AGX Xavier and Jetson Xavier NX Power Button Supervisor Firmware." The connections used on the reference design must be followed exactly and the firmware provided must be used to ensure correct functionality.

3.2 USB SuperSpeed Hub

The USB SS hub design uses a Realtek RTS5420 device. The hub circuit includes a SPI FLASH device which holds configuration information. A design intending to duplicate the developer kit hub implementation should include the same SPI FLASH programmed to match, or the hub should be customized with fuses with the same settings. The configuration in the SPI FLASH includes the following:

- Power enables (DPS1/2/3/4_PWR) set to be active high
- Charging feature disabled
- SSC valid

3.3 Power over Ethernet

The P3509 carrier board includes a 4-pin Power over Ethernet (PoE) header (J19) which brings out the VC power pins of the Ethernet connector. In order to use this alternate PoE power mechanism to power a custom carrier board, the design would require a power converter to take the high voltage PoE supply (38V-60V) and convert it to the correct voltage for the custom carrier board.

3.4 TI TXB0108 Level Shifters

The P3509 carrier board uses these level shifters to shift many of the signals going to the 40-pin header from 1.8V to 3.3V. The design of these level shifters supports bidirectional signaling without the use of a direction signal but has some side effects that should be considered. See the *Jetson Nano Developer Kit 40-Pin Expansion Header GPIO Usage Considerations Applications Note* for details.

3.5 Features Not to be Implemented

The Jetson Xavier NX Developer Kit carrier board features that should not be copied as they are not required or useful for a custom carrier board design. The ID EEPROM (P3509 - U17) is a feature that is used for NVIDIA internal purposes, but not useful on a custom design. A similar function may be desired for a custom design, but the NVIDIA software will not interact with these devices and the I2C address used by the developer kit carrier board ID EEPROM on the I2C2 interface (7'h57) should be avoided.

Chapter 4. Modular Connector

4.1 Module Connector Details

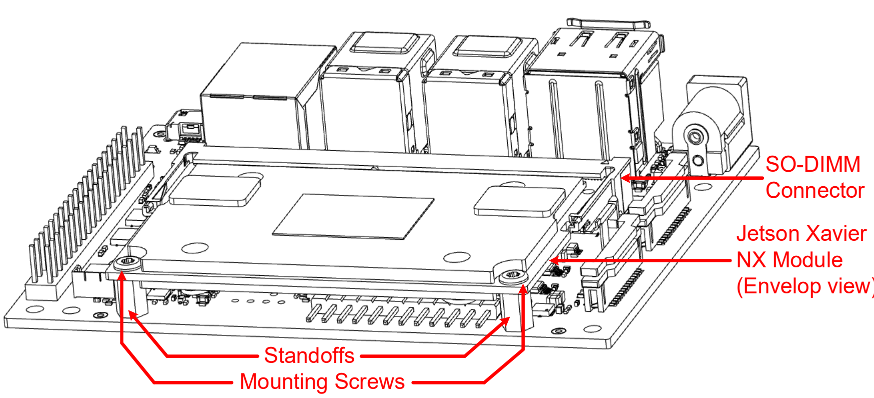
Jetson Xavier NX modules connect to the carrier board using a 260-pin SODIMM connector. The mating connector used on the developer kit carrier board is listed in the Jetson Xavier NX SCL (Supported Components List). This connector is a DDR4 SODIMM, 260-pin, right-angle, standard key type. The full height of the connector is 9.2 mm. Refer to the connector specification for details. Other heights are available.

4.2 Module to Mounting Hardware

The Jetson Xavier NX module is installed in the SODIMM connector which has latching mechanisms to hold the board in place. In addition, it is required that the module is mounted to the main carrier board PCB using metal standoffs and screws (or equivalent), both for mechanical integrity and to provide additional grounding points. The developer kit uses threaded standoffs that are hex, 4.5 mm widths (narrow diameter) x 6.57 ± 0.1 mm length. These have M2.5 threads. The screws used are M2.5 x 3.7 mm, pad head.

Other SODIMM connector heights are available. If a different height connector is used, the standoff height will have to be adjusted accordingly to account for the difference in height from main PCB to module PCB.

Figure 4-1. Jetson Xavier NX Module Installed in SODIMM Connector



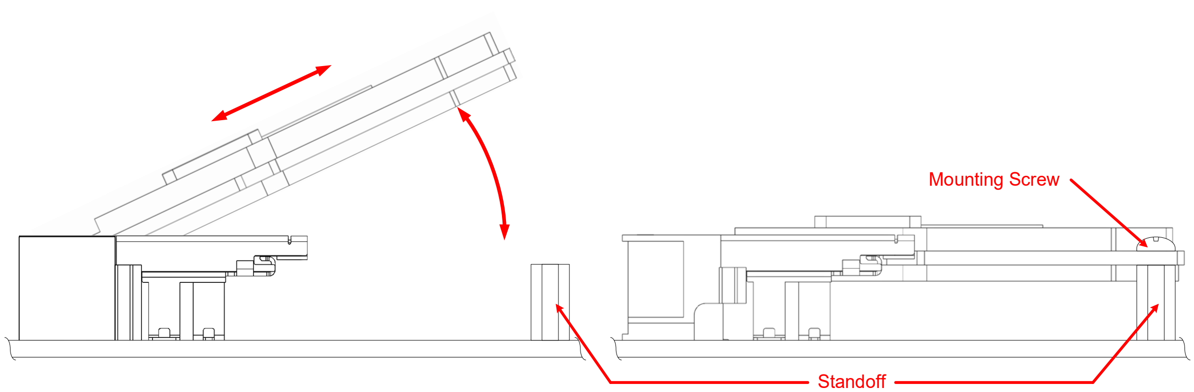
4.3 Module Installation and Removal

To install the Jetson Xavier NX module correctly, follow the sequence and mounting hardware instructions:

Here are some suggested assembly guidelines.

1. Assemble any required thermal solution on the module.
2. Install the module
   a) Start with baseboard that has suitable standoff to match SODIMM connector height.
   b) Insert module fully at an angle of 25-35 degree into the SODIMM connector.
   c) Arc down the module board until the SODIMM connector latch engages.
   d) Secure the module to the baseboard with screws into the standoff/spacer. The developer kit (shown in Figure 3 2) uses a standoff and screws to secure the module to the system/base- board.

Figure 4-2. Module to Connector Assembly Diagram



To remove the module correctly, follow the reverse of the installation sequence.

Chapter 5. Power

Power for the module is supplied on the **VDD_IN** pins and is nominally 5.0V (see the Jetson Xavier NX Data Sheet for supply tolerance and maximum current).

> ! CAUTION: Jetson Xavier NX is not hot-pluggable. Before installing or removing the module, the main power supply (to VDD_IN pins) must be disconnected and adequate time allowed for the various power rails to fully discharge.

Table 5-1. Jetson Xavier NX Power and System Pin Description

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type
251 ↓ 260	VDD_IN	–	Main power – Supplies PMIC and other regulators	Main DC input	Input	5.0V
235	PMIC_BBAT	–	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power. Charging is enabled by default in software. If non-rechargeable battery is to be used, charging should be disabled.	Battery Back-up using coin cell.	Bidir	Input Range: 1.65V-5.5V Output Options: 2.5V, 3.0V, 3.3V, 3.5V
214	FORCE_ RECOVERY*	SOC_GPIO00	Force Recovery strap pin. Held low when SYS_RESET* goes high (i.e. during power-on) places system in USB recovery mode	System	Input	CMOS – 1.8V
240	SLEEP/WAKE*	POWER_ON	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	System	Input	CMOS – 5.0V
233	SHUTDOWN_ REQ*	–	When driven/pulled low by the module, requests the carrier board to shut down. ~5kΩ pull-up to VDD_IN (5V) on the module.	System	Output	Open Drain, 5.0V
237	POWER_EN	(PMIC EN0 through converter logic)	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 100kΩ pulldown is also on the module.	System	Input	Analog 5.0V
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when pulled high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing between module and carrier board supplies. 1kΩ pull-up to 1.8V on the module.	System	Bidir	Open Drain, 1.8V

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type
178	MOD_SLEEP*	SOC_PWR_REQ	Module Sleep. When active (low), indicates module has gone to Sleep (SC7) mode.	Control of HDMI termination FET. See Figure 8-7 .	Output	CMOS – 1.8V
210	CLK_32K_OUT	(PMIC GPIO4 32K CLK Out)	Sleep/Suspend clock	Sleep/suspend clock for devices such as M.2 Key E	Output	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The directions for FORCE_RECOVERY* and SLEEP/WAKE* signals are true when used for those functions. Otherwise as GPIOs, the direction is bidirectional.

5.1 Power Supply and Sequencing

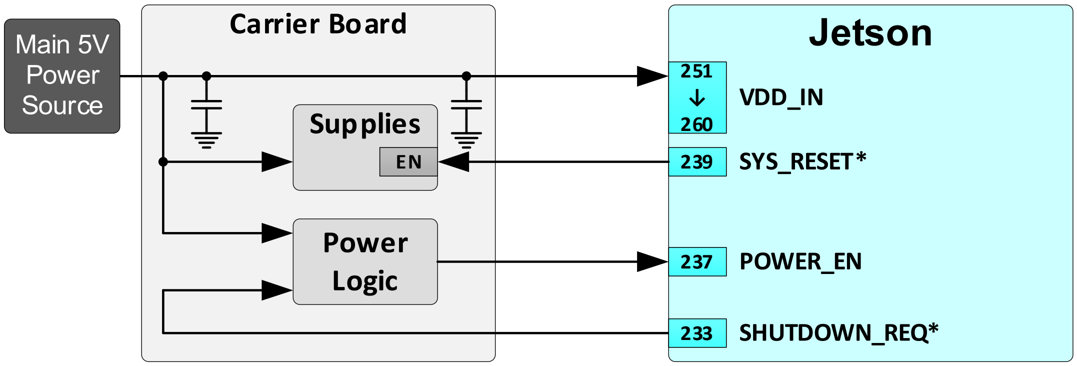
The carrier board receives the main power source and uses this to generate the enable to Jetson Xavier NX module (**POWER_EN**) after the carrier board has ensured the main supply is stable and the associated decoupling capacitors have charged. The carrier board supplies are not enabled at this time. Once **POWER_EN** is driven active (high), the module begins to Power-ON. When the module Power-ON sequence has completed, the **SYS_RESET*** signal is released (pulled high on module) and this is used by the carrier board to enable its various supplies. **SYS_RESET*** is bidirectional and can be driven by the carrier board to reset the module, which results in a full system power cycle. The **SHUTDOWN_REQ*** signal from the module can be driven active (low) if the system must be shut down, due to a critical thermal issue, etc. The power control logic on the carrier board should drive **POWER_EN** inactive (low) if **SHUTDOWN_REQ*** is asserted.

Note: The carrier board cannot drive high or pull high any signals that are associated with the module when the module rails are off. If the designer cannot guarantee a signal will not be driven or pulled high, then either the power rail related to that signal should be left off, or the signals would need to be buffered to isolate them from the module pins. The buffers should only be enabled towards the module when SYS_RESET* goes high.

- POWER_EN
  - **POWER_EN** is a level active signal. When high, the system powers on or stays on. When low, the system powers down or stays off.
  - The developer kit carrier board designs latch **POWER_EN** state to ensure that the signal stays active. The Jetson Nano developer kit carrier board uses an SR latch with discrete logic components, was implemented to latch the **POWER_EN** signal and prevent it from being affected by any other signal other than **SHUTDOWN_REQ***. The Jetson Xavier NX developer kit uses a button MCU controller to latch the **POWER_EN** signal. **POWER_EN** only goes low when a shutdown sequence has been initiated.

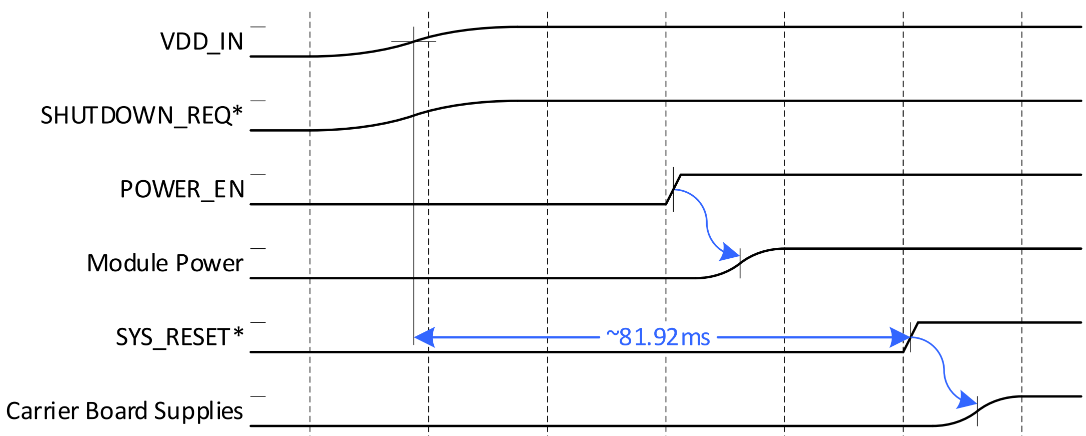
- SYS_RESET*
  - **SYS_RESET*** is bidirectional. The signal is controlled by the PMIC during power-on and power-off. When the system is powered on, **SYS_RESET*** can be driven by the carrier board to reset the module. This results in a full system power cycle.
  - The **SYS_RESET*** signal is asserted by the PMIC during power-on.
  - **SYS_RESET*** is not asserted externally during the power-down sequence. When **POWER_EN** is de-asserted, the PMIC performs a power down sequence which includes asserting **SYS_RESET***.
- SHUTDOWN_REQ*
  - **SHUTDOWN_REQ*** is driven active (low) by the module if the system must be shut down, due to a low power level, a thermal event, or by a GPIO on the PMIC that can be asserted under software control to request a shutdown. The power control logic on the carrier board must drive **POWER_EN** inactive (low) if **SHUTDOWN_REQ*** is asserted.
  - **SHUTDOWN_REQ*** is not driven during power-on. It is pulled up to the 5V supply, so stays inactive. If the system is on and reset is driven low, the PMIC will initiate a full power cycle and start the power-on sequence. Again, **SHUTDOWN_REQ*** is not asserted. **SHUTDOWN_REQ*** will only go low when the system needs to shut down.
  - **SHUTDOWN_REQ*** is de-asserted after **POWER_EN** goes low. **SHUTDOWN_REQ*** comes from a latch on module and is cleared when **POWER_EN** goes low.
  - If **SHUTDOWN_REQ** is asserted, the PMIC will start a system shutdown. **POWER_EN** must be de-asserted within 10 uS after **SHUTDOWN_REQ** is asserted. The system will be powered off (or nearly so) in that time.
  - Asserting **SHUTDOWN_REQ*** is the recommended signal to initiate a power off. Just setting **POWER_EN** high to power the system ON and low to power the system OFF can have issues. Without the **SHUTDOWN_REQ*** signal there can be a logic mismatch between the module and carrier board. If the module shuts down due to a thermal issue, etc. then without the **SHUTDOWN_REQ*** signal the carrier board would not "know" that the module has shut down and the carrier board may just keep **POWER_EN** high. This can cause issues including uncertainties for subsequent power on attempts. The correct sequence should be to assert **SHUTDOWN_REQ*** signal so that carrier knows that module is shutting down so the **POWER_EN** signal can be brought down as well. Using **POWER_EN** to power the system OFF is an option, but **SHUTDOWN_REQ*** must be asserted soon after.
- **Power Rail Discharge:** To satisfy the power down sequencing requirement and prevent unwanted back drive from the carrier board to the module, the following must be true:
  - The carrier board 3.3V power supply that powers any module I/O must be off within 1.5 ms of **SYS_RESET*** assertion.
  - The 1.8V power supply that powers any module I/O must be off within 4 ms.
  - The power rails should be fully discharged before attempting to power back up.

Figure 5-1. System Power and Control Block Diagram



Note: Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

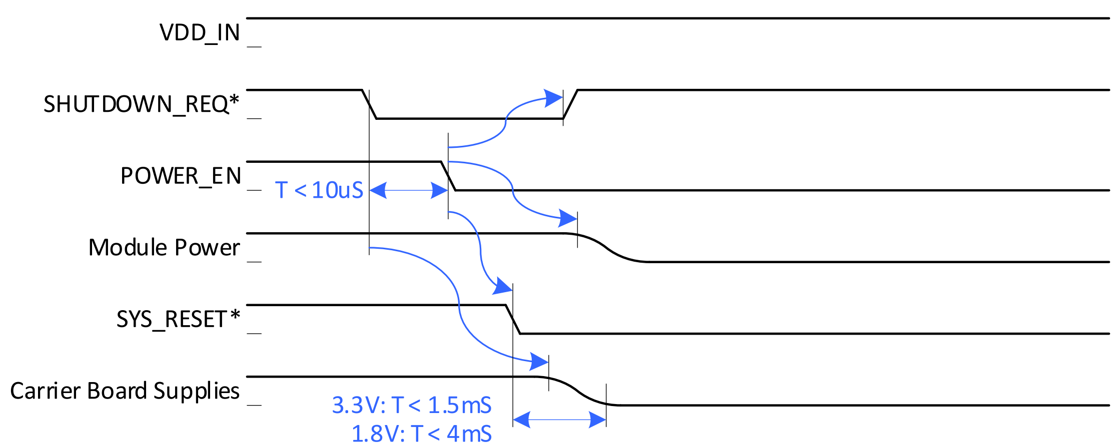
Figure 5-2. Power Up Sequence (No Power Button – Auto Power On)



Notes:

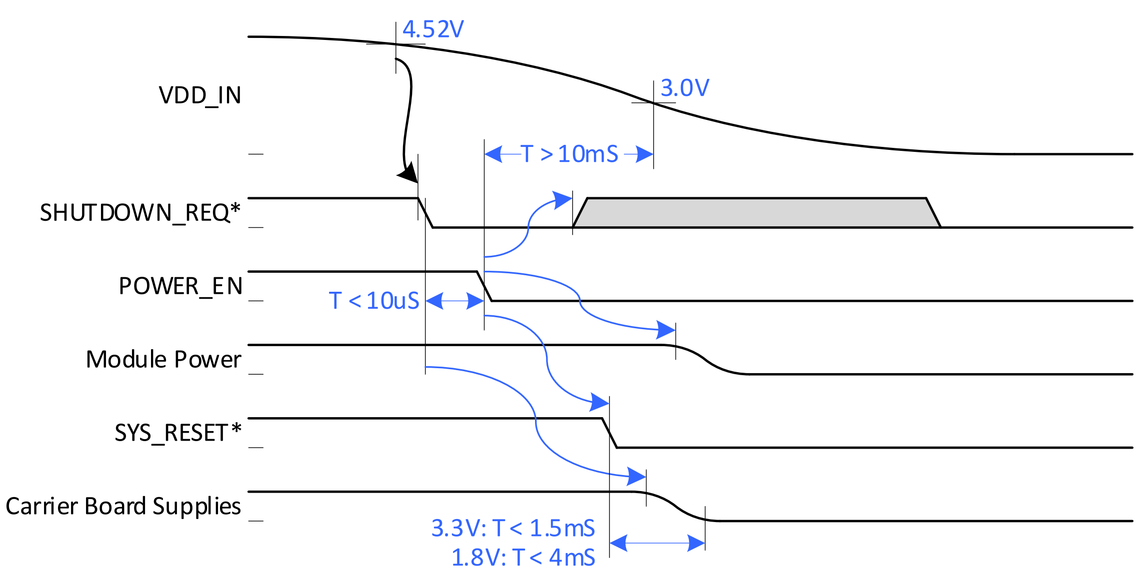
1. SHUTDOWN_REQ* is not driven during power up. The signal is pulled to VDD_IN.
2. SYS_RESET* is driven by the PMIC during power up.

Figure 5-3. Power Down (Initiated by SHUTDOWN_REQ* Assertion)



Note: SYS_RESET* is driven by the PMIC during power down.

Figure 5-4. Power Down (Sudden Power Loss)



Note: SHUTDOWN_REQ* must always be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss.

Chapter 6. USB and PCIe

Jetson Xavier NX allows multiple USB 2.0, USB 3.1 and PCIe interfaces to be brought out of the module.

- USB 2.0: 3x
- USB 3.1: 1x
- PCIe: x1 + x4

The PCIe x4 interface supports both Root Port and Endpoint operation. The PCIe x1 interface supports only Root Port operation.

Table 6-1. Jetson Xavier NX USB 2.0 Pin Description

Pin #	Module Pin Name	Xavier Pin Name	Usage/Description	Recommended Usage	Direction	Pin Type
87	GPIO00	USB_VBUS_EN0	GPIO #0 (USB 0 VBUS Detect)	USB 2.0 Micro B	Bidir	Open Drain, 1.8V
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB conn/device/hub (i.e. Micro B)	Bidir	USB PHY
111	USB0_D_P	USB0_DP				
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB conn/device/hub (i.e. USB 3.1 Hub)	Bidir	USB PHY
117	USB1_D_P	USB1_DP				
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	USB conn/device/hub (i.e. M.2 Key E)	Bidir	USB PHY
123	USB2_D_P	USB2_DP				

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 6-2. Jetson Xavier NX USB 3.1 and PCIe Pin Description

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
131	PCIE0_RX0_N	NVHS0_RX0_N	PCIe #0 Receive 0 (PCIe Ctrl #5 Lane 0)	PCIe x4 conn/device (i.e. M.2 Key M)	Input	PCIe PHY, AC-Coupled for PCIe on carrier board if direct connect.
133	PCIE0_RX0_P	NVHS0_RX0_P				
137	PCIE0_RX1_N	NVHS0_RX1_N	PCIe #0 Receive 1 (PCIe Ctrl #5 Lane 1)			
139	PCIE0_RX1_P	NVHS0_RX1_P				
149	PCIE0_RX2_N	NVHS0_RX2_N	PCIe #0 Receive 2 (PCIe Ctrl #5 Lane 2)			
151	PCIE0_RX2_P	NVHS0_RX2_P				
155	PCIE0_RX3_N	NVHS0_RX3_N	PCIe #0 Receive 3 (PCIe Ctrl #5 Lane 3)			
157	PCIE0_RX3_P	NVHS0_RX3_P				
134	PCIE0_TX0_N	NVHS0_TX0_N	PCIe #0 Transmit 0 (PCIe Ctrl #5 Lane 0)		Output	PCIe PHY, AC-Coupled on carrier board
136	PCIE0_TX0_P	NVHS0_TX0_P				
140	PCIE0_TX1_N	NVHS0_TX1_N	PCIe #0 Transmit 1 PCIe Ctrl #5 Lane 1)			
142	PCIE0_TX1_P	NVHS0_TX1_P				
148	PCIE0_TX2_N	NVHS0_TX2_N	PCIe #0 Transmit 2 (PCIe Ctrl #5 Lane 2)			
150	PCIE0_TX2_P	NVHS0_TX2_P				
154	PCIE0_TX3_N	NVHS0_TX3_N	PCIe #0 Transmit 3 (PCIe Ctrl #5 Lane 3)			
156	PCIE0_TX3_P	NVHS0_TX3_P				
181	PCIE0_RST*	PEX_L5_RST_N	PCIe #0 Reset (PCIe Ctrl #5). 4.7kΩ pull-up to 3.3V on the module. Output when module is Root Port - input when module Endpoint.		Bidir	Open Drain 3.3V, Pull-up on the module
180	PCIE0_CLKREQ*	PEX_L5_CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #5). 47kΩ pull-up to 3.3V on the module. Input when module is Root Port - output when module is Endpoint.			
160	PCIE0_CLK_N	PEX_CLK5N or NVHS0_REFCLK_N	PCIe #0 Reference Clock controlled by on-module mux by SoC CAN0_EN. When CAN0_EN is low, PEX_CLK5 is selected (reference clock when module is Root Port). When CAN0_EN is high, NVHS0_REFCLK is selected (reference clock input when Jetson Xavier NX is an Endpoint).		Bidir	PCIe PHY
162	PCIE0_CLK_P	PEX_CLK5P or NVHS0_REFCLK_P				
167	PCIE1_RX0_N	PEX_RX11_N	PCIe #1 Receive 0 (PCIe Ctrl #4 Lane 0)	PCIe x1 conn/device (i.e. M.2 Key E)	Input	PCIe PHY
169	PCIE1_RX0_P	PEX_RX11_P				
172	PCIE1_TX0_N	PEX_TX11_N	PCIe #1 Transmit 0 (PCIe Ctrl #4 Lane 0)		Output	PCIe PHY, AC-Coupled on carrier board
174	PCIE1_TX0_P	PEX_TX11_P				
183	PCIE1_RST*	PEX_L4_RST_N	PCIe #1 Reset (PCIe Ctrl #4). 4.7kΩ pull-up to 3.3V on the module.		Output	Open Drain 3.3V, Pull-up on the module
182	PCIE1_CLKREQ*	PEX_L4_CLKREQ_N	PCIE #1 Clock Request (PCIe Ctrl #4). 47kΩ pull-up to 3.3V on the module.		Bidir	Open Drain 3.3V, Pull-up on the module
173	PCIE1_CLK_N	PEX_CLK4N	PCIe #1 Reference Clock (PCIe Ctrl #4)		Output	PCIe PHY
175	PCIE1_CLK_P	PEX_CLK4P				
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	Shared between x1 and x4 PCIe interfaces.	Input	Open Drain 3.3V, Pull-up on the module

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
161	USBSS_RX_N	PEX_RX1_N	USB SS Receive (USB 3.1 Ctrl #2)	USB 3.1 connector, device or hub	Input	USB SS PHY, AC-Coupled on carrier board only if direct connect to device
163	USBSS_RX_P	PEX_RX1_P				
166	USBSS_TX_N	PEX_TX1_N	USB SS Transmit (USB 3.1 Ctrl #2)		Output	USB SS PHY, AC-Coupled on carrier board
168	USBSS_TX_P	PEX_TX1_P				

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction shown in this table for PEX_L4_RST* and PCIE_WAKE* signals is true when used for those PCIe functions. Otherwise, if used as GPIOs, the direction is bidirectional.
3. The MPIO Pad Codes are described in the *Xavier Series (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
4. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 6-3 shows the mapping options for Jetson Xavier NX.

Table 6-3. USB SS and PCIe Lane Mapping

Module Pin Names		PCIE0_RX3_N/P PCIE0_TX3_N/P	PCIE0_RX2_N/P PCIE0_TX2_N/P	PCIE0_RX1_N/PPCIE0_TX1_N/P	PCIE0_RX0_N/PPCIE0_TX0_N/P	PCIE1_RX0_N/P PCIE1_TX0_N/P	USBSS_RX_N/P
Xavier Lanes		Lane 5	Lane 4	Lane 3	Lane 2	Lane 11	Lane 1
USB 3.1	PCIe						
1	1x4 + 1x1	PCIe 0 lane 3 Controller #5	PCIe 0 lane 2 Controller #5	PCIe 0 lane 1 Controller #5	PCIe 0 lane 0 Controller #5	PCIe 1 lane 0 Controller #4	USB_SS Port #2
Recommended Usage		PCIe x4 connector or device (I.E. M.2 Key M)				PCIe x1 connector or device (i.e. M.2 Key E)	USB 3.1 connector, device or hub

6.1 USB

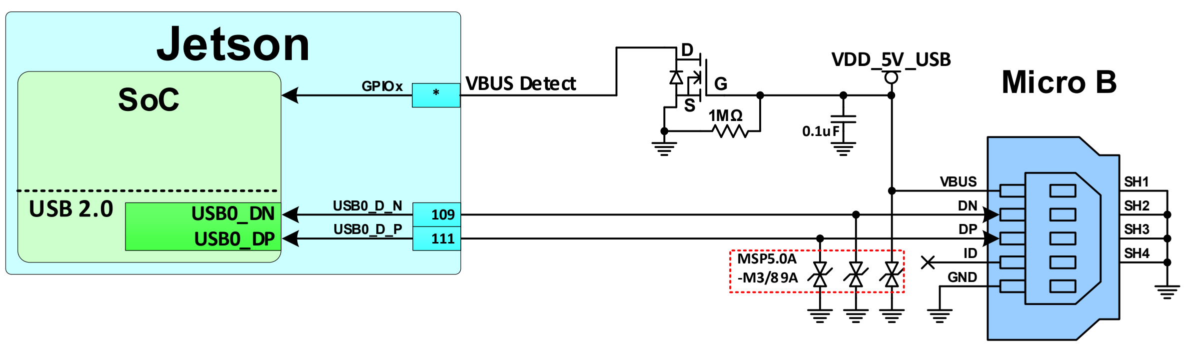
Jetson Xavier NX support s up to three USB 2.0 ports and a single USB 3.1 port. Two examples are shown in Figure 6-1 and Figure 6-2.

Micro B is intended to be used for recovery mode or as a standard USB 2.0 device.

Note: Some non-compliant USB 3.0 devices will not function correctly unless USB 3.1 Gen2 is disabled.

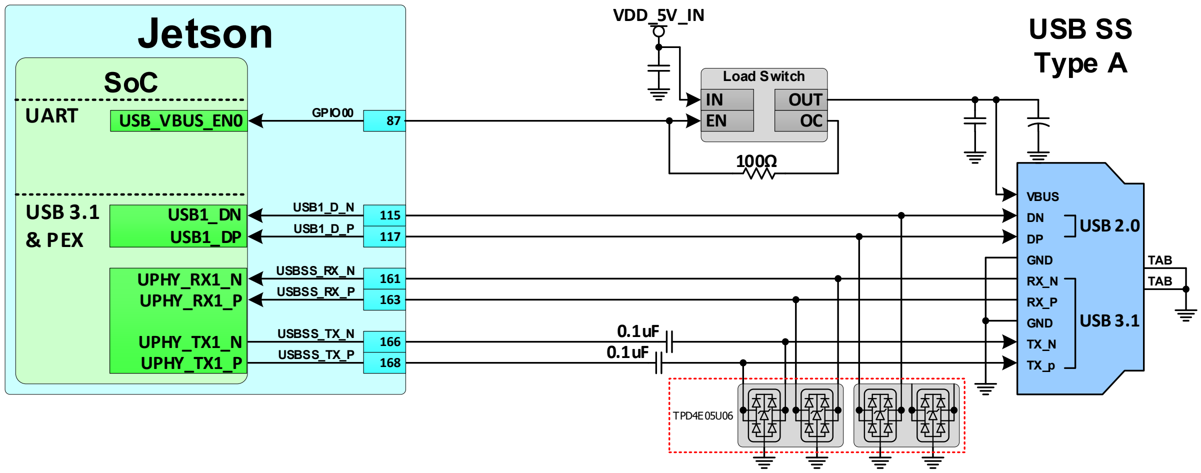
The example shown in Figure 6-1 is for connections to a USB device only connector to be used to support recovery mode (See Section 12.7 for details on recovery mode) or a USB device if booted normally. A USB Micro B connector is shown in the example.

Figure 6-1. USB SS Micro B USB Device and Recovery Connection Example



The example shown in Figure 6-2 is for connections to a USB SS Type A connector to support host only. Recovery mode is not supported.

Figure 6-2. USB SS Type A Host Only Connection Example



Notes:

1. AC capacitors should be located close to either the USB connector, or the Jetson Xavier NX pins.
2. Connector used must be USB Implementers Forum certified if USB 3.1 is implemented.

6.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[2:0]_D_N/P**

Table 6-4. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency (high speed): Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane	GND		
Trace impedance: Diff pair / SE)	90 / 50	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay	6 (960)	In (ps)	
Max intra-pair skew between USBx_D_P and USBx_D_N	7.5	ps	

Notes:

1. Up to four signal vias can share a single GND return via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

6.1.2 USB 3.1 Design Guidelines

The following requirements apply to the USB 3.1 Port #2 PHY interface: **USBSS_TX_N/P**, **USBSS_RX_N/P**.

Table 6-5. USB 3.1 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period GEN1 GEN2	 5.0 / 200 10.0 / 100	Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX & RX
Electrical Specification			
Insertion Loss (IL - Min) Host GEN1 (Type C) GEN1 (Type A) GEN2 Device GEN1 (Micro AB) Resonance Dip Frequency	 -2 -7 -5.4 -1 > 8	 dB dB dB dB GHz	 @ 2.5GHz @ 2.5GHz @ 5GHz @ 2.5GHz The resonance dip could be caused by a via stub for layer transition or trace stub for co-layout.
Time-domain Reflectometer (TDR) Dip GEN1 GEN2	 75 75	Ω	@ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)	≤ −45	dB	DC – 5GHz per each TX-RX NEXT
Impedance			
Trace Impedance: Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic Zdf, does not account for coupling from other trace pairs
Reference plane	GND		
Trace Length/Skew			
Trace loss characteristic (max): GEN1 GEN2	 0.7 0.9	dB/in	@ 2.5GHz (See Figure 6-2) @ 5GHz (See Figure 6-3) The following max length is derived based on this characteristic. The length constraint must be re-defined if loss characteristic is changed.
Breakout Region – Max length	11	mm	Minimum trace width and spacing
Max Trace Length (Host) GEN1 GEN2	 152 (1014) 127 (845)	mm (ps)	
Max Trace Length (Device) GEN1 only	51 (334)	mm (ps)	
Max Intra-Pair Skew (RX/TX_N to RX/TX_P)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length matching should be done before discontinuities.
Differential pair uncoupled length	6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Interleaving			
Trace Spacing: Microstrip / Stripline Pair-Pair To Ref plane and SMT pad To unrelated high-speed signals	 4x / 3x 4x / 3x 4x / 3x	Dielectric height	
Trace Spacing for TX/RX Non-interleaving			

Parameter	Requirement	Units	Notes
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If have to have interleaving routing in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
Min Inter-S_{NEXT} (between TX/RX) Breakout Main-route	 4.85x 3x	Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout Main-route	 11 Max trace length - L_{BRK}	mm	
Via			
Topology	Y-pattern is recommended Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. See Figure 6-4.
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)
Additional Component Placement Order			
	Chip — AC capacitor (TX only) — common mode choke — ESD — Connector		
	See Figure 6-5.		See Figure 6-6.
AC Cap			
Value: Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Voiding	GND/PWR void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max Junction capacitance (IO to GND) GEN1 GEN2	 0.8 0.35	pF	GEN1: SEMTECH RClamp0524p GEN2: TPD4E02B04DQA
Footprint	Pad should be on the net – not trace stub		See Figure 6-7.
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues). See Chapter 17 for details on CMC if implemented.			
FPC (Additional length of Flexible Printed Circuit Board)			
The FPC routing should be included for PCB trace calculations (max length, etc.)			
Characteristic Impedance	Same as PCB		
Loss characteristic	Strongly recommend being the same as the PCB or better		If worse than PCB, the PCB and FPC length must be re-estimated
Connector			
SMT Connector GND Voiding	GND plane under signal pad should be voided. Size of void should be the same size as the pad.		
Connector used must be USB-IF certified			
General: See Chapter 17 for guidelines related to serpentine routing, routing over voids and noise coupling			

The following figures show the USB 3.1. Interface signal routing requirements.

Figure 6-3. IL/NEXT Plot (GEN1)

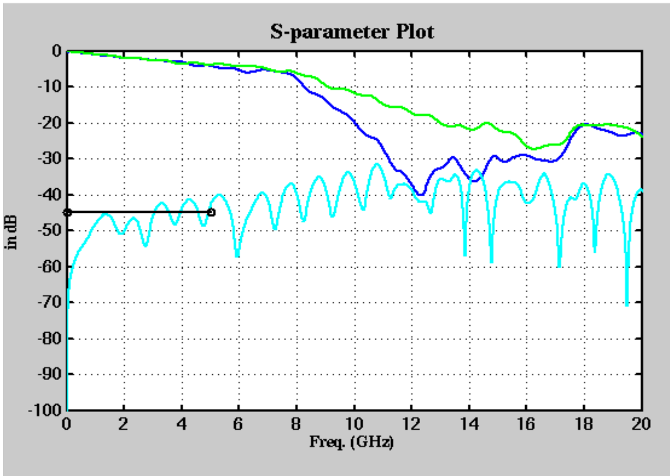


Figure 6-4. IL/NEXT Plot (GEN2)

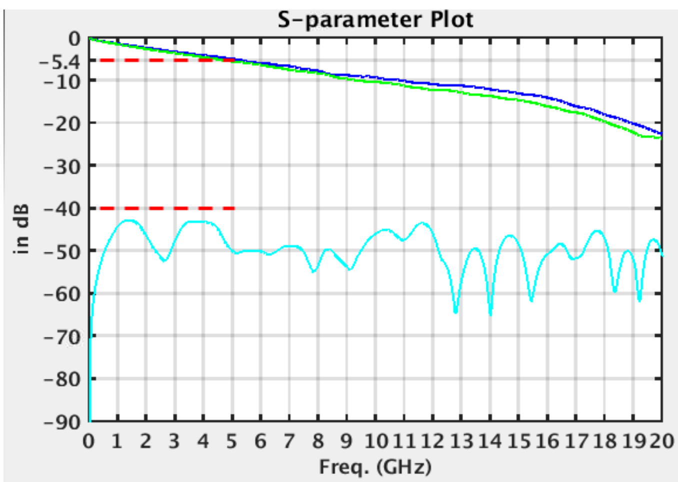


Figure 6-5. Via Topology

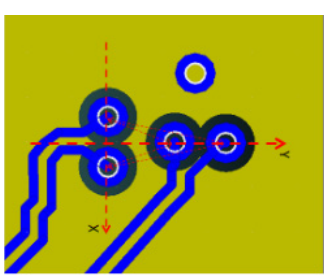


Figure 6-6. Component Order

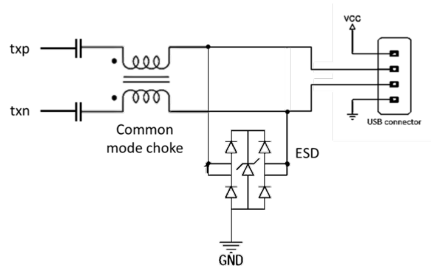


Figure 6-7. Component Placement

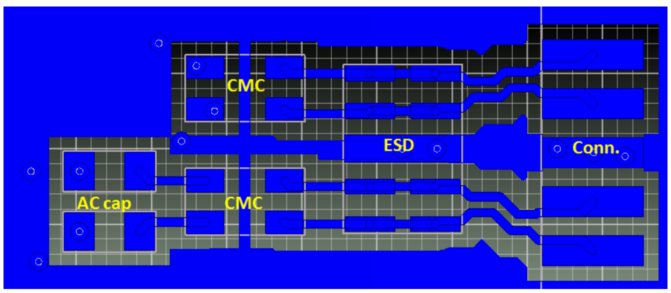
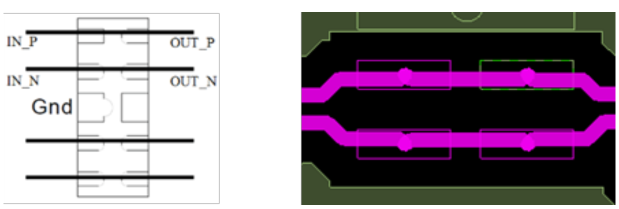


Figure 6-8. ESD Layout Recommendations



6.1.2.1 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs/flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces/areas or power supply components

Table 6-6. Xavier USB 2.0 Signal Connections

Module Ball Name	Type	Termination	Description
USB[2:0]_D_P USB[2:0]_D_N	DIFF I/O	If used, 90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card socket, hub or another device on the PCB.

Table 6-7. Miscellaneous USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
GPIO00 (USB_VBUS_EN0)	I/O		USB0 VBUS Enable: Connect to enable and overcurrent pins of load switch (through 100ohm series resistor to OC pin).
GPIO (VBUS Detect)	I	5V to 1.8V level shifter	VBUS Detect: Connect to VBUS pin of USB connector receiving USB0_+/– interface through level shifter.

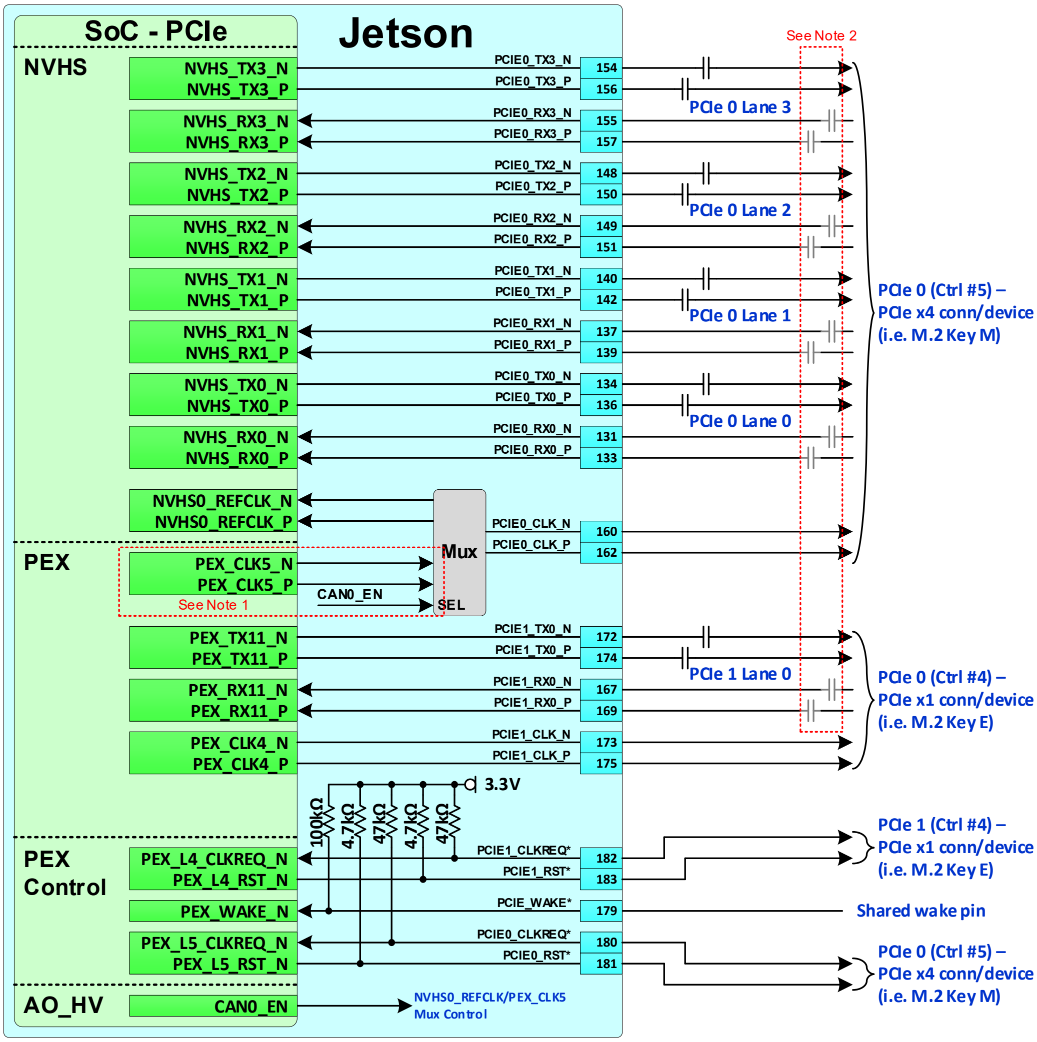
Table 6-8. Xavier USB 3.1 Signal Connections

Module Pin Name	Type	Termination	Description
USBSS_TX_N/P (USB 3.1 Port #2)	DIFF Out	Series 0.1uF caps. ESD Protection near connector if required.	USB 3.1 Differential Transmit Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.
USBSS_RX_N/P (USB 3.1 Port #2)	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. ESD protection near connector if required.	USB 3.1 Differential Receive Data Pairs: Connect to USB 3.1 connectors, hubs or other devices on the PCB.

6.2 PCIe

Jetson Xavier NX brings two PCIe interfaces to the module pins for up to 5 total lanes (1 x4 + 1 x1) for use on the carrier board. The PCIe x4 interface operates up to Gen4 speed and supports both Root Port and Endpoint operation. The PCIe x1 interface operates only up to Gen3 speed and supports only Root Port operation. Figure 6-9 shows both the x1 and x4 interfaces as Root Ports. Figure 6-10 shows the x4 interfaces as an Endpoint.

Figure 6-9. PCIe Root Port Connections Example

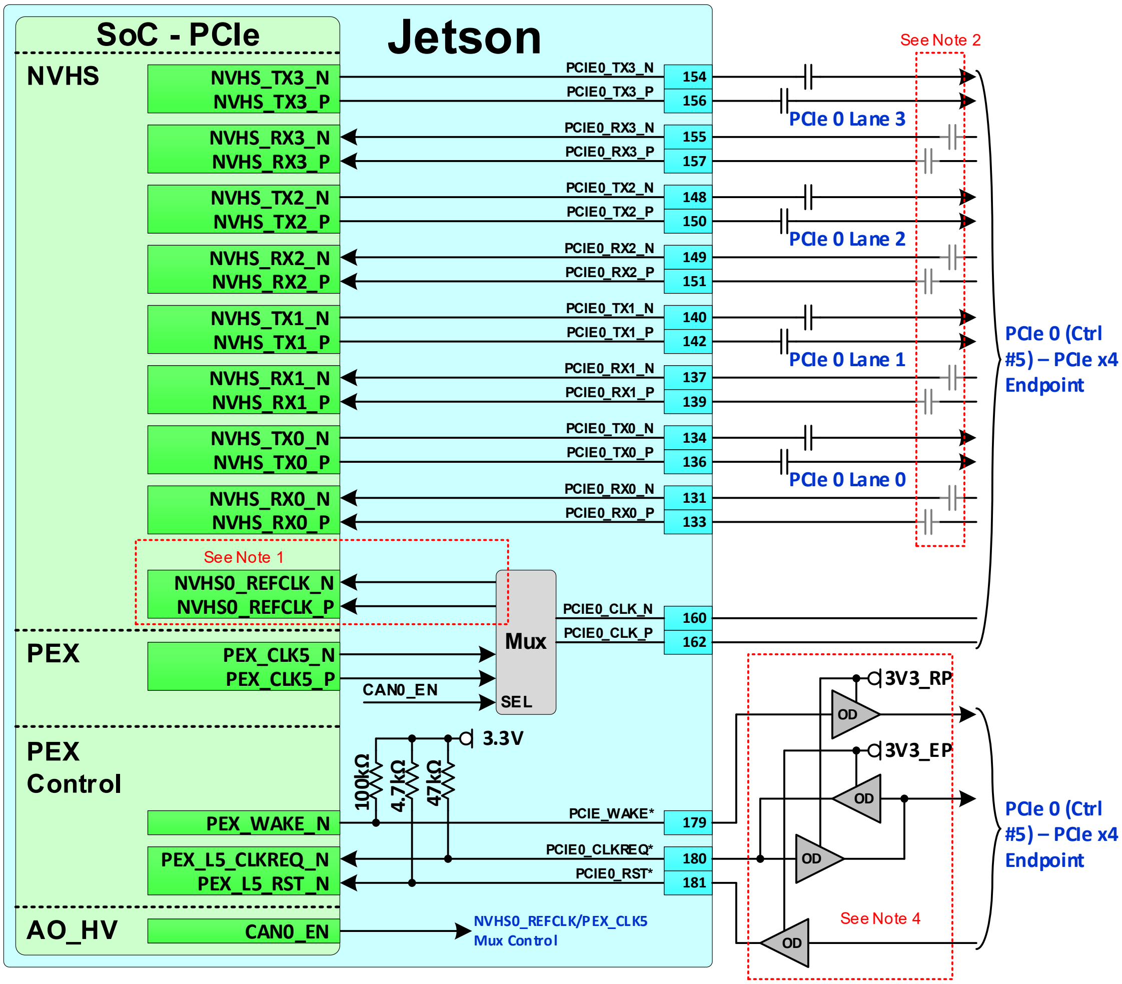


Notes:

1. For Root Port operation, the mux should be set to output the PEX_CLK5 signals. CAN0_EN which is used for the mux select should be set low.
2. AC Capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.
4. The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

Figure 6-10 shows the x4 interface configured as Endpoint for the PCIe Endpoint connections.

Figure 6-10. PCIe Endpoint Connections Example



Notes:

1. For Endpoint operation, the mux should be set to input the reference clock from the PCIe Root Port device to the Jetson Xavier NX NVHS0_REFCLK pins. CAN0_EN which is used for the mux select should be set high.
2. AC capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
3. See design guidelines for correct AC capacitor values.
4. Open-drain buffers are required on the PCIe control signals when Jetson Xavier NX is configured as Endpoint. These isolate the lines from the on-module pull-ups as well as ensure the Endpoint and Root Port devices do not have their pads driven high before power is applied (3V3_RP is 3.3V supply on the Root Port side and 3V3_EP is the 3.3V supply on the Endpoint side.
5. The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

6.2.1 PCIe Design Guidelines

The following tables provide the PCIe routing guidelines for the PCIe #1 (x1) or PCIe #0 (x4) interfaces. PCIe #1 supports up to Gen3 and the first table applies. PCIe #0 supports up to Gen4 and if the design will need to operate at Gen4 speed, the second routing table applies.

Table 6-9. PCIe Interface Signal Routing Requirements (to Gen3)

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	8.0 / 125	Gbps / ps	4.0GHz, half-rate architecture
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To GND Single Ended for P & N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%. See Note 1
Reference plane	GND		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 3x / 4x 3x / 4x 3x / 4x	Dielectric	TX and RX should not be routed on the same layer. See Note 2.
Length/Skew			
Trace loss budget (for carrier board routing) Routing direct to device Routing to PCIe/M.2 connector	 -11.5 -7.5	dB/in	@ 4GHz (See Figure 6-2), Loss: GEN3 budget – module – end device – safety margin (-22dB + 3.5dB + 4dB + 3dB) Loss: GEN3 budget – module – end device – safety margin (-22dB + 3.5dB + 8dB + 3dB)
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length (delay) Direct to device on carrier board Stripline Microstrip Routed to PCIe or M.2 connector Stripline Microstrip	 15.3 (2680) 14.4 (2160) 10 (1750) 9.4 (1400)	in (ps)	Mid-loss PCB of 0.8dB/in (Microstrip) or 0.75dB/in (Stripline) is used. Also, 175ps/in for Stripline routing and 150ps/in for Microstrip.
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.075 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities. See notes 3 and 4.
Within pair (intra-pair) matching between subsequent discontinuities	0.075 (0.5)	mm (ps)	See notes 3 and 4.
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place GND vias as symmetrically as possible to data pair vias. GND via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	 2 for TX traces and 2 for RX trace No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		

Parameter	Requirement	Units	Notes
AC Cap			
Value GEN1/GEN2: Min/Max GEN3: Min/Max	 0.075 / 0.265 0.176 / 0.265	uF	0.1uF or 0.22uF recommended for GEN1 or GEN2. 0.22uF recommended for GEN3. Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		See Figure 6-12.
Connector			
Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		See Figure 6-13.
General: See Chapter 17 for guidelines related to serpentine routing, routing over voids and noise coupling			

Notes:

1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. For trace loss >= 0.7dB/in @ 2.5 GHz, the max trace length should be 7 inches. To reduce trace loss, ensure the loss tangent of the dielectric material and roughness of the metal are tightly controlled.
4. The average of the differential signals is used for length matching.
5. Do length matching before Via transitions to different layers or any discontinuity to minimize common mode conversion.

Figure 6-11. Insertion Loss S-Parameter Plot (SDD21)

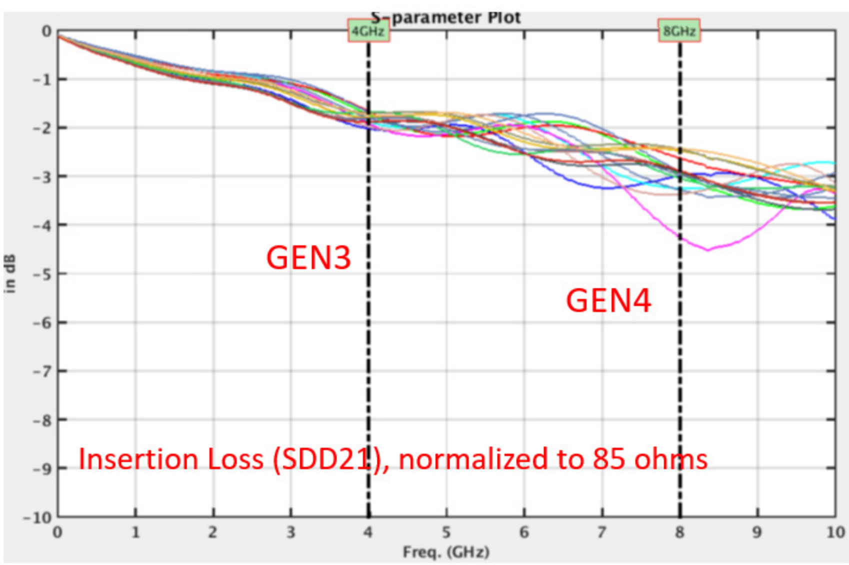


Figure 6-12. Insertion Loss S-Parameter Plot (SDD11)

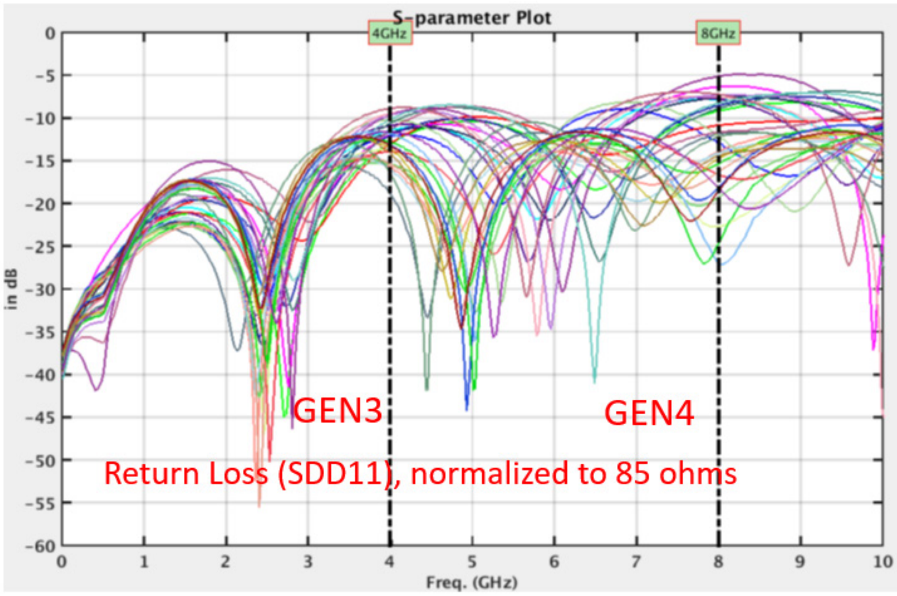


Figure 6-13. AC Cap Voiding

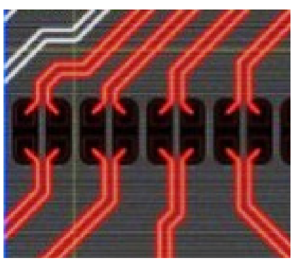


Figure 6-14. Connector Voiding

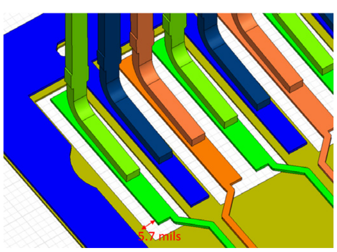


Table 6-10. PCIe Gen4 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	16.0 / 62.5	Gbps / ps	8.0GHz, half-rate architecture
Topology	Point-point		Unidirectional, differential. Driven by 100 MHz common reference clock
Termination	43	Ω	To GND Single Ended for P and N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%
Reference plane	GND		
Fiber-weave effect	• Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew • Use zig-zag route instead of straight to minimize skew, this is a mandatory for PCIe gen4 design		See Figure 6-14
Spacing			
Trace Spacing (Stripline) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 4x 4x 4x	Dielectric	TX and RX should not be routed on the same layer. If this is required in a design, they should not be interleaved, and the spacing between the closest RX and TX lanes must be 9x Dielectric spacing.
Length/Skew			
Trace loss budget (for carrier board routing) Routing direct to device Routing to PCIe/M.2 connector	 -16 -10.5	dB/in	@ 4GHz (See Figure 6-2), Loss: GEN4 budget – module – end device – safety margin (-28dB + 5dB + 4dB + 3dB) Loss: GEN3 budget – module – end device – safety margin (-28dB + 5dB + 9.5dB + 3dB)
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length (delay) Direct to device on carrier board Stripline Microstrip Routed to PCIe or M.2 connector Stripline Microstrip	 11.9 (2070) 10.9 (1630) 7.8 (1360) 7.1 (1070)	in (ps)	Mid-loss PCB of 1.47dB/in (Microstrip) or 1.35dB/in (Stripline) is used. Also, 175ps/in for Stripline routing and 150ps/in for Microstrip.
Max PCB via distance from the Device/Connector	41.9	ps	Max distance from Device ball or Connector pin to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities.
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place GND vias as symmetrically as possible to data pair vias. GND via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	4		Use micro via or back drilled via - no via stub allowed.
Max Via stub length	na		Not Allowed
AC Cap			

Parameter	Requirement	Units	Notes
Value Min/Max	0.22	uF	20%, 0402 X5R or better. Only required for TX pair when routed to connector. Place close to TX side.
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is required.		See Figure 6-12.
MIsc.			
GND fill rule	Remove unwanted GND fill that is either floating or act like antenna		
Connector			
Voiding	Void all layers of golden finger area under the pad 5.7 mils larger than the pad size is recommended.		See Figure 6-13.
General: See Chapter 17 for guidelines related to serpentine routing, routing over voids and noise coupling			

Notes:

1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. The average of the differential signals is used for length matching.
4. Do length matching before Via transitions to different layers or any discontinuity to minimize common mode conversion.

Figure 6-15. Example Zig-Zag Routing

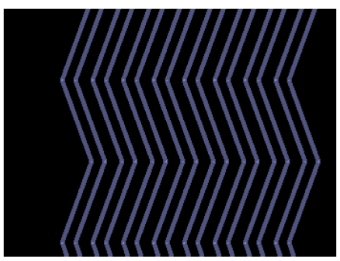


Table 6-11. PCIe Signal Connections

Module Pin Name	Type	Termination	Description
PCIe Interface 0 (x4 – Controller #5)			
PCIE0_TX3_N/P PCIE0_TX2_N/P PCIE0_TX1_N/P PCIE0_TX0_N/P	DIFF OUT	Series 0.22uF Capacitor	**Differential Transmit Data Pairs:** Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_RX3_N/P PCIE0_RX2_N/P PCIE0_RX1_N/P PCIE0_RX0_N/P	DIFF IN	Series 0.22uF capacitors near Jetson Xavier NX pins or device if device on main PCB.	**Differential Receive Data Pairs:** Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE0_CLK_N/P	DIFF OUT (Rootport) DIFF IN (Endpoint)		**Differential Reference Clock Output:** Connected to a mux on the module that selects either PEX_CLK5 or NVHS0_REFCLK. Connect to REFCLK_N/P pins of PCIe device/connector. For Root Port operation, set the mux to select PEX_CLK3 (CAN0_EN = 0). For Endpoint, set the mux to select NVHS0_REFCLK (CAN_EN = 1).

Module Pin Name	Type	Termination	Description
PCIE0_CLKREQ*	I/O (Root Port) I (Endpoint)	47kΩ pull-up to VDD_3V3_SYS on module	PCIe Clock Request for PCIE0_CLK: Connect to CLKREQ pins on device/connector(s)
PCIE0_RST*	O (Root Port) I (Endpoint)	4.7kΩ pull-up to VDD_3V3_SYS on module	PCIe Reset: Connect to PERST pins on device/connector(s)
PCIe Interface 1 (x1 – Controller #4)			
PCIE1_TX0_N/P	DIFF OUT	Series 0.22uF Capacitor	Differential Transmit Data Pair: Connect to TX_N/P pins of PCIe connector or RX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_RX0_N/P	DIFF IN	Series 0.22uF capacitors near Jetson Xavier NX pins or device if device on main PCB.	Differential Receive Data Pair: Connect to RX_N/P pins of PCIe connector or TX_N/P pin of PCIe device through AC cap according to supported configuration.
PCIE1_CLK_N/P	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_N/P pins of PCIe device/connector
PCIE1_CLKREQ*	I/O	47kΩ pull-up to VDD_3V3_SYS on module	PCIe Clock Request for PCIE1_CLK: Connect to CLKREQ pins on device/connector(s). If the module is configured as an Endpoint, include open-drain buffers between the clock request pin on the module and the device/connector. One buffer should have the output to the module and be powered by the 3.3V rail on the module. The other buffer should have the output pointing at the connector/device and be powered by the 3.3V rail at the connector/device. These buffers isolate the on-module pull-up resistors as well as ensures the pins on both the Root Port and Endpoint sides will not be driven high before the associated power is enabled.
PCIE1_RST*	O	4.7kΩ pull-up to VDD_3V3_SYS on module	PCIe Reset: Connect to PERST pins on device/connector(s). If the module is configured as an Endpoint, include an open-drain buffer between the reset pin on the module and the device/connector powered by the 3.3V rail at the connector/device. The buffer should have the output toward the module. This isolates the on-module pull-up resistor as well as ensures this signal will not be pulled/driven high before the module is powered on.
Common			
PCIE_WAKE*	I	100kΩ pull-up to VDD_3V3_SYS on module	PCIe Wake: Connect to WAKE pins on device or connector. If the module is configured as an Endpoint, include an open-drain buffer between the wake pin on the module and the device/connector powered by the 3.3V rail at the connector/device. The buffer should have the output toward the connector/device. This isolates the on-module pull-up resistors as well as ensures this signal will not be pulled/driven high before the Root Port is powered on.

Chapter 7. Gigabit Ethernet

Jetson Xavier NX integrates a Realtek RTL8211FDI Gigabit Ethernet PHY. The magnetics and RJ45 connector is implemented on the carrier board.

Table 7-1. Jetson Xavier NX Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)	LAN	Output	
188	GBE_LED_LINK	–	Ethernet Link LED (Green)	LAN	Output	
184	GBE_MDI0_N	–	GbE Transformer Data 0	LAN	Bidir	MDI
186	GBE_MDI0_P	–	GbE Transformer Data 0	LAN	Bidir	MDI
190	GBE_MDI1_N	–	GbE Transformer Data 1	LAN	Bidir	MDI
192	GBE_MDI1_P	–	GbE Transformer Data 1	LAN	Bidir	MDI
196	GBE_MDI2_N	–	GbE Transformer Data 2	LAN	Bidir	MDI
198	GBE_MDI2_P	–	GbE Transformer Data 2	LAN	Bidir	MDI
202	GBE_MDI3_N	–	GbE Transformer Data 3	LAN	Bidir	MDI
204	GBE_MDI3_P	–	GbE Transformer Data 3	LAN	Bidir	MDI

Notes: In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.

Figure 7-1. Jetson Xavier NX Ethernet Connections

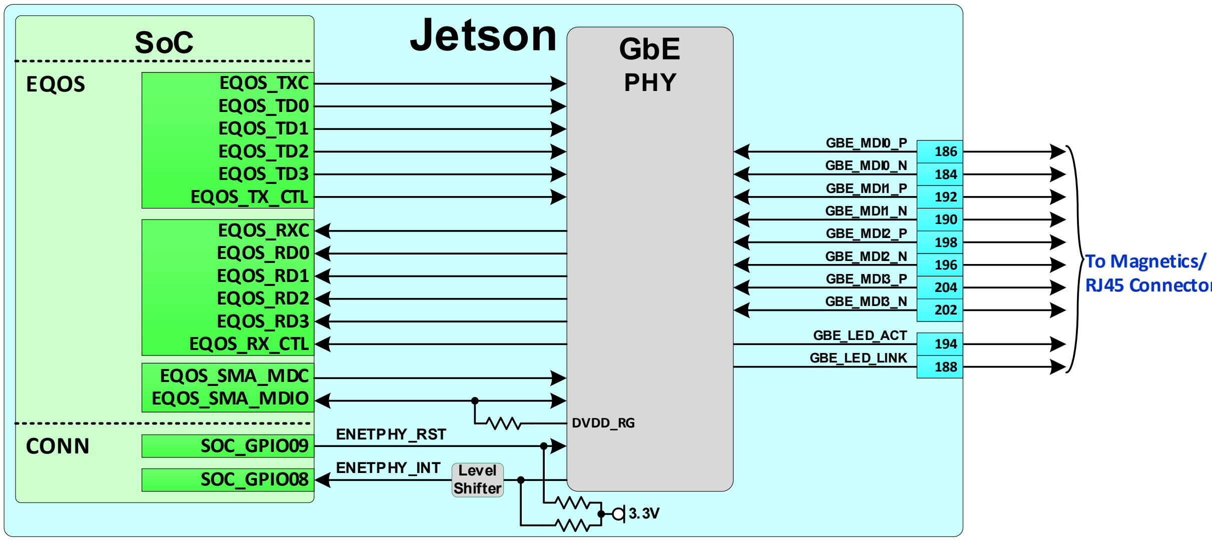


Figure 7-2. Gigabit Ethernet Magnetics and RJ45 Connections

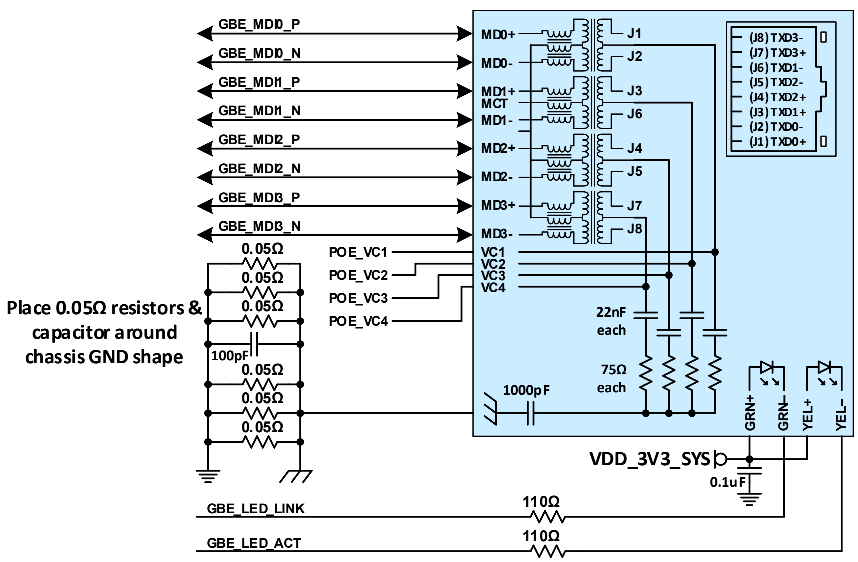


Table 7-2. Ethernet MDI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Reference plane		GND		
Trace impedance	Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)		0.763	mm	
Max trace length/delay		109 (690)	mm (ps)	
Max within pair (intra-pair) skew		0.15 (1)	mm (ps)	
Number of vias		minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.
Notes: Xavier does not support delay/skewing of clock vs data. This must be enabled in the PHY.				

Table 7-3. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
GBE_MDI[3:0]_N/P	DIFF I/O		Gigabit Ethernet MDI IF Pairs: Connect to Magnetics -/+ pins
GBE_LED_LINK	O	110Ω (minimum) series resistor	Gigabit Ethernet Link LED: Connect to green LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS
GBE_LED_ACT	O	110Ω (minimum) series resistor	Gigabit Ethernet Activity LED: Connect to yellow LED cathode on RJ45 connector. Anode connected to VDD_3V3_SYS

Chapter 8. Display

Jetson Xavier NX designs can select from several display options including VESA® Embedded DisplayPort® (eDP) for embedded displays, and HDMI™ or DisplayPort (DP) for external displays. The two display interfaces can be run simultaneously.

Table 8-1. Jetson Xavier NX eDP and DP Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
90	DP0_AUX_N	DP_AUX_CH0_N	DisplayPort 0 Aux– or HDMI DDC SDA	DP connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
92	DP0_AUX_P	DP_AUX_CH0_P	DisplayPort 0 Aux+ or HDMI DDC SCL	DP connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
39	DP0_TXD0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0 or HDMI Lane 2	DP connector	Output	AC-Coupled on carrier board
41	DP0_TXD0_P	HDMI_DP0_TXDP0	DisplayPort 0 Lane 0 or HDMI Lane 2	DP connector	Output	AC-Coupled on carrier board
45	DP0_TXD1_N	HDMI_DP0_TXDN1	DisplayPort 0 or HDMI Lane 1	DP connector	Output	AC-Coupled on carrier board
47	DP0_TXD1_P	HDMI_DP0_TXDP1	DisplayPort 0 or HDMI Lane 1	DP connector	Output	AC-Coupled on carrier board
51	DP0_TXD2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2 or HDMI Lane 0	DP connector	Output	AC-Coupled on carrier board
53	DP0_TXD2_P	HDMI_DP0_TXDP2	DisplayPort 0 Lane 2 or HDMI Lane 0	DP connector	Output	AC-Coupled on carrier board
57	DP0_TXD3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3– or HDMI Clk Lane	DP connector	Output	AC-Coupled on carrier board
59	DP0_TXD3_P	HDMI_DP0_TXDP3	DisplayPort 0 Lane 3– or HDMI Clk Lane	DP connector	Output	AC-Coupled on carrier board
88	DP0_HPD	DP_AUX_CH0_HPD	HDMI or DisplayPort 0 Hot Plug Detect. Must be active high for DP. For HDMI, the polarity can be changed in SW.	DP connector	Input	CMOS – 1.8V
98	DP1_AUX_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA	HDMI Connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
100	DP1_AUX_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL	HDMI Connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC)
63	DP1_TXD0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2	HDMI Connector	Output	AC-Coupled on carrier board
65	DP1_TXD0_P	HDMI_DP1_TXDP0	DisplayPort 1 Lane 0 or HDMI Lane 2	HDMI Connector	Output	AC-Coupled on carrier board
69	DP1_TXD1_N	HDMI_DP1_TXDN1	DisplayPort 1 or HDMI Lane 1	HDMI Connector	Output	AC-Coupled on carrier board
71	DP1_TXD1_P	HDMI_DP1_TXDP1	DisplayPort 1 or HDMI Lane 1	HDMI Connector	Output	AC-Coupled on carrier board

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
75	DP1_TXD2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0			
77	DP1_TXD2_P	HDMI_DP1_TXDP2				
81	DP1_TXD3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3 or HDMI Clk Lane			
83	DP1_TXD3_P	HDMI_DP1_TXDP3				
96	DP1_HPD	DP_AUX_CH1_HPD	Display Port 1 or HDMI Hot Plug Detect. Must be active high for DP. For HDMI, the polarity can be changed in SW.		Input	CMOS – 1.8V
94	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction shown in this table for DP_AUX_CH[1:0]_HPD is true when used for Hot-plug Detect. Otherwise if used as GPIOs, the direction is bidirectional.

A standard DP 1.4 or HDMI V2.0 interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively.

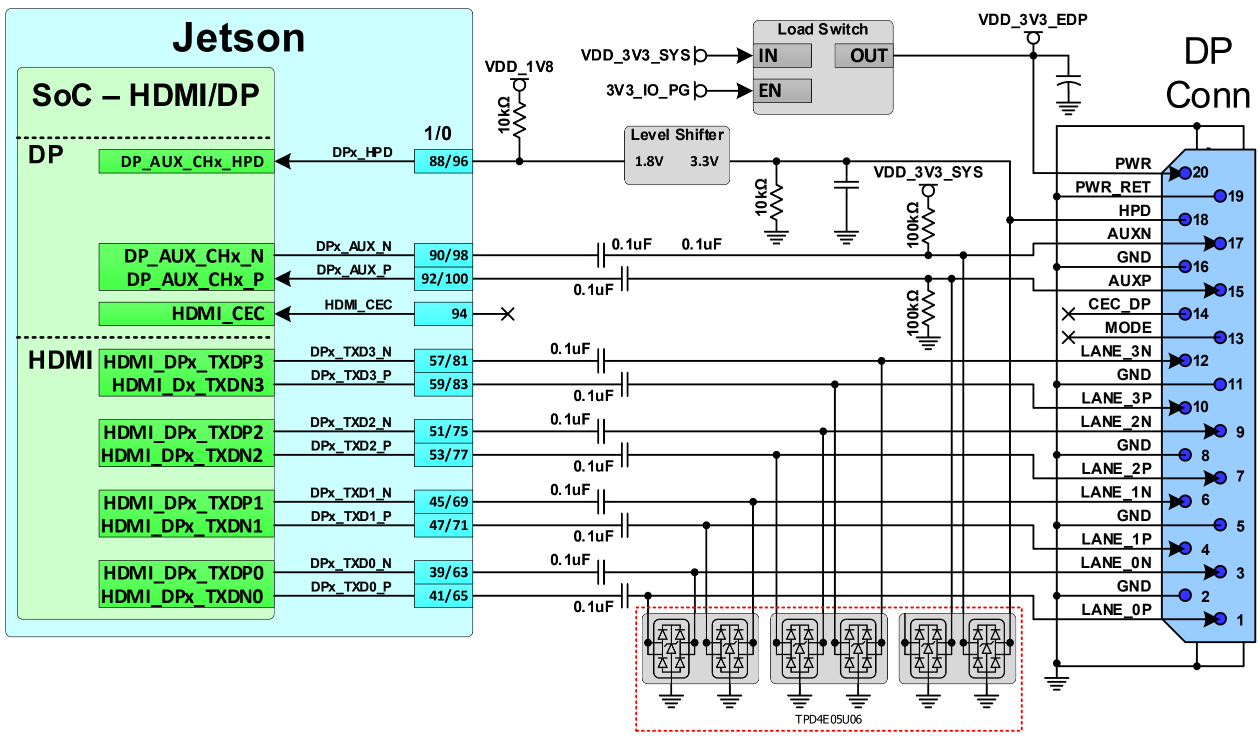
Table 8-2. DP and HDMI Pin Mapping

Module Pin Name	Module Pin #s	HDMI	DP
DP[1:0]_TXD3_P DP[1:0]_TXD3_N	59/83 57/81	TXC+ TXC –	TX3+ TX3–
DP[1:0]_TXD2_P DP[1:0]_TXD2_N	53/77 51/75	TX0+ TX0–	TX2+ TX2–
DP[1:0]_TXD1_P DP[1:0]_TXD1_N	47/71 45/69	TX1+ TX1–	TX1+ TX1–
DP[1:0]_TXD0_P DP[1:0]_TXD0_N	41/65 39/63	TX2+ TX2–	TX0+ TX0–

8.1 eDP and DP

Figure 8-1 shows the DP and eDP connection example.

Figure 8-1. DP and eDP Connection Example



Notes:

1. Level shifter required on DP0_HPD to avoid the pin from being driven when Jetson Xavier NX is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display). The reference design uses a BJT level shifter and a resistor divider is needed. See the reference design if a similar approach will be used.
2. Load Switch enable is from powergood pin of main 3.3V supply.

8.1.1 eDP and DP Routing Guidelines

The following routing requirements meet the eDP and DP routing guidelines.

Figure 8-2. eDP and DP Differential Main Link Topology

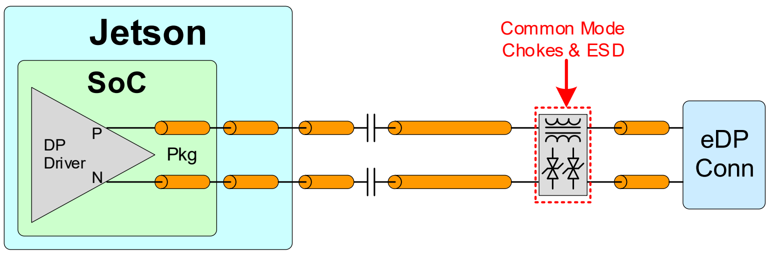


Table 8-3. ePD and DP Main Link Signal Requirements Including DP_AUX

Parameter	Requirement	Units	Notes
Specification			
Max data rate / Min UI RBR HBR HBR2 HBR3	 1.6 / 617 2.7 / 370 5.4 / 185 8.1 / 123	 Gbps / ps	Per data lane
Number of loads / topology	1	load	Point-Point, differential, unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Spec			
IL (min) RBR HBR HBR2 HBR3	 -0.7 -1.2 -2.4 -4.0	 dB @ 0.81GHz dB @ 1.35GHz dB @ 2.7GHz dB @ 4.05GHz	
Resonance dip frequency (min) HBR2 HBR3	 8 12	 GHz	
TDR dip (min)	85	Ω	@ Tr-200ps (10%-90%)
FEXT (max)	-40 -30 -30	dB @ DC dB @ 2.7GHz dB @ 2.7GHz	See Figure 8-3 and TBD
Impedance			
Trace impedance Diff pair	90 85	Ω (±15%)	100Ω is the spec. target.

Parameter	Requirement	Units	Notes
			85Ω is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference plane	GND		
Trace Length, Spacing and Skew			
Trace loss characteristic (max) Up to HBR2 HBR3	 0.81 0.7	 dB/in@ 2.7GHz dB/in@ 4.0GHz	The max lengths are derived based on this characteristic. See Note 2.
Max PCB via dist. from connector RBR/HBR HBR2/HBR3	 No requirement 7.63 (0.3)	mm (in)	
Max trace length/delay from Jetson Xavier NX TX to connector (Up to HBR3) Stripline Microstrip	 100 (700) 100 (600)	mm (ps)	175ps/inch assumption for stripline, 150ps/inch for microstrip.
Trace spacing (pair-pair) Stripline Microstrip (HBR/RBR) Microstrip (HBR2/HBR3)	 3x 4x 5x	dielectric	
Trace spacing (Main link to AUX) Stripline/Microstrip	 3x / 5x	 dielectric	
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See Note 3
Max inter-pair (pair-pair) skew	150	ps	See Note 4
Via			
Max GND transition via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching via near signal vias.
Via Structure			
Impedance dip (min) Recommended via dimension Drill/Pad for impedance control Antipad (min) Via pitch (min)	97 92 200/400 840 880	Ω @ 200ps Ω @ 35ps um um um	The via dimension is required for HDMI-DP co-layout.
Topology	Y-pattern is recommended Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See eDP/DP guideline Figure 8-5
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2mm center-center.		See eDP/DP guideline Figure 8-6
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain a return path, while its Xtalk suppression is limited.
Max # of vias PTH vias Micro vias	2 if all vias are PTH via		

Parameter	Requirement	Units	Notes
	Not limited as long as total channel loss meets IL spec		
Max via stub length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max distance from AC cap to connector RBR/HBR HBR2/HBR3	 No requirement 0.5	 in	
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
Connector			
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2:** Standard DP connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7 mil larger than the connector pad.
General: See Chapter 17 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
4. The average of the differential signals is used for length matching.

The following figures show the eDP and DP interface signal routing requirements.

Figure 8-3. S-Parameter (up to HBR2)

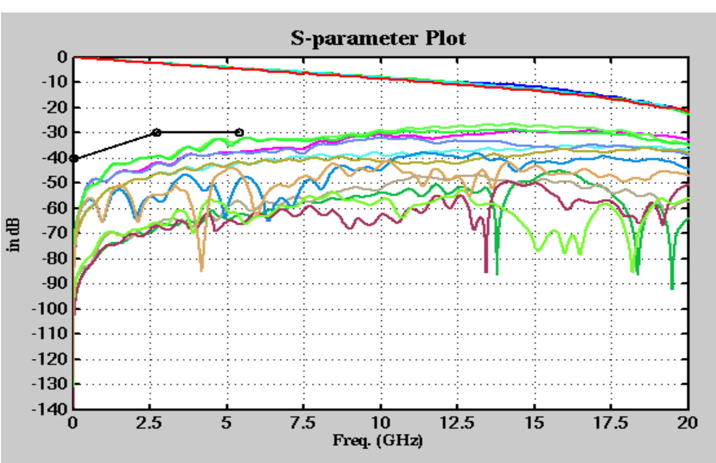


Figure 8-4. S-Parameter (up to HBR3)

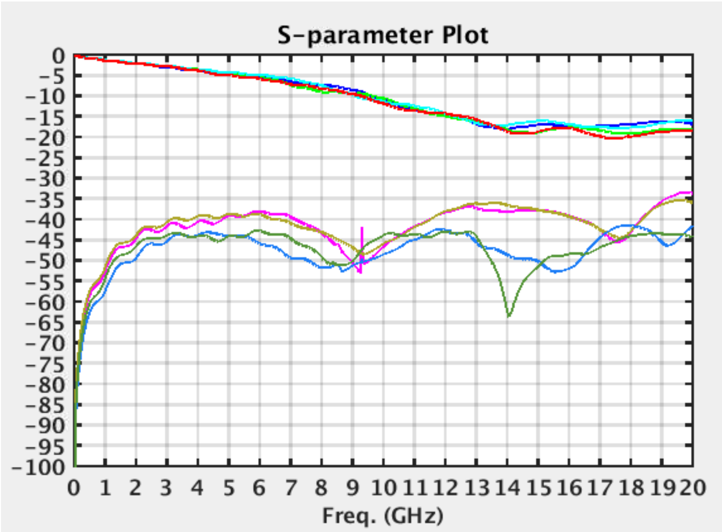


Figure 8-5. Via Topology #1

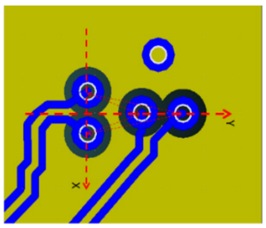


Figure 8-6. Via Topology #2

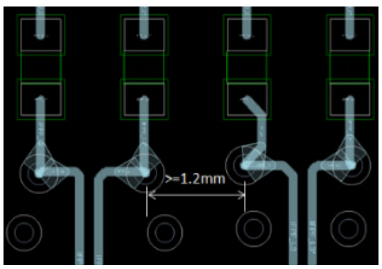


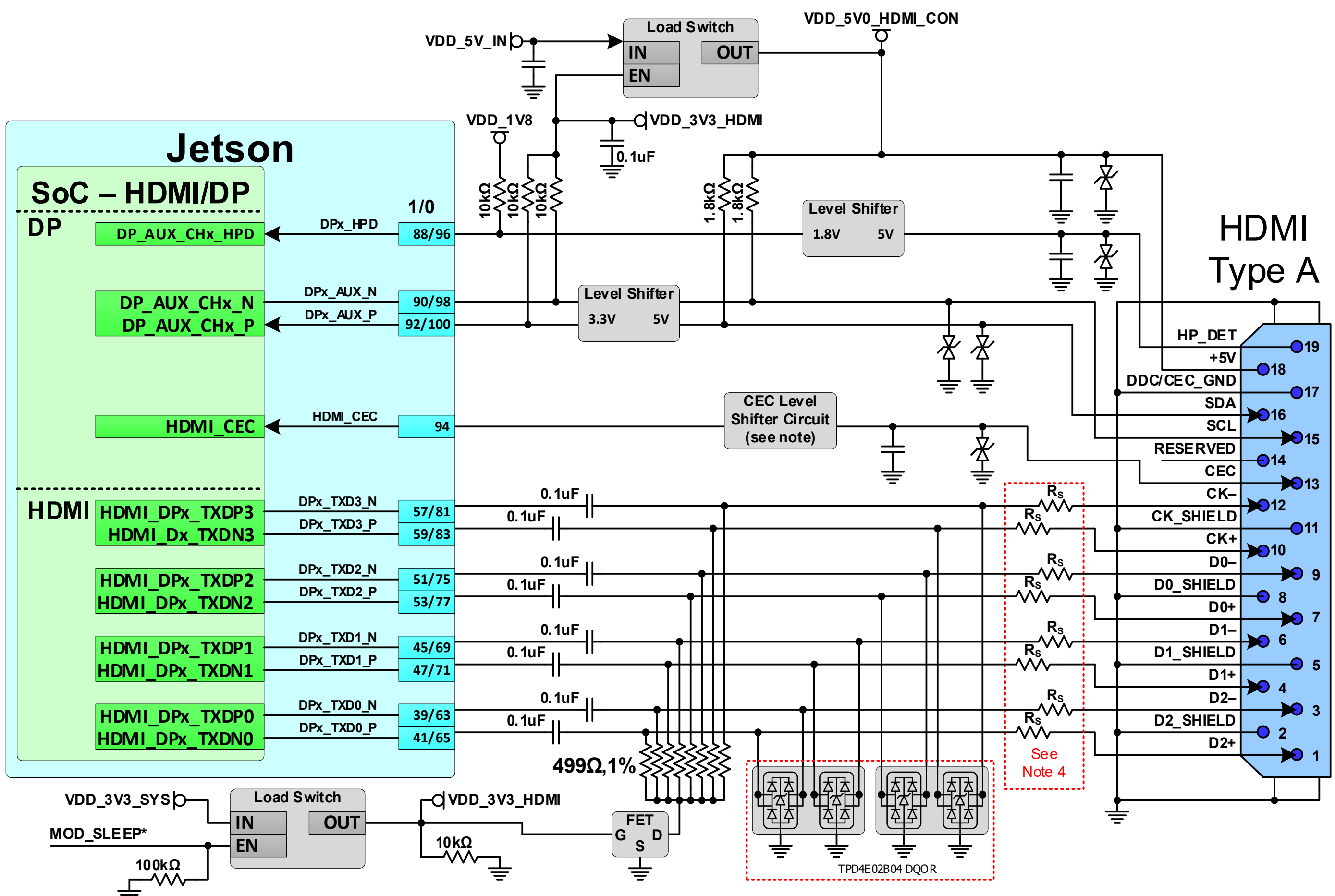
Table 8-4. eDP and DP Signal Connections

Module Pin Name	Type	Termination	Description
DPx_TXD[3:0]_N/P	O	Series 0.1uF capacitors and ESD to **GND** on all.	**eDP/DP Differential CLK/Data Lanes:** Connect to matching pins on display connector.
DPx_AUX_N/P	I/OD	Series 0.1uF capacitors. 100kΩ pulldown on DP0_AUX_P and 100kΩ pull-up to VDD_3V3_SYS on DP0_AUX_N. ESD to **GND** on both.	**eDP/DP: Auxiliary Channels:** Connect to AUX_CH-/+ on display connector.
DPx_HPD	I	Level shifter (1.8V on module side, 3.3V on DP/eDP connector side) and ESD to **GND**..	**eDP/DP: Hot Plug Detect:** Connect to HPD pin on display connector through level shifter.

8.2 HDMI

A standard DP 1.2a or HDMI V2.0 interface is supported. See Figure 8-7 for more details.

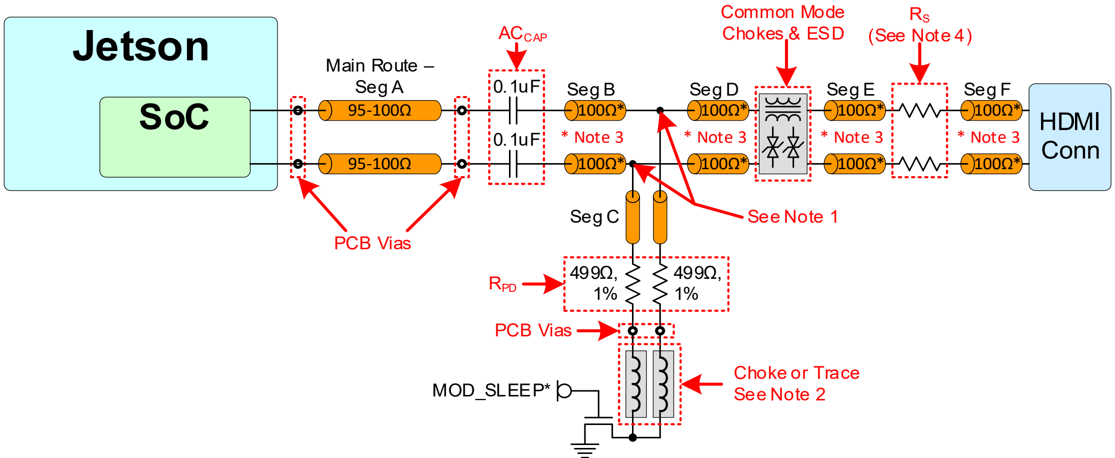
Figure 8-7. HDMI Connection Example



Notes:

1. Level shifters required on DDC/HPD. Xavier pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting. The HPD level shifter in the reference design is inverting. The reference design uses a BJT level shifter and a resistor divider is needed. See the reference design if a similar approach will be used.
2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of the "HDMI Interface Signal Routing Requirements" table (Table 8-5).
3. The DP1_TXx pads are native DP pads and require series AC capacitors (ACCAP) and pull-downs (RPD) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when Jetson Xavier NX is off or in sleep mode to meet the HDMI VOFF requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
4. Series resistors RS are required. See the RS section in Table 8-5 for details.
5. See reference design for CEC level shifting/blocking circuit.

Figure 8-8. HDMI Clk and Data Topology



Notes:

1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH @ DC-100 MHz) between pull-downs and FET are chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 ohm differential impedance, or as uncoupled 50 ohm SE traces.
4. RS series resistor is required to meet HDMI 2.0 compliance. See the RS section in Table 8-5 for details.

Table 8-5. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, differential
Termination At receiver On-board	 100 500	 Ω	Differential To 3.3V at receiver To GND near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs
	IL/FEXT plot: See HDMI Guideline Figure 8-9		TDR plot: See Figure 8-10
Impedance			

Parameter	Requirement	Units	Notes
Trace impedance: Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	GND		
Trace spacing/Length/Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. See Note 1.
Trace spacing (pair-pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	 3x 4x 5x to 7x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main link to DDC) Stripline Microstrip	 3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max total length/delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 100 (690) 90 (531) 100 (590)	mm (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip). Stripline is preferred.
Max Total Length/Delay (Pre-1.4b - (up to 165Mhz) Microstrip Stripline	 254 (1500) 225 (1500)	mm (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max GND transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	- Y-pattern is recommended - keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See Figure 8-11
Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	uM	
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of vias PTH via u-via	 2 if all vias are PTH via Not limited if total channel loss meets IL spec.		
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main route via dimensions should comply with the via structure rules (See via section)			See topology in Figure 8-8
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			

Parameter	Requirement	Units	Notes
Example of a case where space is limited for placing components.	Top: See Figure 8-12		Bottom: See Figure 8-12
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-via design	 Place cap on bottom layer if main route above core Place cap on top layer if main route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		See Figure 8-13
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		Placement: See Figure 8-15
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between R_{PD} and FET choke Max trace Rdc Max trace length	 600 or 1 ≤20 4	 Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) See Chapter 17 for details on CMC if implemented.			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR
Footprint	Pad right on the net instead of trace stub		See Figure 8-16
Location	After pull-down resistor/CMC and before R_S		
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		See Figure 8-17
Series Resistor (R_S) – Series resistor on N/P path for HDMI 2.0 (mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	GND/PWR void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		See Figure 8-18
Trace between components	Uncoupled structure		See Figure 8-19
HDMI connector			

Parameter	Requirement	Units	Notes
Connector voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		See Figure 8-20
General: See Chapter 17 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

The following figures show the HDMI interface signal routing requirements.

Figure 8-9. IL/FEXT Plot

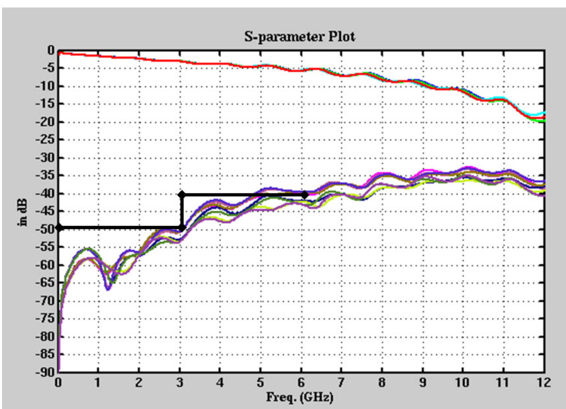


Figure 8-10. TDR Plot

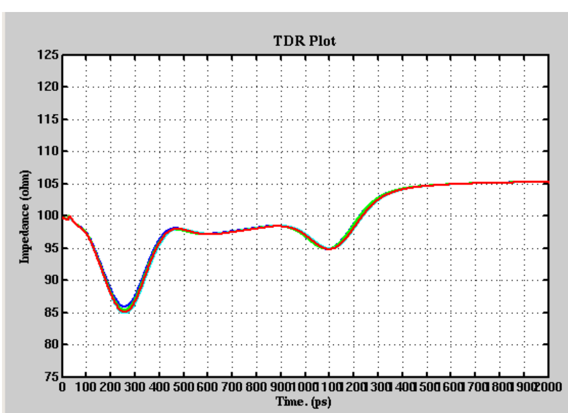


Figure 8-11. HDMI Via Topology

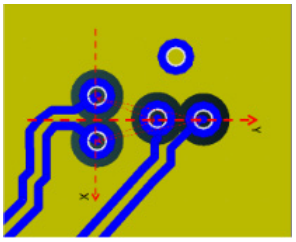


Figure 8-12. Add-On Components – Top

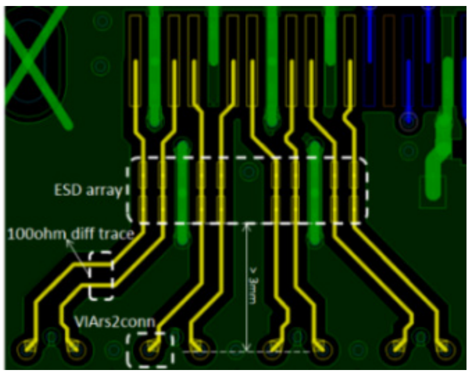


Figure 8-13. Add-on Components – Bottom

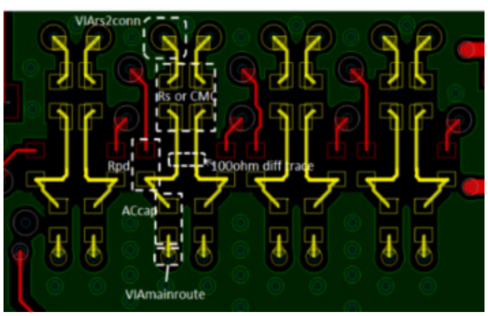


Figure 8-14. AC Cap Void

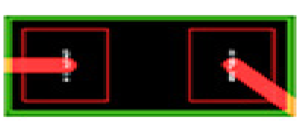


Figure 8-15. RPD/Choke, FET Placement

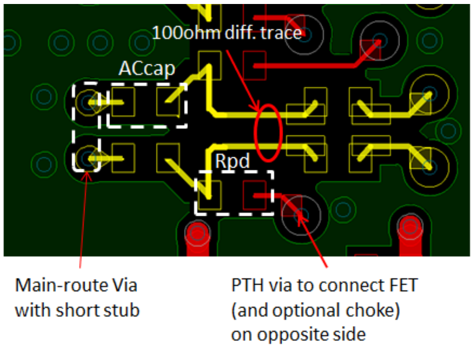


Figure 8-16. ESD Footprint

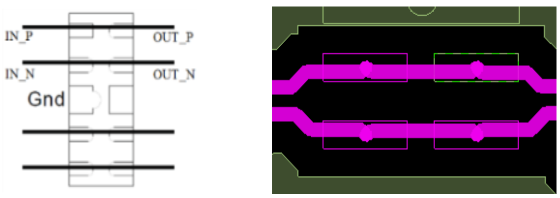


Figure 8-17. ESD Void

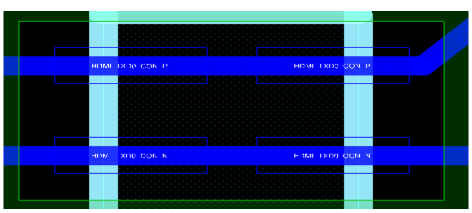


Figure 8-18. SMT Pad Trace Entering

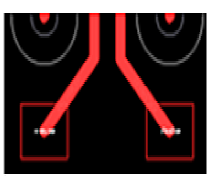


Figure 8-19. SMT Pad Trace Between

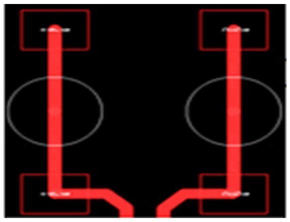


Figure 8-20. Connector Voiding

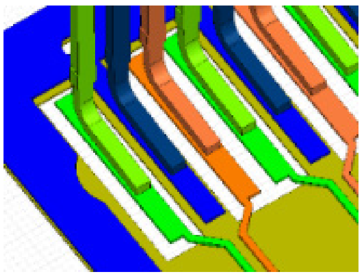


Table 8-6. HDMI Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DPx_TXD3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → ESD to GND →.≤6Ω R_S (series resistor)	**HDMI Differential Clock:** Connect to **C–/C+** and pins on HDMI connector
DPx_TXD[2:0]_N/P	DIFF OUT		**HDMI Differential Data:** Connect to HDMI Data pins (See Table 8-2)
DPx_HPD	I	From module pin: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to GND on connector side → 100pF/12pF caps to GND → ESD to GND.	**HDMI Hot Plug Detect:** Connect to **HPD** pin on HDMI connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure for details.	**HDMI Consumer Electronics Control:** Connect to CEC on HDMI connector through circuitry.
DPx_AUX_N/P	I/OD	From module pins: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → ESD to GND	**HDMI: DDC Interface – Clock and Data**: Connect DP1_AUX_N to SDA and DP1_AUX_P to SCL on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector and ESD to GND.	**HDMI 5V supply to connector: Connect to +5V on HDMI connector.**

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

Chapter 9. MIPI CSI Video Input

Jetson Xavier NX brings fourteen MIPI CSI lanes to the connector. Up to three quad-lane camera streams plus one dual-lane stream or up to six dual-lane camera streams are supported. Each data lane has a peak bandwidth of up to 2.5 Gbps.

Table 9-1. Jetson Xavier NX CSI Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	2-lane Camera #1, 4-lane Camera #1 (lower 2 lanes)	Input	MIPI D-PHY
12	CSI0_CLK_P	CSI_A_CLK_P				
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0			
6	CSI0_D0_P	CSI_A_D0_P				
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1			
18	CSI0_D1_P	CSI_A_D1_P				
9	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1 Clock	2-lane Camera #2, 4-lane Camera #1 (upper 2 lanes)		
11	CSI1_CLK_P	CSI_B_CLK_P				
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0			
5	CSI1_D0_P	CSI_B_D0_P				
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1			
17	CSI1_D1_P	CSI_B_D1_P				
28	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2 Clock	2-lane Camera #3, 4-lane Camera #2 (lower 2 lanes)		
30	CSI2_CLK_P	CSI_C_CLK_P				
22	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2 Data 0			
24	CSI2_D0_P	CSI_C_D0_P				
34	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2 Data 1			
36	CSI2_D1_P	CSI_C_D1_P				
27	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3 Clock	2-lane Camera #4, 4-lane Camera #2 (upper 2 lanes)		
29	CSI3_CLK_P	CSI_D_CLK_P				
21	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3 Data 0			
23	CSI3_D0_P	CSI_D_D0_P				
33	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3 Data 1			
35	CSI3_D1_P	CSI_D_D1_P				
52	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4 Clock			
54	CSI4_CLK_P	CSI_E_CLK_P				

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
46	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4 Data 0	2-lane Camera #5, 4-lane Camera #3 (lower 2 lanes)		
48	CSI4_D0_P	CSI_E_D0_P				
58	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4 Data 1			
60	CSI4_D1_P	CSI_E_D1_P				
40	CSI4_D2_N	CSI_F_D0_N	Camera, CSI 4 Data 2	4-lane Camera #3 (upper 2 lanes)		
42	CSI4_D2_P	CSI_F_D0_P				
64	CSI4_D3_N	CSI_F_D1_N	Camera, CSI 4 Data 3			
66	CSI4_D3_P	CSI_F_D1_P				
76	DSI_CLK_N	CSI_G_CLK_N	Camera, CSI 5 Clock	2-lane Camera #6		
78	DSI_CLK_P	CSI_G_CLK_P				
70	DSI_D0_N	CSI_G_D0_N	Camera, CSI 5 Data 0			
72	DSI_D0_P	CSI_G_D0_P				
82	DSI_D1_N	CSI_G_D1_N	Camera, CSI 5 Data 1			
84	DSI_D1_P	CSI_G_D1_P				

Notes: In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.

Table 9-2. Jetson Xavier NX Camera Miscellaneous Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C. 2.2kΩ pull-up to 3.3V on the module.	Cameras (shared)	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	CAM_I2C_SDA				
116	CAM0_MCLK	EXTPERIPH1_CLK	Camera 0 Reference Clock	Camera #1	Output	CMOS – 1.8V
114	CAM0_PWDN	SOC_GPIO04	Camera 0 Powerdown or GPIO			
122	CAM1_MCLK	EXTPERIPH2_CLK	Camera 1 Reference Clock	Camera #2		
120	CAM1_PWDN	SOC_GPIO05	Camera 1 Powerdown or GPIO			
118	GPIO01	SOC_GPIO41	GPIO #1 or Generic Clock Output #1	Camera #3	Output (note)	
216	GPIO11	SOC_GPIO42	GPIO #11 or Generic Clock Output #2	Camera #4		

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction shown in this table for CAM[1:0]_MCLK and CAM[1:0]_PWDN is true when used for those functions. These pins are GPIOs and can support input or output (bidirectional). The direction indicated for GPIO01 and GPIO11 is associated with their use as clock outputs.

Figure 9-1. 4 Lane CSI Camera Connection Example

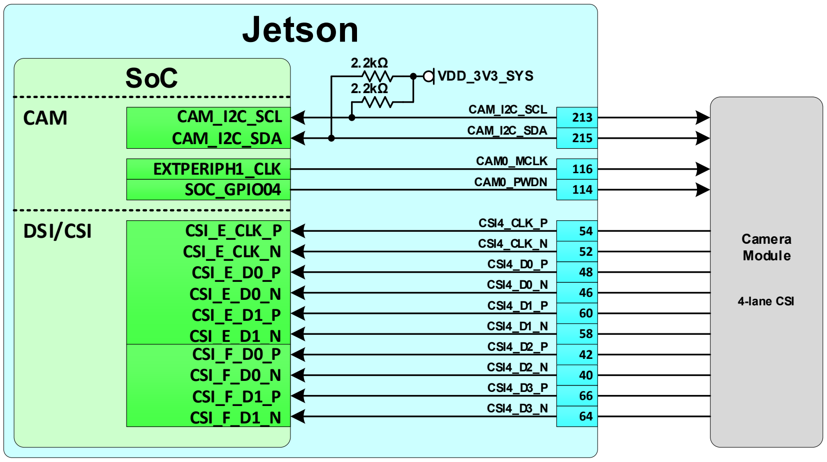


Table 9-3. CSI Configurations

Cameras	CSI0 CLK/Data[1:0]	CSI 1 CLK	CSI1 Data[1:0]	CSI2 CLK/Data[1:0]	CSI 3 CLK	CSI3 Data[1:0]	CSI4 CLK/Data[1:0]	CSI4 DATA[3:2]	CSI5 (DSI pins) CLK/Data[1:0]
2-Lanes Each									
1 of 6 cameras	√								
2 of 6 cameras		√	√						
3 of 6 cameras				√					
4 of 6 cameras					√	√			
5 of 6 cameras							√		
6 of 6 cameras									√
4-Lanes Each									
1 of 3 cameras	√		√						
2 of 3 cameras				√		√			
3 of 3 cameras							√	√	

Notes:

1. CSI 4 can be used as a x1, x2, or x4 CSI interface.
2. Each 2-lane options shown can also be used for one single lane camera.

Figure 9-2. CSI Connection Options

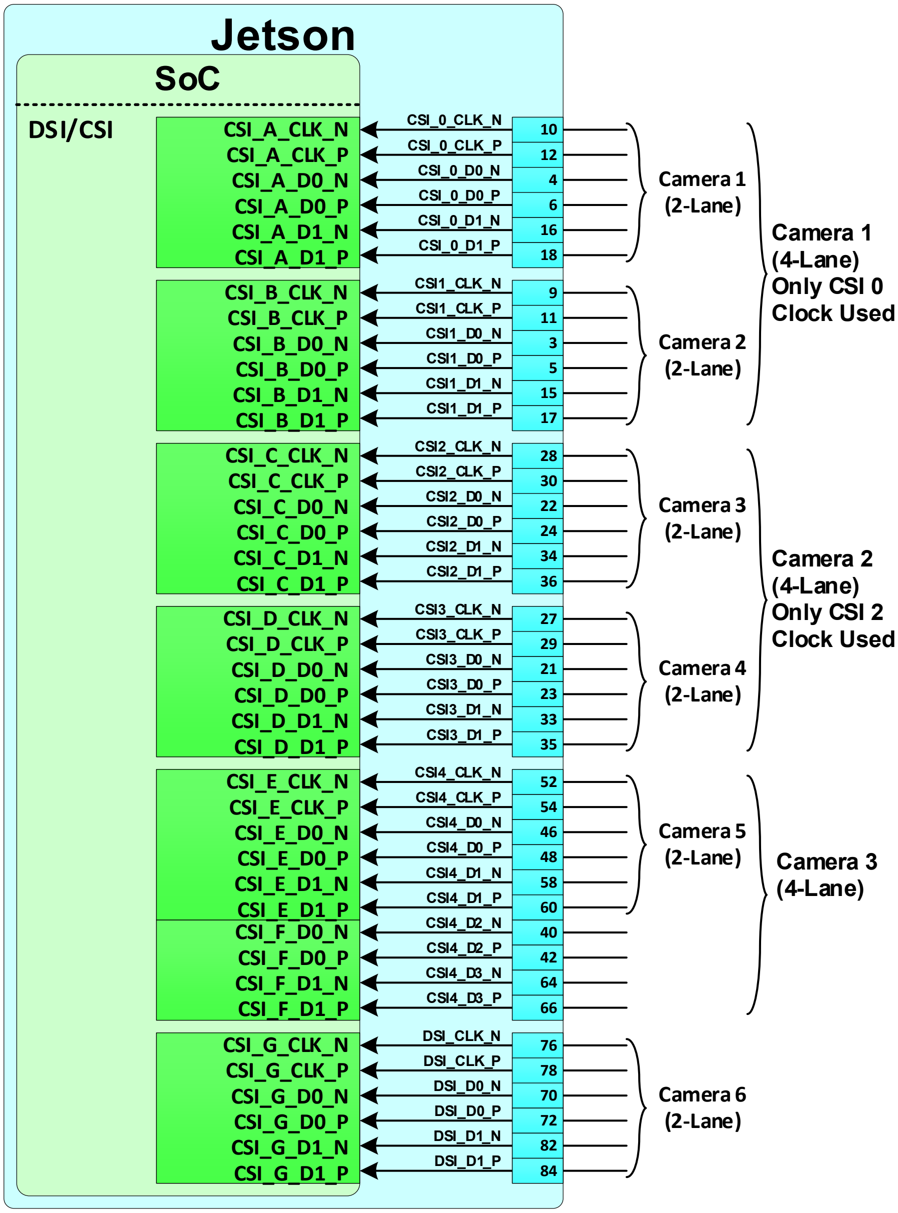
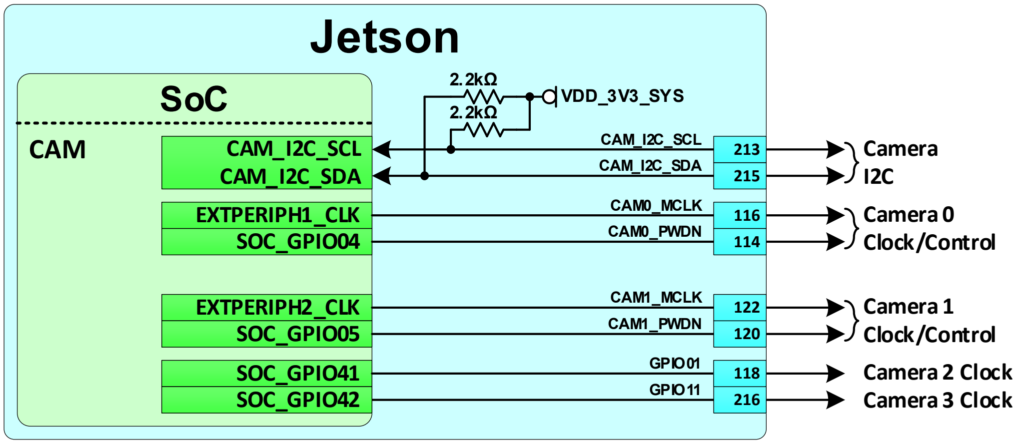


Figure 9-3. Available Camera Control Pins



9.1 CSI Design Guidelines

The following tables describe the design guidelines for the CSI design.

Table 9-4. MIPI CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of loads	1	load	
Reference plane	**GND**		
Trace impedance: Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance.
Trace spacing: Microstrip / Stripline	2x / 2x	dielectric	
Max PCB breakout delay	48	ps	
Max Insertion loss 1 Gbps 1.5 Gbps 2.5 Gbps	 3.00 2.90 1.92	 dB	
Max trace delay / length 1 Gbps (Stripline/Microstrip) 1.5 Gbps 2.5 Gbps	 2526 (421) / 2487 (421) 1913 (319) / 1885 (319) 900 (150) / 886 (150)	 ps (mm)	

Parameter	Requirement	Units	Notes
Max intra-pair skew	1	ps	
Max trace delay skew between **DQ** and **CLK** **1 / 1.5 / 2.5 Gbps**	40 / 26.7 / 16	ps	DQ includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			
Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.			

Table 9-5. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[4:0]_CLK_N/P Camera #[5:1] DSI_CLK_N/P Camera #6	I	See note	CSI Differential Clocks: Connect to clock pins of camera. See Table 9-3 for details
CSI[3:0]_D[1:0]_N/P Camera #[4:1] CSI4_D[3:0]_N/P Camera #5 DSI_D[1:0]_N/P Camera #6	I/O	See note	CSI Differential Data Lanes: Connect to data pins of camera. See Table 9-3 for details

Table 9-6. Miscellaneous Camera Connections

Module Pin Name	Type	Termination	Description
CAM_I2C_CLK CAM_I2C_DAT	O I/O	2.2kΩ pull-ups **VDD_3V3_SYS** (on Jetson Xavier NX).	**Camera I2C Interface:** Connect to I2C SCL and SDA pins of imager.
CAM[1:0]_MCLK GPIO01 (opt. MCLK2) GPIO11 (opt. MCLK3)	O		**Camera Master Clocks:** Connect to camera reference clock inputs.
CAM[1:0]_PWDN	O		**Camera Power Control signals (or GPIOs [1:0]):** Connect to power down pins on camera(s).

Chapter 10. SD Card and SDIO

Jetson Xavier NX uses one SDMMC interface for on-module eMMC (SDMMC4 on Xavier) and brings one to the connector pins for SD Card or SDIO use.

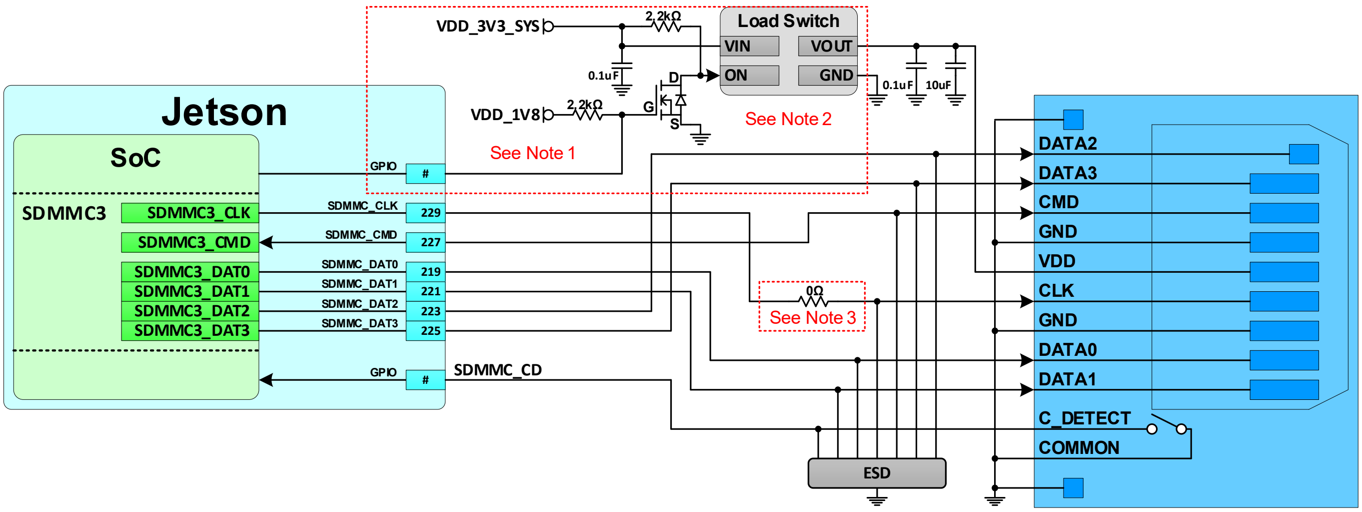
Table 10-1. Jetson Xavier NX SDIO Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock	SD Card or SDIO Device	Output	CMOS – 1.8V/3.3V
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command		Bidir	
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0			
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1			
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2			
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3			

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction shown in the table above for SDMMC_CLK is true when used for that function. If used as a GPIO, the pin supports input or output (bidirectional).
3. If the SDMMC pins are connected to a 1.8V only device, the interface voltage should be configured for 1.8V operation in the Pinmux.

Figure 10-1. SD Card Connection Example



> **Notes:**
> 1. The supply or load switch for the SD Card VDD must be enabled with a GPIO from Jetson. This is required for correct operation after a warm boot. The GPIO used should be selected so VDD is not powered on by default.
> 2. The supply (regulator, load switch, etc.) used to supply the SD Card VDD rail should be current limited if the supply is shorted to GND.
> 3. Having 0Ω, 0402 resistor is recommended in case of issues with EMI where it can be replaced with an appropriate device.

Table 10-2. SD Card and SDIO Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency 3.3V Signaling DS HS 1.8V Signaling SDR12 SDR25 SDR50 SDR104 DDR50	 25 (12.5) 50 (25) 25 (12.5) 50 (25) 100 (50) 208 (104) 50 (50)	 MHz (MB/s)	See Note 1
Topology	Point to point		
Reference plane	GND or PWR		See Note 2
Trace impedance	50	Ω	±15%. 45Ω optional depending on stack-up
Max via count			Independent of stack-up layers.

Parameter	Requirement	Units	Notes
PTH HDI	4 10		Depends on stack-up layers.
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	Up to four signal vias can share 1 GND return via
Trace spacing – Microstrip / Stripline	4x / 3x	dielectric	
Trace length SDR50 / SDR25 / SDR12 / HS / DS Min Max SDR104 / DDR50 Min Max	 16 (100) 139 (876) 16 (100) 83 (521)	mm (ps)	
Max trace length/delay skew in/between CLK and CMD/DAT SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	14 (87.5) 2 (12.5)	mm (ps)	See Note 3
Keep CLK, CMD and DATA traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.

Table 10-3. SD Card and SDIO Signal Connections

Function Signal Name	Type	Termination	Description
SDMMC_CLK	O		SD Card / SDIO Clock: Connect to CLK pin of device.
SDMMC_CMD	I/O		SD Card / SDIO Command: Connect to CMD pin of device
SDMMC_D[3:0]	I/O		SD Card / SDIO Data: Connect to Data pins of device
GPIO	I		SD Card Detect (Optional): Connect available GPIO on module to CD pin of SD Card socket.

Chapter 11. Audio

Xavier supports multiple PCM and I2S audio interfaces. It also includes a flexible audio port switching architecture.

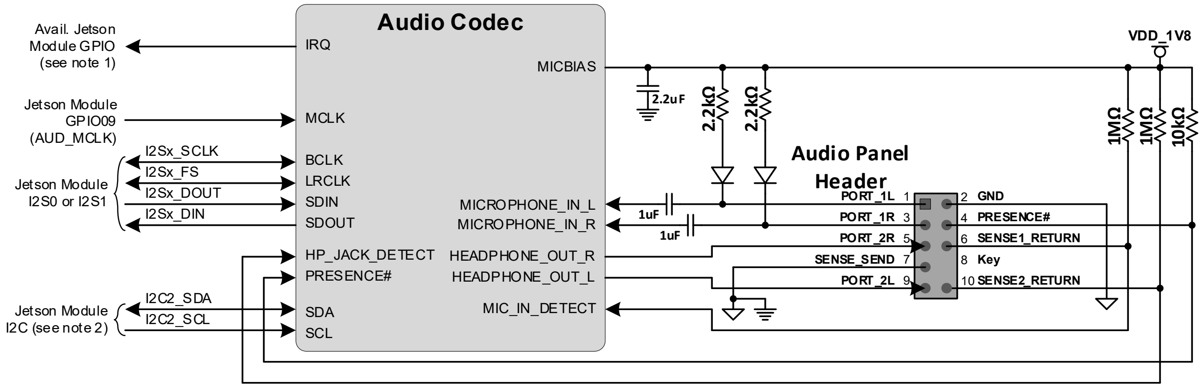
Table 11-1. Jetson Xavier NX Audio Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
199	I2S0_SCLK	DAP5_SCLK	I2S Audio Port 0 Clock	Audio Device	Bidir	CMOS – 1.8V
197	I2S0_FS	DAP5_FS	I2S Audio Port 0 Left/Right Clock		Bidir	
193	I2S0_DOUT	DAP5_DOUT	I2S Audio Port 0 Data Out		Output (note)	
195	I2S0_DIN	DAP5_DIN	I2S Audio Port 0 Data In		Input (note)	
226	I2S1_SCLK	DAP3_SCLK	I2S Audio Port 1 Clock	Audio Device (i.e. M.2 Key E)	Bidir	
224	I2S1_FS	DAP3_FS	I2S Audio Port 1 Left/Right Clock		Bidir	
220	I2S1_DOUT	DAP3_DOUT	I2S Audio Port 1 Data Out		Output (note)	
222	I2S1_DIN	DAP3_DIN	I2S Audio Port 1 Data In		Input (note)	
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Audio Device	Output (note)	

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction indicated for I2S[1:0]_DOUT and _DIN are associated with their use as I2S data lines. The direction for GPIO09 is associated with its use as Audio Master Clock. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 11-1. Audio Codec Connection Example



Notes:

1. The Interrupt pin from the audio codec can connect to any available Jetson Xavier NX GPIO. If the pin must be wake-capable, choose one of the GPIOs that supports this function.
2. I2C2 supports 1.8V operation since the interface is pulled to 1.8V through 4.7kΩ resistors on the module. If another I2C interface on Jetson Xavier NX is used, a level shifter will be required as all the others are 3.3V.
3. Refer to the Intel High Definition Audio/AC'97 website for the latest information: https://www.intel.com/content/www/us/en/support/articles/000005512/boards-and-kits/desktop-boards.html.

Table 11-2. I2S Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Configuration / device organization		1	load	
Max loading		8	pF	
Reference plane		GND		
Breakout region impedance		Min width/spacing		
Trace impedance		50	Ω	±20%
Via proximity (signal to reference)		< 3.8 (24)	mm (ps)	See note 1
Trace spacing	Microstrip or Stripline	2x	dielectric	
Max trace length/delay		~22 (3600)	In (ps)	See note 2
Max trace length/delay skew between **SCLK** and SDATA_**OUT/IN**		~1.6 (250)	In (ps)	See note 2

Note: Up to four signal vias can share a single GND return via.

Table 11-3. Audio Signal Connection

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		**I2S Serial Clock:** Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		**I2S Frame Select (Left/Right Clock):** Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		**I2S Data Output:** Connect to data input pin of audio device.
I2S[1:0]_DIN	I		**I2S Data Input:** Connect to data output pin of audio device.
GPIO09	O		**Audio Codec Master Clock:** Connect to clock pin of audio codec.

Chapter 12. Miscellaneous Interfaces

12.1 I2C

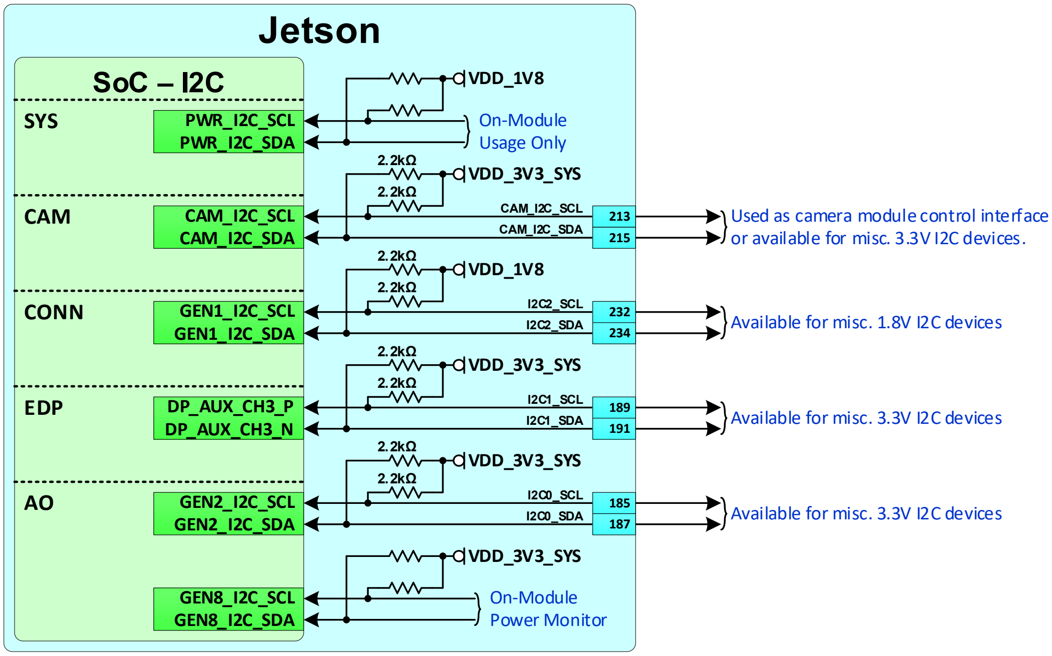
Jetson Xavier NX brings four I2C interfaces to the connector pins. **CAM_I2C** is included in the camera pin description table earlier in this design guide. The assignments in the "I2C Interface Mapping" table should be used where applicable for the I2C interfaces.

Table 12-1. Jetson Xavier NX I2C Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
185	I2C0_SCL	GEN2_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (general)	Bidir	Open Drain – 3.3V
187	I2C0_SDA	GEN2_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
189	I2C1_SCL	DP_AUX_CH3_P	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
191	I2C1_SDA	DP_AUX_CH3_N	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
232	I2C2_SCL	GEN1_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V
234	I2C2_SDA	GEN1_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.

Figure 12-1. I2C Connections



12.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson Xavier NX do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format). The I2C2 interface is connected to an EEPROM on the module which uses I2C address 7'h50.

Notes:

1. The Jetson Xavier NX I2C interfaces have 2.2 kΩ pull-ups on the module. Pads for additional pull-ups are recommended in case a stronger pull-up is required due to additional loading on the interfaces.
2. IF I2C interfaces are routed to M.2 Key E or Key M connectors, it is recommended that 0Ω series be included to allow these to be disconnected. Some M.2 Key E and Key M cards can cause conflicts with other devices connected to the I2C interfaces.

Table 12-2. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency: Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple masters/slaves		
Max loading: Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace impedance	50 – 60	Ω	±15%
Trace spacing	1x	dielectric	
Max trace length/delay Standard Mode Fm, Fm+ Modes	 3400 (~20) 1700 (~10)	ps (in)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference.

Table 12-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C0_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**I2C #0 Clock and Data.** Connect to CLK and Data pins of any 3.3V devices
I2C1_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**I2C #1 Clock and Data.** Connect to CLK and Data pins of 3.3V devices.
I2C2_SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_1V8** on Jetson Xavier NX	**I2C #2 Clock and Data.** Connect to CLK and Data pins of any 1.8V devices
CAM_I2C_ SCL/SDA	I/OD	2.2kΩ pull-ups to **VDD_3V3_SYS** on Jetson Xavier NX	**Camera I2C Clock and Data.** Connect to CLK and Data pins of any 3.3V devices

Notes:

1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

12.2 SPI

The Jetson Xavier NX brings out two of the Xavier SPI interfaces. See Figure 12-2.

Table 12-4. Jetson Xavier NX SPI Pin Descriptions

<table>
<tr><th>Pin #</th><th>Module Pin Name</th><th>Xavier Signal</th><th>Usage/Description</th><th>Recommended Usage</th><th>Direction</th><th>Pin Type</th></tr>
<tr><td>91</td><td>SPI0_SCK</td><td>SPI1_SCK</td><td>SPI 0 Clock</td><td rowspan="3">SPI #0 Device #0 or #1</td><td rowspan="4">Bidir</td><td rowspan="4">CMOS – 1.8V</td></tr>
<tr><td>93</td><td>SPI0_MISO</td><td>SPI1_MISO</td><td>SPI 0 Master In / Slave Out</td></tr>
<tr><td>89</td><td>SPI0_MOSI</td><td>SPI1_MOSI</td><td>SPI 0 Master Out / Slave In</td></tr>
<tr><td>95</td><td>SPI0_CS0*</td><td>SPI1_CS0</td><td>SPI 0 Chip Select 0</td><td>SPI #0 Device #0</td></tr>
</table>

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1	SPI #0 Device #1		
106	SPI1_SCK	SPI3_SCK	SPI 1 Clock	SPI #1 Device #0 or #1		
108	SPI1_MISO	SPI3_MISO	SPI 1 Master In / Slave Out			
104	SPI1_MOSI	SPI3_MOSI	SPI 1 Master Out / Slave In			
110	SPI1_CS0*	SPI3_CS0	SPI 1 Chip Select 0	SPI #1 Device #0		
112	SPI1_CS1*	SPI3_CS1	SPI 1 Chip Select 1	SPI #1 Device #1		

Notes: In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.

Figure 12-2. SPI Connections

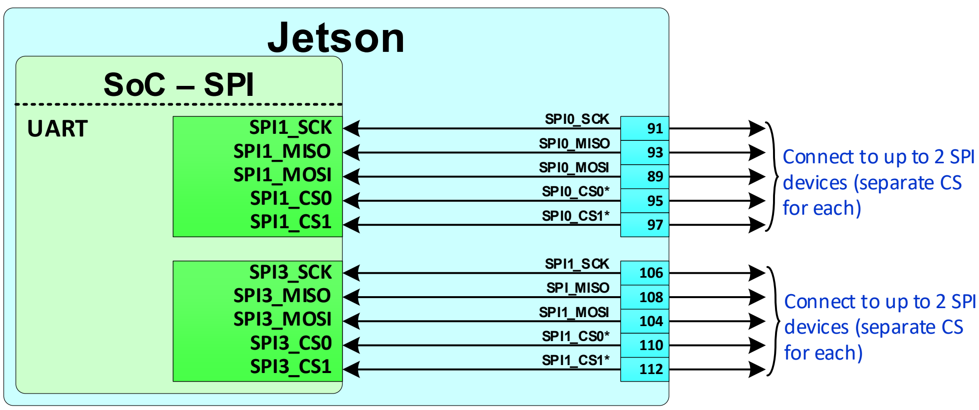
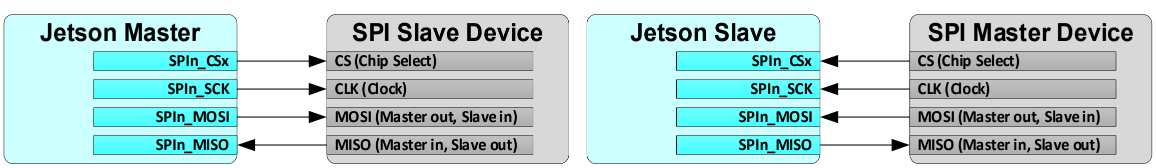


Figure 12-3 shows the basic connections used.

Figure 12-3. Basic SPI Master and Slave Connections



12.2.1 SPI Design Guidelines

The following guidelines meet the SPI design guidelines.

Figure 12-4. SPI Topologies

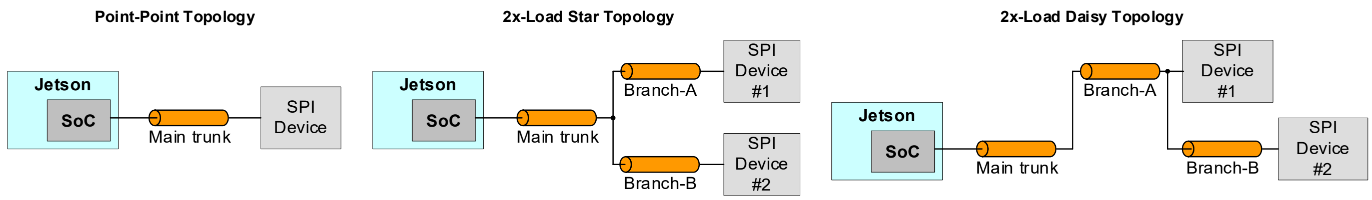


Table 12-5. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency	65	MHz	
Configuration / device organization	4	load	
Max loading (total of all loads)	15	pF	
Reference plane	GND		
Breakout region impedance	Minimum width and spacing		
Max PCB breakout delay	75	ps	
Trace impedance	50 – 60	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric	
Max trace length/delay (PCB main trunk) For **MOSI, MISO, SCK and CS** Point-point 2x-load star/daisy	195 (1228) 120 (756)	mm (ps)	
Max trace length/delay (Branch-A) for **MOSI, MISO, SCK** and **CS** 2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from **MOSI, MISO** and **CS** to **SCK**	16 (100)	mm (ps)	At any point

Note: Up to four signal vias can share a single GND return via

Table 12-6. SPI Signal Connections

Module Pin Names (Function)	Type	Termination	Description
SPI[1:0]_CLK	I/O		**SPI Clock.**: Connect to peripheral CLK pin(s)
SPI[1:0]_MOSI	I/O		**SPI Data Output**: Connect to slave peripheral MOSI pin(s)
SPI[1:0]_MISO	I/O		**SPI Data Input**: Connect to slave peripheral MISO pin(s)
SPI[1:0]_CS[1:0]*	I/O		**SPI Chip Selects.**: Connect one CSx* pin per SPI interface to each slave peripheral CS pin on the interface

12.3 UART

The Jetson Xavier NX brings three UARTs out to the main connector. See Figure 12-5 for typical assignments of the three available UARTs.

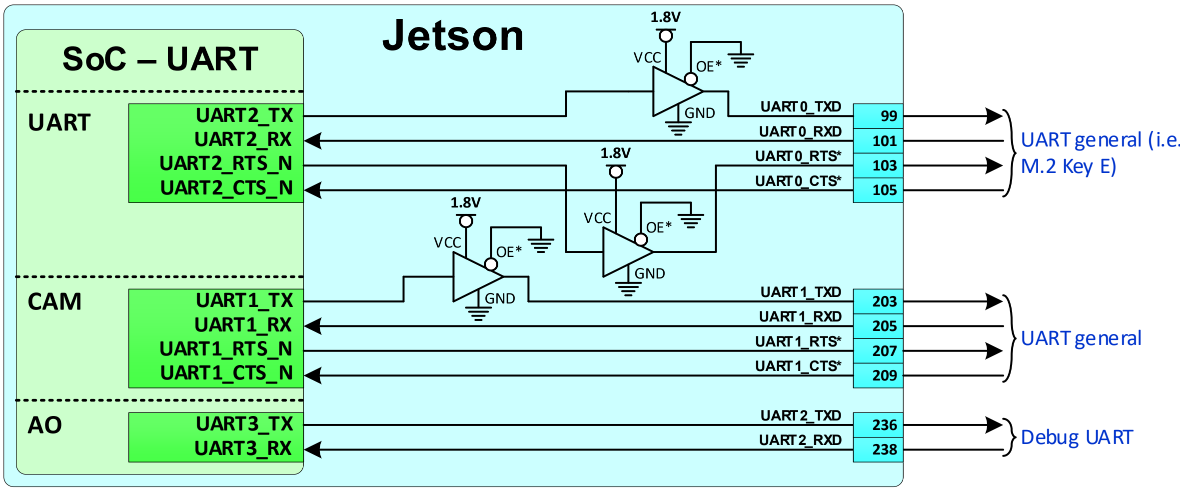
Table 12-7. Jetson Xavier NX UART Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
99	UART0_TXD	UART2_TX	UART 0 Transmit	UART general (i.e. M.2 Key E)	Output	CMOS – 1.8V
101	UART0_RXD	UART2_RX	UART 0 Receive		Input	
103	UART0_RTS*	UART2_RTS	UART 0 Request to Send		Output	
105	UART0_CTS*	UART2_CTS	UART 0 Clear to Send		Input	
203	UART1_TXD	UART1_TX	UART 1 Transmit	UART general	Output	
205	UART1_RXD	UART1_RX	UART 1 Receive		Input	
207	UART1_RTS*	UART1_RTS	UART 1 Request to Send		Output	
209	UART1_CTS*	UART1_CTS	UART 1 Clear to Send		Input	
236	UART2_TXD	UART3_TX	UART 2 Transmit.	Debug UART	Output	
238	UART2_RXD	UART3_RX	UART 2 Receive		Input	

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction indicated for the UART pins except for is true when used for that function. Otherwise, these pins support GPIO functionality and most can support both input and output (bidirectional) functionality. The exception is UART0_TXD, UART0_RTS* and UART1_TXD. These have output-only buffers on the module to keep them from being affected by connected devices during boot as they are associated with SoC strapping pins.

Figure 12-5. Jetson Xavier NX UART Connections



Note: The buffers on UART0_TXD, UART0_RTS* and UART1_TXD are there to prevent connected devices from changing the pin state during power-on. These pins are associated with SoC Strapping pins.

Table 12-8. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TXD	O		UART Transmit: Connect to peripheral RXD pin of device
UART[2:0]_RXD	I		UART Receive: Connect to peripheral TXD pin of device
UART[1:0]_CTS*	I		UART Clear to Send: Connect to peripheral RTS pin of device
UART[1:0]_RTS*	O		UART Request to Send: Connect to peripheral CTS pin of device

12.4 CAN

Jetson Xavier NX brings a single controlled area network (CAN) interface to the main connector.

Table 12-9. Jetson Xavier NX CAN Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
143	CAN_RX	CAN0_DIN	CAN Receive	CAN PHY	Input	CMOS – 3.3V
145	CAN_TX	CAN0_DOUT	CAN Transmit		Output	CMOS – 3.3V

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction indicated for the CAN signals are associated with that usage. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 12-6. Jetson Xavier NX CAN Connections

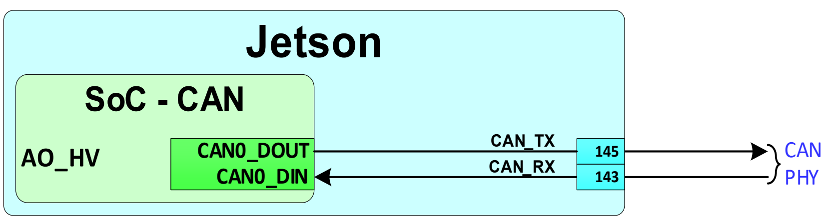


Table 12-10. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	5	Mbps / MHz	
Configuration / Device Organization	1	load	
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length (for RX & TX only)	223 (1360)	mm (ps)	See Note 2
Max Trace Length/Delay Skew from RX to TX	8 (50)	mm (ps)	See Note 2

Table 12-11. CAN Signal Connections

Module Pin Name	Type	Termination	Description
CAN_TX	O		CAN Transmit: Connect to matching pin of device
CAN_RX	I		CAN Receive: Connect to Peripheral pin of device

12.5 Fan

Jetson Xavier NX provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins and functions can be found in the following locations:

- Jetson Xavier NX Pin Mux
  - This is used to configure GPIO14 (PWM) for **FAN_PWM** and GPIO08 for **FAN_TACH**. The pin used for **FAN_PWM** is configured as **GP_PWM6**. The pin used for **FAN_TACH** is configured as a GPIO.
- Xavier (SoC) Technical Reference Manual (TRM)
  - Functional descriptions and related registers can be found in the TRM for the **FAN_PWM** (PWM chapter).

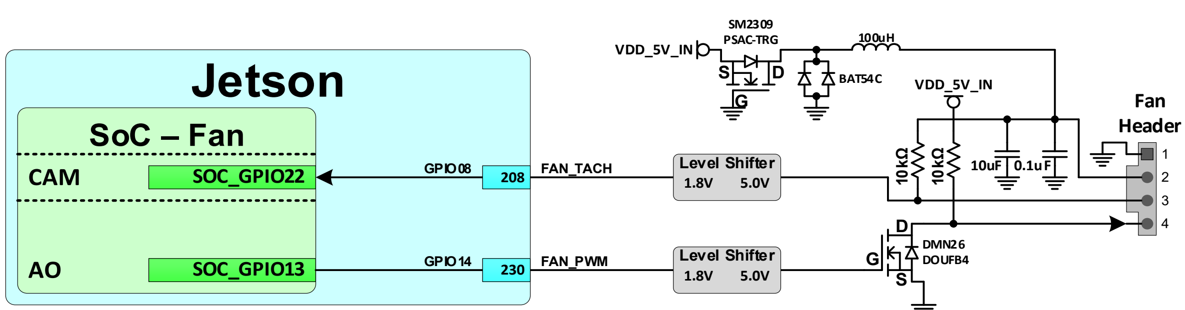
Table 12-12. Jetson Xavier NX Fan Pin Descriptions

Pin #	Module Pin Name	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
230	GPIO14	SOC_GPIO13	Fan PWM	Fan	Output (note)	CMOS – 1.8V
208	GPIO08	SOC_GPIO22	Fan tachometer	Fan	Input (note)	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.
2. The direction indicated for GPIO014 and GPIO08 is associated with their use as Fan PWM/Tach. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 12-7. Jetson Xavier NX Fan Connections



12.6 Debug

Jetson Xavier NX supports a UART for debugging purposes. The UART intended for debug is UART2 with is routed to a level shifter then to a 12-pin automation header on the developer kit carrier board.

Table 12-13. Jetson Xavier NX Debug UART Pin Descriptions

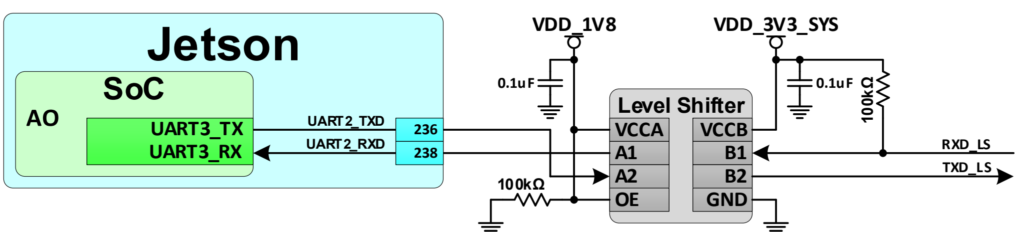
Pin #	Module Pin Name (see note 4)	Xavier Signal	Usage/Description	Recommended Usage	Direction	Pin Type
238	UART2_RXD	UART3_TX	UART 2 receive	Debug UART	Input	CMOS – 1.8V
236	UART2_TXD	UART3_RX	UART 2 transmit		Output	

Note: In the Type/Dir column, Output is from Jetson Xavier NX. Input is to Jetson Xavier NX. Bidir is for Bidirectional signals.

Table 12-14. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART2_TXD	O		UART #2 Transmit: Connect to RX pin of serial device
UART2_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Xavier NX side of the device.	UART #2 Receive: Connect to TX pin of serial device

Figure 12-8. Debug UART Connections



Note: If level shifter is implemented, pull-up is required on the RXD line on the non-Jetson Xavier NX side of the level shifter. This is required to keep the input from floating and toggling when no device is connected to the debug UART.

12.7 USB Recovery Mode

USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed. To enter USB recovery mode, the **FORCE_RECOVERY*** pin is held low when **SYS_RESET*** goes high which can be when the system is powered on or **SYS_RESET*** is asserted after the system is powered on.

- **FORCE_RECOVERY*** is the SoC RCM0 strap.
- Only **USB0_D_N/P** supports USB Recovery Mode.

No other signals are required or supported for entering Force Recovery mode. Neither VBUS or ID detection is needed. As long as the force recovery strap is held low coming out of reset, Jetson Xavier NX will configure USB0 as a device and enter recovery mode.

See the USB section (Section 6.1) for an example figure that shows USB0 connected to a USB Micro B connector.

Chapter 13. PADS

Jetson Xavier NX signals that come from the SoC may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

13.1 Internal Pull-ups for Dual Voltage Block Pins Power at 1.8V

Several of the MPIO pads are on blocks designed to be powered at either 1.8V or 3.3V. These blocks are powered at 1.8V on Jetson Xavier NX, and the internal pull-up at initial Power-ON is not effective. The signal may only be pulled up a fraction of the 1.8V rail. Once the system boots, software can configure the pins for 1.8V operation and the internal pull-ups will work correctly. If these signals need the pull-ups during Power-ON, external pull-up resistors should be added. The following pins listed are the affected pins. These are the Jetson Xavier NX pins on the dual voltage blocks powered at 1.8V with Power-ON reset default of Internal pull-up enabled.

- SDMMC_DAT0
- SDMMC_DAT1
- SDMMC_DAT2
- SDMMC_DAT3
- SDMMC_CMD
- SPI1_CS0*
- SPI1_CS1*

13.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt-trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt-trigger mode provides better noise immunity and can help avoid extra edges from being "seen" by the Xavier inputs. Input clocks include the I2S and SPI clocks (**I2Sx_SCLK** and **SPIx_SCK**) when Xavier is in slave mode. The **FAN_TACH** pin [GPIO8] is another input that could be affected by noise on the signal edges. The **SDMMC_CLK** pin, while used to output the clock, also sample the clock at the input to help with read timing. Therefore, the **SDMMC_CLK** pin may benefit from enabling Schmitt-trigger mode. Care should be taken if the Schmitt-trigger mode setting is changed from the default initialization mode as this can influence interface timing.

13.3 Pins Pulled or Driven High During Power-ON

The Jetson Xavier NX is powered up before the carrier board (See Section 5.1 for power sequencing). Table 13-1 lists the pins on Jetson Xavier NX that default to being pulled or driven high. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer/shifter should be disabled until the device power is enabled.

Table 13-1. Pins Pulled or Driven High by Xavier Prior to SYS_RESET* Inactive

Jetson Xavier NX Pin	Power-ON reset Default	Pull-up Strength (kΩ)		Jetson Xavier NX Pin	Power-ON reset Default	Pull-up Strength (kΩ)
SYS_RESET*	Driven high	na		SPI0_CS0*	Internal pull-up	~15
SLEEP/WAKE*	Internal pull-up	~100		SPI0_CS1*	Internal pull-up	~15
FORCE_RECOVERY*	Internal pull-up	~100		SPI1_CS0*	Internal pull-up	~18
UART1_RXD	Internal pull-up	~100		SPI1_CS1*	Internal pull-up	~18

Table 13-2. Pins with External Pull-ups to Supply on before SYS_RESET* Inactive

Jetson Xavier NX Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)		Jetson Xavier NX Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)
I2C0_SCL/SDA	3.3	2.2		SPI1_CS0*	1.8	100
I2C1_SCL/SDA	3.3	2.2		SPI1_CS1*	1.8	100
I2C2_SCL/SDA	1.8	2.2		PCIE[1:0]_CLKREQ*	3.3	47
CAM_I2C_SCL/SDA	3.3	2.2		PCIE[1:0]_RST*	3.3	4.7
				PCIE_WAKEN	3.3	100

Chapter 14. Unused Interface Terminations

14.1 Unused Multi-purpose Standard CMOS Pad Interfaces

The following Jetson Xavier NX pins (and groups of pins) are Xavier MPIO pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in Table 14-1 that are not used can be left unconnected.

Table 14-1. Unused MPIO Pins and Pin Group

Jetson Xavier NX Pins / Pin Groups		Jetson Xavier NX Pins / Pin Groups
FORCE_RECOVERY*		SDMMC
GPIO00		I2S
PCIE[1:0]_CLK/RST/CLKREQ/WAKE		UART
GPIO xx		I2C
DP0_HPD, DP1_HPD, HDMI_CEC		SPI
CAM Control, Clock		

14.2 Unused Dedicated Special Purpose Pad Interfaces

See the Unused SFIO (Special Function I/O) interface pins section in the design checklist attached to this design guide.

Chapter 15. Design and Bring-Up Checklists

The design checklist is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design. The bring-up checklist is intended to provide basic items to check during bring-up for power delivery and the various interfaces used in a design.

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents. Excel files with the .nvxlsx extension will need to be renamed to .xlsx to open.

Chapter 16. Jetson Xavier NX Pin Descriptions

The Jetson Xavier NX pin description is attached to this design guide.

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents. Excel files with the .nvxlsx extension will need to be renamed to .xlsx to open.

Chapter 17. General Routing Guidelines

17.1 Signal Name Conventions

The following conventions are used in describing the signals for Xavier:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDMMC_CMD**, written in bold to distinguish it from other text. All active-low signals are identified by an asterisk (*) after the signal name. For example, **SYS_RESET*** indicates an active-low signal. Active-high signals do not have the underscore-N (**_N**) after the signal names. For example, **SDMMC_CMD** indicates an active-high signal. Differential signals are identified as a pair with the same names that end with **_P** and **_N** or for USB 2.0, DP and DN (for positive and negative, respectively). For example, **CSI_0_D0_P** and **CSI_0_D0_N** indicate a differential signal pair.
- The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The following table lists the I/O codes used in the signal description tables.

Table 17-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

17.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils (1/1000 of an inch) unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in "mm" (millimeter) or "in" (inch) or in terms of signal delay in "ps" (pico-seconds) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

17.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

- SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing
  - SE impedance of trace (along with diff impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline. Note: 1 mil = 1/1000th of an inch.

> **Note**: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

17.4 Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.1, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

- Controlled Impedance
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified SE and Diff impedances. Unless otherwise noted, trace impedance values are ±15%.

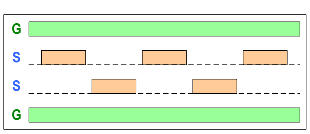
- Max Trace Lengths/Delays
  Trace lengths/delays should include the carrier board PCB routing (where the Jetson Xavier NX mating connector resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson Xavier NX to the actual connector (i.e. USB, HDMI, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- Trace Delay/Flight Time Matching
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) and inner-layer 180psi. If one signal is routed 10 inches on outer layer and second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

17.4.1 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see Figure 17-1).

Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.

Figure 17-1. General PCB Routing Guidelines



> **Note**: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

17.5 Common High-Speed Interface Requirements

The following table describes the common high-speed interface requirements.

Table 17-2. Common High-Speed Interface Requirements

Parameter	Requirement	Units	Notes
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues)			
Preferred device			Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. Refer to Common Mode Choke Requirement section.
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)	8 (53)	mm (ps)	TDK ACM2012D-900-2P See Figure 17-2
Common-mode impedance @ 100MHz Min/Max	65/90	Ω	
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω	@T_R-200ps (10%-90%)
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Serpentine			
Min bend angle	135	deg (α)	S1 must be taken care in order to consider Xtalk to adjacent pair. See USB 3.1 Guideline in Figure 17-3.
Dimension — Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical high-speed traces away from other signal traces or unrelated power traces/areas or power supply components		

The following figures show the common high-speed interface signal routing requirements.

Figure 17-2. Common Mode Choke

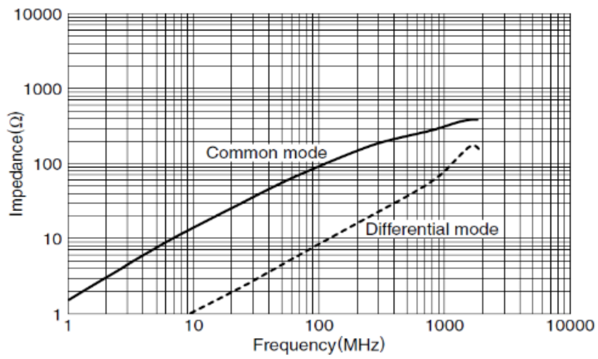
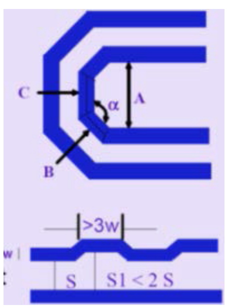


Figure 17-3. Serpentine



17.6 Test Points for High Speed Interfaces

Ideally, test points are not preferred on very high-speed interface traces as they can degrade signal integrity. However, to be able to do compliance testing, or interface tuning where applicable, it may be necessary to include test points at least for early revisions of a design. The test points are generally required near the receiver. If a connector or some other device (capacitor, resistor, and so on) exists near the receiver, the pins can be used as test points without creating additional signal degradation. Where connector or discrete device pins are not accessible near the receiver end of an interface, it may be necessary to include test points. When test points are needed for very high-speed interface signals, follow these recommendations:

- Test points should be very small (less than 0.5 mm).
- Test points should be located on the existing trace (no stub).
- If the test points are placed on differential signals, they should be symmetric for each P and N signal.