Circuit Theory and Electronics Fundamentals - T4

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Abstract

In this report, we focus on a signal applicator, directed to audio, converting a 10mV signal into a signal with around 100V, however this amplification is not the same for all frequencies, making the work focused on the optimization of the circuit to obtain a bigger and more useful amplification band as well as a bigger gain. With these objectives, a theoretical analysis and a simulation analysis were made using *Ngspice*. In the end, a bandwidth of 1.571×10^6 was reached and a gain of 37.29 in dB.

Resumo

Neste relatório, debruçamo-nos sobre um aplificador de sinal, direcionado a audio, convertendo um sinal de 10mV num sinal com cerca de 100V, contudo esta amplificação não é igual para todas as frequências, fazendo com que o trabalho se focasse na otimização do circuito de modo a obter uma maior e mais útil banda de amplificação assim como um maior ganho. Com estes objetivos, foram feitas uma análise teórica e uma análise de simulação utilizando o *Ngspice*. No final atingiu-se uma banda de 1.571×10^6 e um ganho de 37.29 em dB.

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1 Introduction

The main goal of this laboratory assignment is to analyse and better understand how an audio amplifier works and to design it having in mind that it should have a good relation efficiency-price. So, one has to find an optimal solution for the circuit built, which corresponds to a circuit that minimizes the cost, based not only in the number of component but on the type of them (see price table 1), maximizing the amplifying bandwidth and minimizing the lower cutoff frequency. This is because the frequencies that are more difficult to achieve in a amplifier like the one analysed are the lower ones.

To calculate the total cost associated to this circuit, one considered that it equals the sum of the cost of the resistors, capacitors and transistors. This maximization process can be compacted in a function called merit.

Component	Price
Resistors	1 MU $k\Omega^{-1}$
Capacitors	1 MU μF^{-1}
Transistors	0.1 MU transistor^{-1}

Table 1: Price table for the components used

$$M = \frac{10 \log\left(\frac{V_{in}}{V_{out}}\right) * \text{bandwidth}}{\text{Cost} * \text{LowerCutOffFrequency}} \quad (1)$$

The bandwidth corresponds to the difference between the higher cutoff frequency and the lower cutoff frequency, and those being defined by the frequencies from which the gain is lower than 3dB compared with the maximum value obtained. The V_{in}'s maximum value is set at $10mV$ (mandatory) in order for the goal to be well defined. Additionally to the components seen in the price table 1, we also use a voltage source of $12V$ that will have an important role in the amplification of the input voltage.

The circuit can also be divided in 2 main regions: the gain stage and the output stage. The gain stage has the main goal of amplifying the signal, as it is suggested by its name, and the output stage to reduce the impedance of the circuit that is connected to the output audio emitter of 8Ω. This is necessary because having a high output impedance, Zo, in the circuit would make all the current pass through the audio emitter, wasting significant amounts of power and increasing the distortion of the signal. On the other hand, with the goal of averting the degradation of the input voltage, one must have a high input impedance, Zi

Furthermore, and considering all the points mentioned before, the circuit used for this purpose was the following:

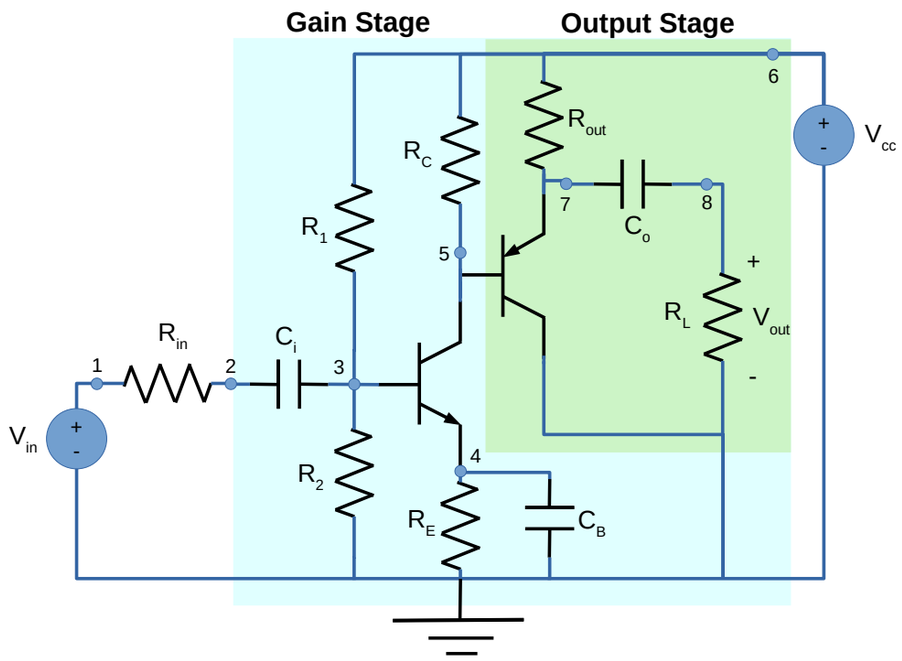


Figure 1: *Circuit analysed. The fixed values are V_{in} at $10mV$, being of any frequency from 0 to 10^8 Hz, V_{cc} at $12V$ and the two resistors R_{in} with 100Ω and R_L with 8Ω.*

The results were obtained through a theoretical analysis, in which one predicted the output by using a theoretical method that suited the real circuit and through a simulation that was made using *Ngspice*. The results obtained through both methods will be analysed throughout the report. However, because the models used in *Ngspice* are more correct than the ones used on the theoretical analysis, any type of optimization was done almost exclusively in the simulation analysis

2 Simulation Analysis and the Path for the Greater Good

For this analysis, we used the BC557A model for the PNP-transistor and the BC547A model for the NPN-transistor, from Philips available in *Ngspice*, having then created the circuit presented in Fig. 1 (it was using Ngspice that we determined, in fact, what was the best circuit for our purposes).

The use of a bypass capacitor, C_B, in parallel with a resistor on the gain stage has the main objective of "absorbing" AC noise in order to produce a cleaner DC signal. On the other hand, the output coupling capacitor used, C_o, is used to filter the signal, passing the wanted AC signal and blocking the undesired DC components. Finally, we also used a input coupling capacitor, which value should be sufficiently high to allow us to obtain a small value for the lower cutoff frequency.

Besides this there was not a lot more information to conclude what was the maximum of the function merit like a closed formula so our approach was based on incremental modification in order to understand the purpose of each component in the circuit each is was summarized in the effect on the gain (g), bandwidth (BW) and lower cutoff frequency (lCf).

It was concluded that the increase in C_O would decreses the lCf; the increase in R_{out} increses g and decreases BW; the increase in C_B decreases lCf; R_E and R_C increases seem to have a similar effect, decreasing BW, a by a lot less g and lCf; R_1 and R_2 seem to be very unstable needing to be at very special values to mantain the transistor in the active zone and at last C_i, increase causes a decrease in lCf. Then it was a matter of maximizing the merit function understanding what is being increased and decreased.

Finally, one found the values considered as the best to find an optimal merit score which are given by:

Component	**Value**	**Cost**	**Component**	**Value**	**Cost**
R_{in}	100Ω	0.1	C_i	135μF	135
R_1	$90k\Omega$	90	T_{NPN}	-	0.1
R_2	$10k\Omega$	10	T_{NPN}	-	0.1
R_E	120Ω	0.12	C_B	1840μF	1840
R_C	$2.3k\Omega$	2.3	R_{out}	330Ω	0.33
R_L	8Ω	0.008	C_o	1200μF	1200

Table 2: Values of the components used on Fig. 1.

2.1 Cost and Merit Score

Evaluating the merit, and knowing that the cost is given by (2)

$$cost = 2 \cdot 0.1 + (0.1 + 90 + 10 + 0.12 + 2.3 + 0.008 + 0.33) + (135 + 1840 + 1200) = 3278.06\text{MU} \quad (2)$$

2.2 Gain stage

To understand the role played by the gain stage this circuit one plotted the results obtained for the gain and phase at the end of this stage which is between node 5 and ground.

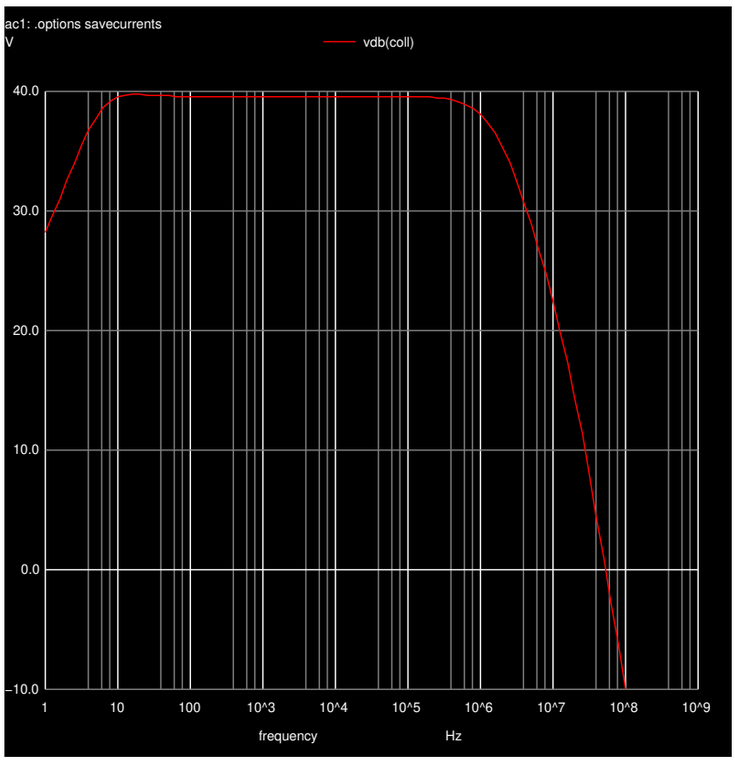


Figure 2: *Plot* obtained at the end of the gain stage

2.3 Output stage

In this stage the output signal will be analysed, which is the voltage difference in the resistor R_L, but the main goal of this stage is to minimize the output impedance.

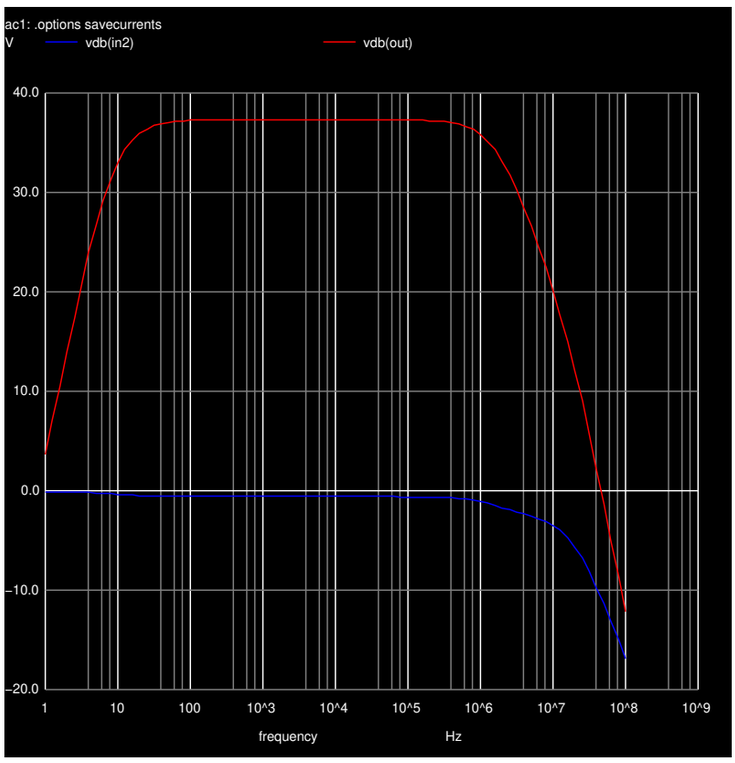


Figure 3: *Plot* obtained for the dB voltage at the circuit output and comparison with the initial dB voltage at the circuit input

2.4 Values obtained and impedances

Resuming, in the following table, we present the values obtained in *Ngspice* for some relevant quantities as the gain, the lower and higher cut-off frequencies, the bandwidth ort the final merit score obtained:

Quantity	Value
Gain	73.2378
Gain (dB)	37.2947 dB
Lower cut-off frequency	12.5855 Hz
Upper cut-off frequency	1.57176E+06 Hz
Bandwidth	1.57175E+06 Hz
Cost	3278.06 MU
Merit	2790.17

Table 3: Relevant quantities obtained on *Ngspice* simulation

As anticipated on the introduction, one should have a high input impedance and a small output impedance. The values obtained through the *Ngspice* simulation were for the input impedance were:

Quantity	Value
Zi	1385.89 + (-36.7344)j Ω
|Zi|	1386.38 Ω

Table 4: Values obtained for the input impedance

And for the output impedance were:

Quantity	Value
Zo	14.0507 + (0.625162)j Ω
|Zo|	14.0646 Ω

Table 5: Values obtained for the output impedance

3 Theoretical Analysis

The theoretical analysis can be subdivided in 3 parts

3.1 DC analysis

For the DC part, we followed a similar thought to the first code the teacher had which is: the capacitors block the current going through it! However, we chose to calculate the currents in such a way as to not divide the circuit in the same way the teacher's code did. Thus, if we define I_{xi}, where x can be c, e, b and i $1, 2$, as being the currents going in the collector, emitter and base, for each of the transistors, respectively, and I_{R1} and I_{R2} to be the currents going through the resistors R_1 and R_2, we can then retrieve all the important information from the circuit using the matrix in (3).

$$\begin{bmatrix} -\beta_1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\beta_2 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 1 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & R_2 & R_1 \\ 0 & R_c & R_e & R_c & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & R_{out} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{b1} \\ I_{c1} \\ I_{e1} \\ I_{b2} \\ I_{c2} \\ I_{e2} \\ I_{R1} \\ I_{R2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -V_{cc} \\ V_{cc} - V_{beon} \\ V_{cc} - V_{beon} \end{bmatrix} \tag{3}$$

This then allows to for the calculation of g_m, r_π and r_o using the equations below.

$$g_m = I_c / V_T \tag{4}$$

$$r_\pi = \beta / g_m \tag{5}$$

$$r_o = V_{AFN} / I_c \tag{6}$$

Where each parameter is calculated for each transistor, according to the respective β and I_c. This also allows for the calculation of the output and input impedances for each stage,

$$Z_{I1} = \frac{1}{\frac{1}{R_B} + \frac{r_{o1}+R_c+R_e}{(r_{o1}+R_c+R_e)(R_{\pi 1}+R_e)+g_{m1}R_e r_{o1} r_{\pi 1} - R_e^2}} \tag{7}$$

$$Z_{O1} = \frac{1}{\frac{1}{r_{o1}} + \frac{1}{R_c}} \tag{8}$$

$$Z_{I2} = \frac{g_{m2}+g_{\pi 2}+g_{o2}+g_{e2}}{g_{\pi 2}}(g_{\pi 2}+g_{o2}+g_{e2}) \tag{9}$$

$$Z_{O2} = \frac{1}{g_{m2}+g_{\pi 2}+g_{o2}+g_{e2}} \tag{10}$$

Through Octave, we get Tab. 6.

$Z_{I1}(\Omega)$	$Z_{O1}(\Omega)$
6171.629952	2001.150604
$Z_{I2}(\Omega)$	$Z_{O2}(\Omega)$
23019.363709	0.727991

Table 6: Input and output impedances for the gain and output stages.

We can also calculate immediately the total impedance through (11) and the value is presented in Tab. 7.

$$Z_O = \frac{1}{g_{o2} + \frac{g_{m2}}{g_{\pi 2}} g_B + g_{e2} + g_B} \tag{11}$$

$Z_O(\Omega)$	9.152525

Table 7: Total output of the stages.

3.2 Incremental analysis

As for the incremental analysis, the DC voltage source V_{cc} is shut down and so the nodes 0 (ground) and 6 are merged together and the transistors are approximated by the model that includes 2 capacitors, 2 resistors and a dependent voltage source (model needed in order to capture the higher cutoff frequency in the theoretical analysis). The circuit analysed in this part is presented bellow.

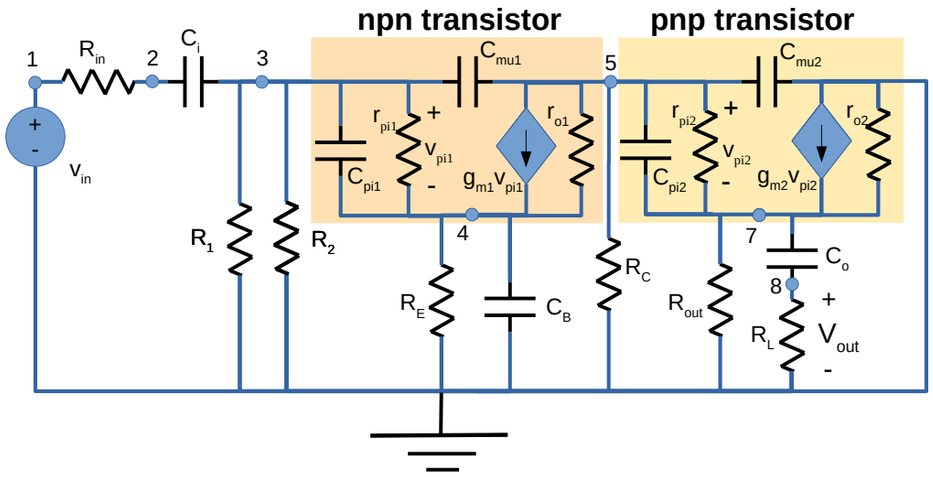


Figure 4: *Circuit in the incremental analysis. There is no node 6 because it was merged with ground.*

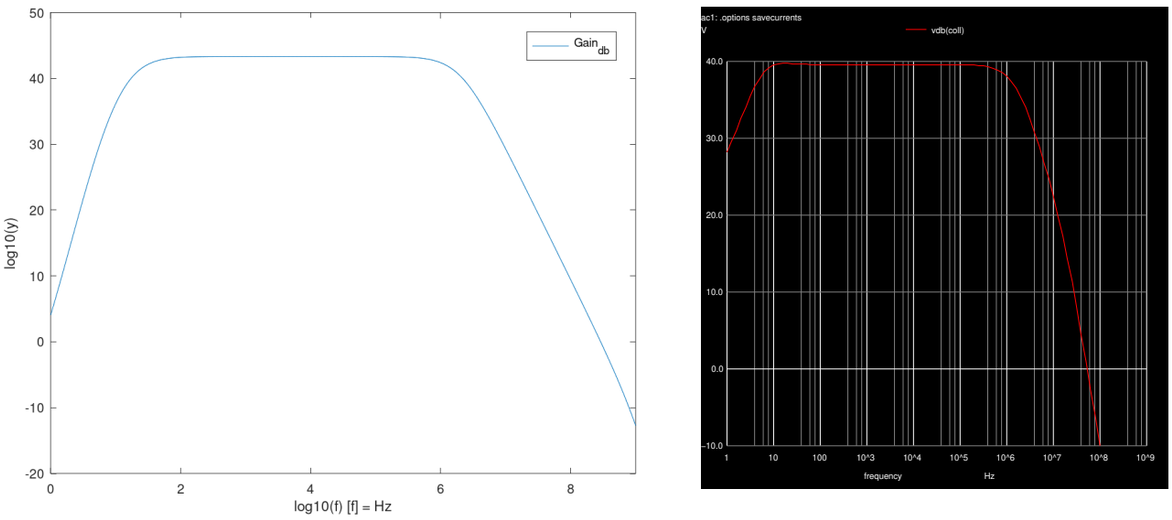
Then the nodal analysis method is applied in order to obtain in the end the output of each stage, which is V_5 and V_{out}. In order to simplify this method, R_{in} and C_i are merged into Z_{in}, disappearing node 2. Same process is applied in R_E and C_B that are in parallel, creating Z_{DE}. It is also defined $V_0 = 0$, because it's ground and $V_1 - V_0 = V_{in}$, which leaves only nodes 3, 4, 5, 7 and 8 for analysis.

$$\begin{cases} \frac{V_3-V_{in}}{Z_{in}} + \frac{V_3-V_0}{R2} + \frac{V_3-V_0}{R1} + \frac{V_3-V_4}{R_{\pi 1}} + (V_3-V_4)i\omega C_{\pi 1} + (V_3-V_5)i\omega C_{\mu 1} = 0 \quad \text{(node 3)} \\ \frac{V_4-V_3}{R_{\pi 1}} + \frac{V_4-V_0}{Z_{DE}} + \frac{V_4-V_5}{r_{o1}} - g_{m1}(V_3-V_4) = 0 \quad \text{(node 4)} \\ g_{m2}(V_3-V4) + \frac{V_5-V_4}{r_{o1}} + (V_5-V_3)i\omega C_{\mu 1} + \frac{V_5-V_0}{r_C} + (V_5-V_0)i\omega C_{\mu 2} + (V_5-V_7)i\omega C_{\pi 2} + \frac{V_5-V_7}{r_{\pi 2}} = 0 \quad \text{(node 5)} \\ (V_7-V_5)i\omega C_{\pi 2} + \frac{V_7-V_5}{r_{\pi 2}} + \frac{V_7-V_0}{r_{out}} + (V_7-V_8)i\omega C_o - g_{m2}(V_5-V_7) + \frac{V_7-V_0}{r_{o2}} = 0 \quad \text{(node 7)} \\ (V_8-V_7)i\omega C_o + \frac{V_8-V_0}{r_L} = 0 \quad \text{(node 8)} \end{cases} \tag{12}$$

Which is equivalent to the matrix form that is to be solved in Octave.

$$\begin{bmatrix} G_{in}+G_2+G_1+G_{\pi 1}+i\omega C_{\mu 1} & -G_{\pi 1} & -i\omega C_{\mu 1} & 0 & 0 \\ -G_{\pi 1}-g_{m1} & G_{\pi 1}+G_{DE}+G_{o1}+g_{m1} & -G_{o1} & 0 & 0 \\ g_{m1}-i\omega C_{\mu 1} & g_{m1}-G_{o1} & G_{o1}+G_C+G_{\pi 2}+i\omega C_{\mu 1}+i\omega C_{\mu 2} & -G_{\pi 2}-i\omega C_{\mu 2} & 0 \\ 0 & 0 & -G_{\pi 2}-g_{m2} & G_{\pi 2}+G_{o2}+G_{out}+g_{m2}+i\omega C_o & -i\omega C_o \\ 0 & 0 & 0 & -i\omega C_o & i\omega C_o+G_L \end{bmatrix} \begin{bmatrix} V_3 \\ V_4 \\ V_5 \\ V_7 \\ V_8 \end{bmatrix} = \begin{bmatrix} V_{in}G_{in} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{13}$$

4 Side by side comparison between both analysis results

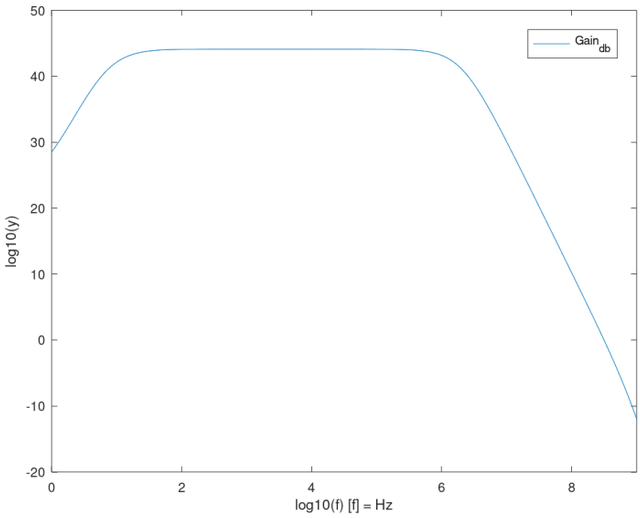


(a) Theoretical analysis

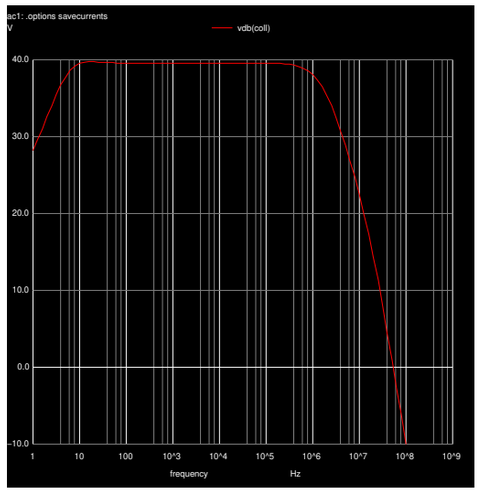
(b) Simulation analysis

Figure 5: Comparison between the obtained plots for the gain stage output dB voltage on *Ngspice* and *Octave*

Once the linear approximation for the transistors were the version with the capacitors the shape of the curves are similar but there are still differences, specifically the theoretical analysis predicts an gain voltage in dB of above 40 as the simulation predicts slightly bellow 40. The other considerable difference is for the higher frequency that both expect very low gains but the simulation analysis decreases faster.



(a) Theoretical analysis



(b) Simulation analysis

Figure 6: Comparison between the obtained plots for the circuit output dB voltage on *Ngspice* and *Octave*

Between the gain stage and the output stage the signal maintains the shift for above 40 in the theoretical analysis, but the difference for the higher frequencies seems to be attenuated. This is to be expected but

Quantity	**Value**
Gain	146.663979
Gain (dB)	43.326469
Lower cut-off frequency	14.307230 Hz
Higher cut-off frequency	1668100.537200 Hz
Bandwidth	1668086.229970 Hz
Cost	3278.058000 MU
Merit	5216.386618
|Zi|	6171.629952Ω
|Zo|	9.152525Ω

Table 8: Theoretical analysis.

Quantity	**Value**
Gain	73.2378
Gain (dB)	37.2947 dB
Lower cut-off frequency	12.5855 Hz
Upper cut-off frequency	1.57176E+06 Hz
Bandwidth	1.57175E+06 Hz
Cost	3278.06 MU
Merit	2790.17
Zi	1385.89 + (-36.7344)j Ω
|Zi|	1386.38 Ω
Zo	14.0507 + (0.625162)j Ω
|Zo|	14.0646 Ω

Table 9: Simulation analysis

Table 10: Relevant values for our goals.

The differences in the gain and in the input impedance cannot be ignored. These may come from the approximations done in the theoretical analysis when we totally ignore the capacitors contribution. Furthermore, we also use a 8x8 matrix, which might easily introduce numerical errors. Thus, because the rest of the values are around the same magnitude, we feel that it is a good result overall, given the nonlinear aspect of the transistor. One last comment, because our OP, although sufficient for us to be working in the FAR, is close to V_{beon} (it is so in order to increase our merit), which might make the transistor, in the Ngspice model, to start to behave differently than from our analysis through Octave.

5 Conclusion

In this laboratory assignment, as presented above, we were proposed to build and study the behaviour of an audio amplifier circuit. To build it, one considered two different regions: a gain stage

and an output stage with different objectives.

The values of the multiple components on the circuit were adjusted in order to increase the merit score which evaluates the efficiency of the circuit and its cost. To increase the efficiency of the circuit, we tried to maximize the amplifying bandwidth and to minimize the lower cutoff frequency while trying to keep a low total cost for the circuit.

To evaluate how good the built amplifier was, we recurred to the merit score presented in Eq. (1). Overall, one can consider the results obtained in the simulation analysis (section 2) as very satisfactory. The results given by the simulation analysis show a bandwidth of $\sim 10^6$ and a lower cutoff frequency ~ 10.

Comparing the results obtained in the simulation and the theoretical analysis, one can conclude that the general shape and values are similar although some small differences appear. The ones in the gain and in the input and output impedance are the more significant but those may come from the matrix calculations and the approximation models used for the transistors that are the only non linear components in this circuit, divisions by 0 also may appear because the analysis is done in a very wide range of values, from 1 Hz to 10^8 Hz. These deviations make up for a slightly bigger merit in the theoretical analysis but the one that is the closest to reality is the simulation analysis so the final merit for the circuit is 2790.17.

Therefore, and having explained the differences registered between the theoretical and the simulation analysis, it can be stated that the goals for this laboratory assignment were successfully achieved.

References

[1] Ngspice official website, *http://ngspice.sourceforge.net/*