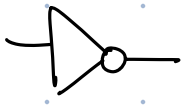
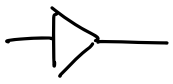
logic gates.

NOT



$Y = \bar{A}$

BUF

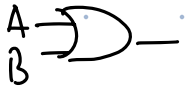


$Y = A$

AND

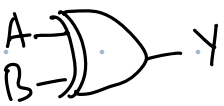
$Y = AB$

OR



$Y = A + B$

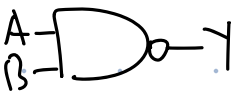
XOR



$Y = A \oplus B$

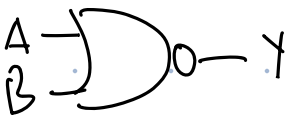
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

NAND



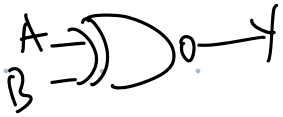
$Y = \overline{AB}$

NOR



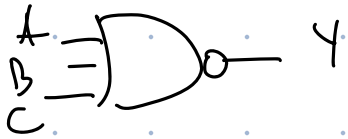
$Y = \overline{A+B}$

XNOR



A	B	Y
0	0	1
1	0	0
0	1	0
1	1	1

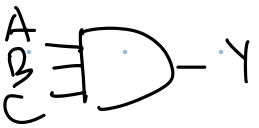
NOR3



$Y = \overline{A+B+C}$

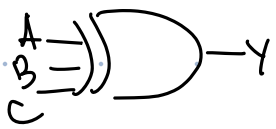
A	B	C	Y
0	0	0	1
⋮	⋮	⋮	0
			⋮
			0

AND3



$Y = ABC$

XOR3

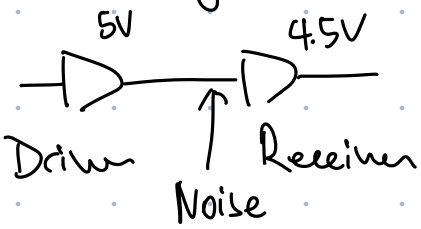


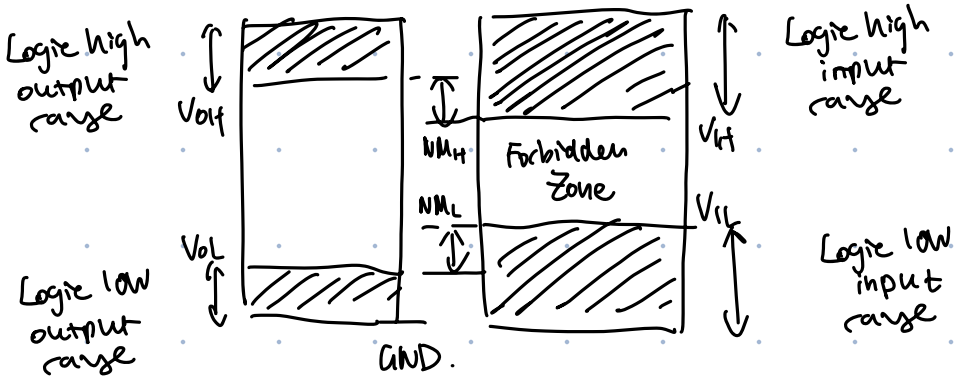
$Y = A \oplus B \oplus C$

(outputs 1 when an odd # of inputs is 1.

Noise

- Anything that degrades the signal.



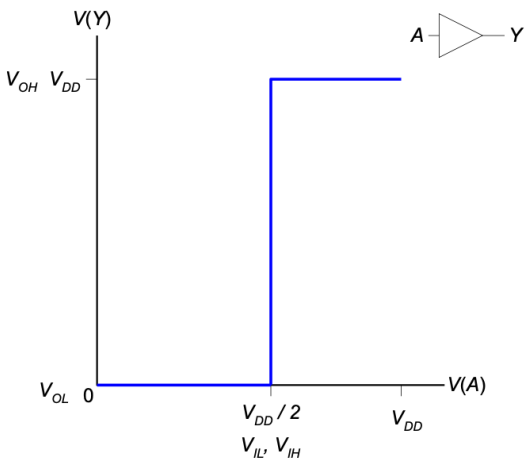


$$NM_H = V_{OH} - V_{IH}$$

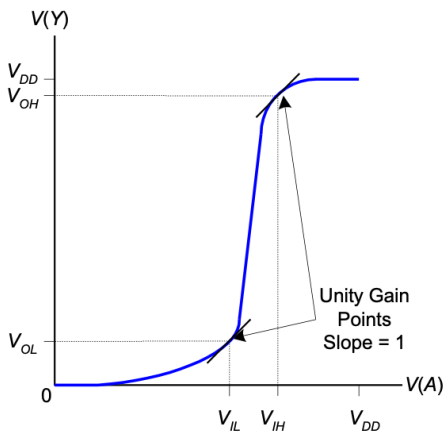
$$NM_L = V_{OL} - V_{IL}$$

DC Transfer Characteristics

Ideal Buffer:



Real Buffer:



$NM_H = NM_L = V_{DD}/2$

$NM_H, NM_L < V_{DD}/2$

Transistors

↳ building blocks for logic gates.

↳ 3 ported voltage-controlled switch.

d & s connected (ON) only when g = 1.

↳ 2 types of transistors: nMOS & pMOS.

type	gate voltage V=0	V=1
nMOS	0	1
pMOS	1	0

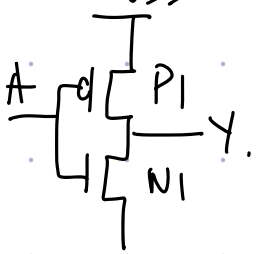
pass good 0's: connect source to GND

pass good 1's: connect source to VDD

Using Transistors to build gates

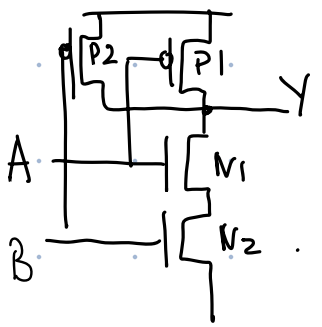
① NOT Gate.

A	Y
0	1
1	0



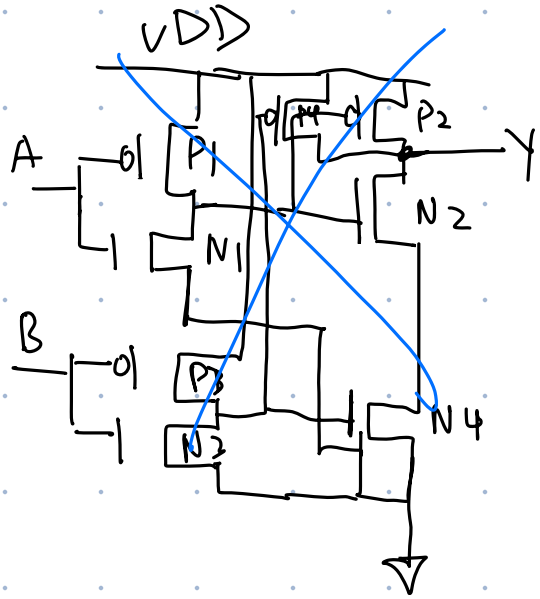
② NAND GATE

A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

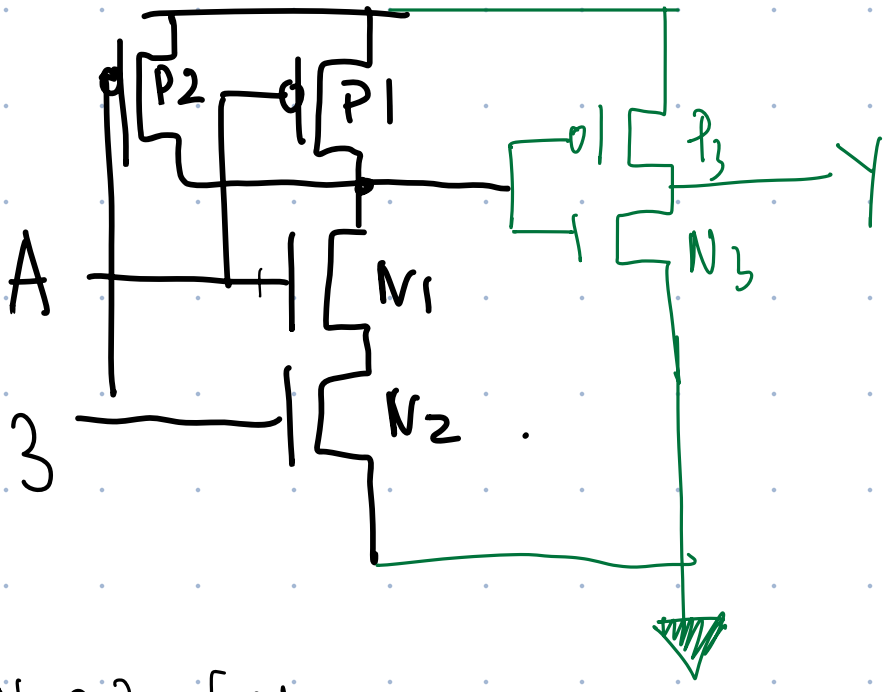


③ AND2 GATE

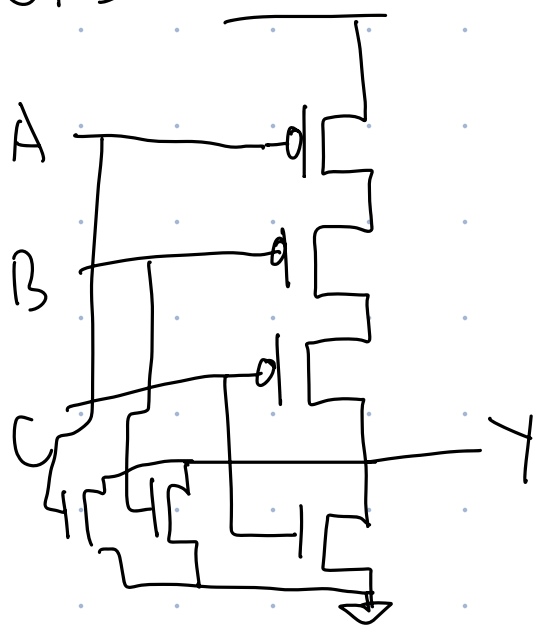
A	B	Y
0	0	0
1	0	0
0	1	0
1	1	0



should be NAND+NOT, not NOT+NAND)

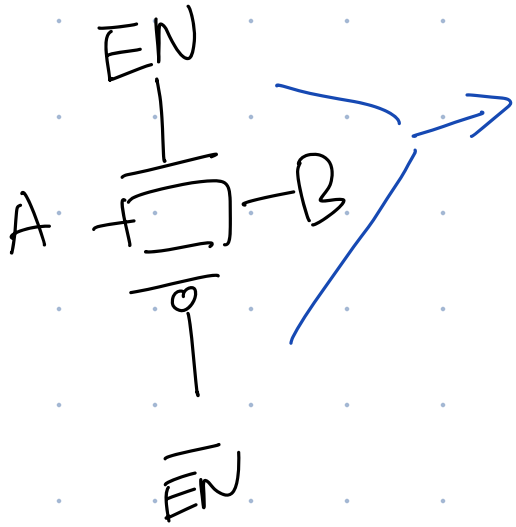


④NOR3 Gate



* It is easier to build inversion gates with CMOS transistors.

Transmission Gates



controlled by complementary signals.

ensures that the nMOS & pMOS are on & off together.