

BASIC LOGIC GATES

Dr. Suneth Pathirana

B.Sc.(UWU-CST)(Hons), M.Sc.(AI)(Moratuwa), MIEEE, Ph.D.(MSU)

Senior Lecturer

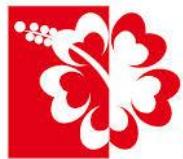
Department of Computer Science & Informatics

Uva Wellassa University of Sri Lanka

suneth@uwu.ac.lk



About the Lecturer – Academic / Research



Doctor of Philosophy in Neurorobotics

Management and Science University of Malaysia

with Research Collaboration of
Taylor's University



GPA = 4.00 / 4.00



Master of Science in Artificial Intelligence

Department of Computational Mathematics

with Research Collaboration of
Dept. of Electronic & Telecommunication Engineering,
University of Moratuwa

GPA = 3.73 / 4.00



Member of [IEEE](#)



Member of [Sri Lankan Association for Artificial Intelligence](#)

About the Lecturer – Professional Experience



Lecturer

Department of Computer Science,
University of Ruhuna



Post-Graduate Research Affiliate

Artificial Intelligence Labs,
Department of Computational Mathematics
Dept. of Electronic & Telecommunication Engineering,
University of Moratuwa



Instructor (Computing)

University of Colombo



Project Manager – Team Lead - Software Engineer

Head, Mobile Application Development Division
IDOLA (PVT) LTD. (www.idola.lk)



Intern Research Scientist (Robotics)

Arthur C. Clerk Institute (www.accimt.ac.lk)

Academic Collaborations



Member – Board of Study | Visiting Lecturer (PG)

CODL / Faculty of Applied Sciences / Computing
Sabaragamuwa University, Belihuloya



Visiting Lecturer

Faculty of Technology

South Eastern University, Oluvil



VIDYA JYOTHI PhD Supervisor | Visiting Professor

Department of Electrical Engineering

Faculty of Engineering

Vidya Jyothi Institute of Technology (VJIT)

Hyderabad, India (<https://vjit.ac.in>)

Department of Computer Science & Informatics, Uva Wellassa University

Research Collaborations



REVA
UNIVERSITY



About the Lecturer – Professional Experience (Up to Late 2020)

- ④ Total Professional Experience – **15 Yrs+**
- ④ Which Include:
 - Industry – 1 Yrs+
 - Full-time Research – 3 Yrs+
 - **Teaching in State Universities – 14 Yrs+**

Contribution to International Scientific Research

Vision based inference for mobile robots in order to avoid obstacles, is one of the most attracted areas for both domains of Computer Vision and Robotics. Computer Vision, more specifically the vision for intelligent machines enables mobile robots to perceive the external world with 'wisdom'. Therefore Vision based obstacle avoidance has become one of the major research areas of Robotics. Estimating the motion path and predicting the motion behavior of a dynamic object with only single camera (monocular vision) is a real challenge. We realized this can be done by analyzing a sequence of image frames extracted from a live video stream. But, these analytic techniques must be extremely fast in real time processing, since the decision drawn within reasonably short response time is the only 'god' to safeguard the robot & ensure the safety of others in environment! Therefore, we postulate a fuzzy-mathematical model: an Artificial Intelligence approach to achieve the ultimate objective, which has a significant impact in terms of simplicity (reduced complexity) together with efficiency (minimized computational overhead: resource consumption), rather than conventional mathematical modeling.

A (Monocular) Vision based Mobile Robot



Suneth Pathirana



Suneth Pathirana is a researcher in Artificial Intelligence & Robotics. Obtained B.Sc.(C.Sc.)(Sp.)(Hons) from Uva Wellassa University of Sri Lanka in 2010. Then joined University of Colombo, later University of Ruhuna as a Lecturer. Completed M.Sc. in AI at University of Moratuwa in 2013. Currently reading for Ph.D. at MSU, Malaysia.



978-3-659-67610-9

Pathirana

A Fuzzy-Mathematical Model to Motion Detection with Monocular Vision

Vision Based Mobile Robots

LAP LAMBERT
Academic Publishing

Related Disciplines

- ④ The knowledge gained through this course will be continued with...
 - This will be a prerequisite for...

Course Code/Title	Level	Compulsory / Elective
SCT 384-2 Embedded Systems	300	C
CST 477-2 Robotics	400	O
CST 437-2 Internet of Things	400	O

Objective + Learning Outcomes

① Objective:

- Provide a necessary and essential knowledge on digital logic and microcomputer organization and its function.

② Learning Outcomes:

- On successful completion of this course, the student will be able to...
 - ❖ Have a sound knowledge and understanding on digital logic components.
 - ❖ Have a basic knowledge on microcomputer architecture

Recommended Text

- ④ Bartee T. C., (1991), Computer Architecture & Logic Design, (McGraw Hill)
- ④ Hennessy J.L., Patterson D.A., (2006), Computer Architecture: A Quantitative Approach, 4th Edition, (Morgan Kaufmann)

Evaluation Methodology

40%

Continuous Assessments

- **2 Take-Home Assignments**
(5 Marks Each)
- **2 Uninformed Quiz**
(5 Marks Each)
- **Mid Semester Exam (20%)**

60%

End Semester Exam

Analog Vs. Digital



23:59:59



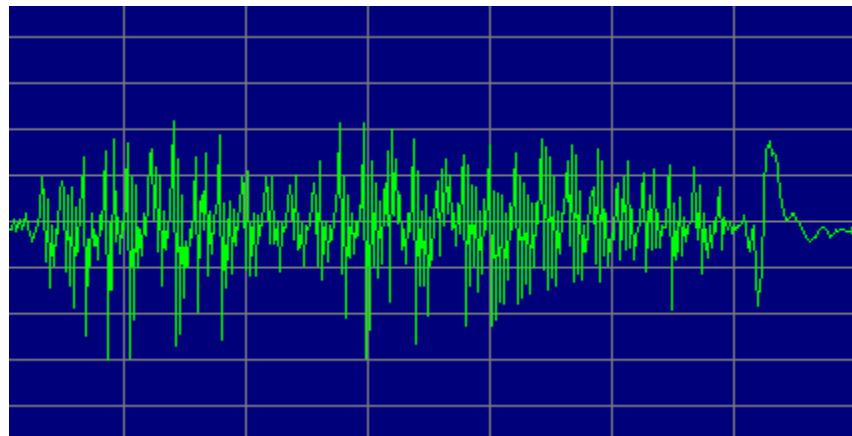
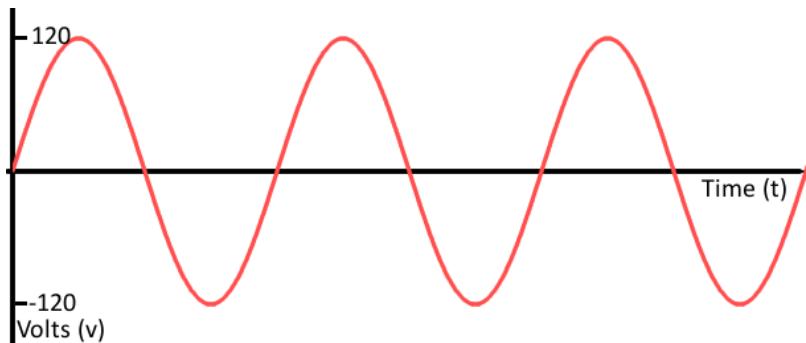
Analog Vs. Digital

- ④ Almost all the real world systems exhibit analog features
- ④ The common theme beyond the analog concept is **infinite** combinations (possibilities)
 - Ex: A user can set the Volume of this analog TV to 34.5678976544321 % (theoretically)
 - And the frequency of the Tuner can be set to any value range within the range 300 MHz and 3 GHz (for UHF)



Analog Signals

- ④ A time-versus-voltage graph of an analog signal should be **smooth** and **continuous**



Analog Electronics

- ④ Most of the fundamental electronic components – resistors, capacitors, inductors, diodes, transistors, and operational amplifiers – are all inherently analog
- ④ Circuits built with a combination of solely these components are usually analog
- ④ Analog circuits are usually much more **susceptible to noise** (small, undesired variations in voltage)
 - Small changes in the voltage level of an analog signal may produce significant errors when being processed.

Analog Storage Devices

@ Magnetic Tapes

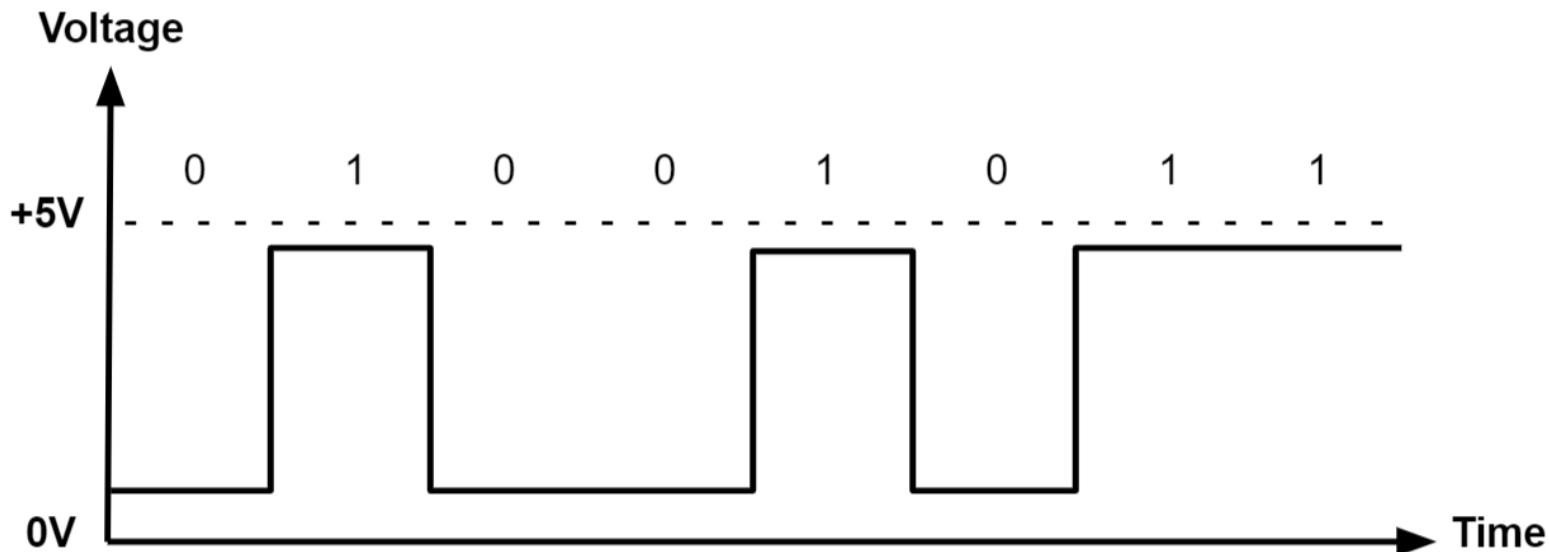


@ Photo Film



Analog Vs. Digital

- ④ Digital signals and objects are expected to behave in a manner of **discrete** or **finite**, meaning there is a limited set of values they can be
- ④ That could mean just two total possible values



Migrating (Transforming) From Analog to Digital



The Revolution Begins: Invention of the Transistor

- ④ The thermionic triode, a vacuum tube invented in 1907, enabled amplified radio technology and long-distance telephony
- ④ The triode, however, was a fragile device that consumed a substantial amount of power
- ④ In 1909, physicist William Eccles discovered the crystal diode oscillator
- ④ Austro-Hungarian physicist Julius Edgar Lilienfeld filed a patent for a **field-effect transistor (FET)** in Canada in 1925

Vacuum Tubes



ComputerHope.com



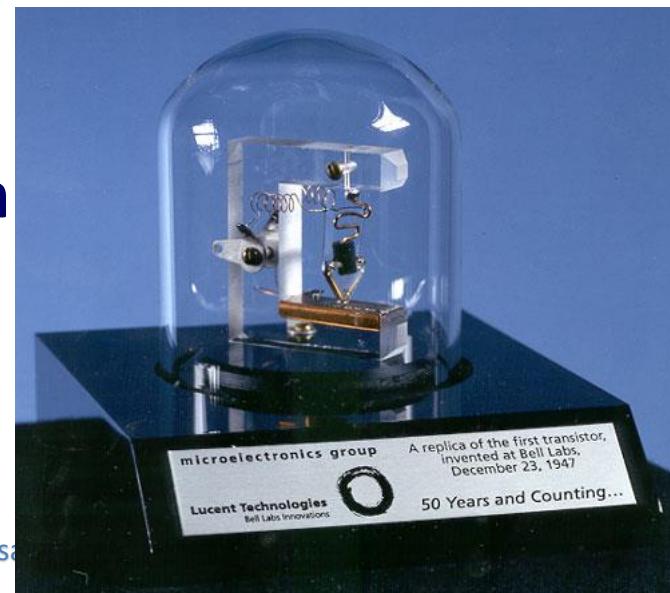
The Revolution: Invention of the Bipolar Transistor

- ④ In late 1947, **John Bardeen, Walter Brattain** and the Solid State Physics Group leader **William Shockley** invented the new knowledge of semiconductors at AT&T's Bell Labs in Murray Hill, New Jersey

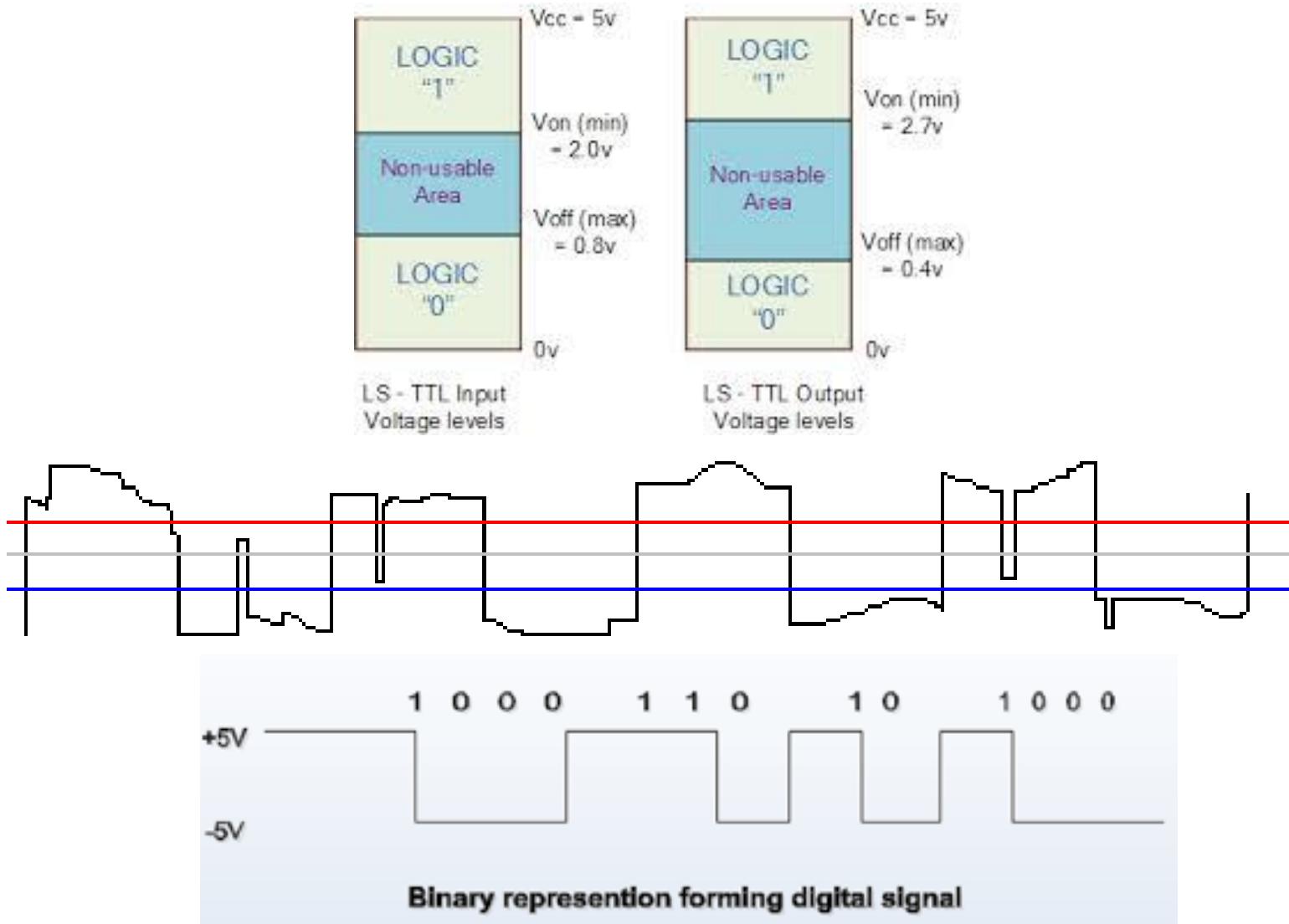
➤ The term transistor was coined by John R. Pierce as a contraction of the term *transresistance*



- ④ Shockley, Bardeen, and Brattain were jointly awarded the **1956 Nobel Prize in Physics** "for their researches on semiconductors and their discovery of the transistor effect"

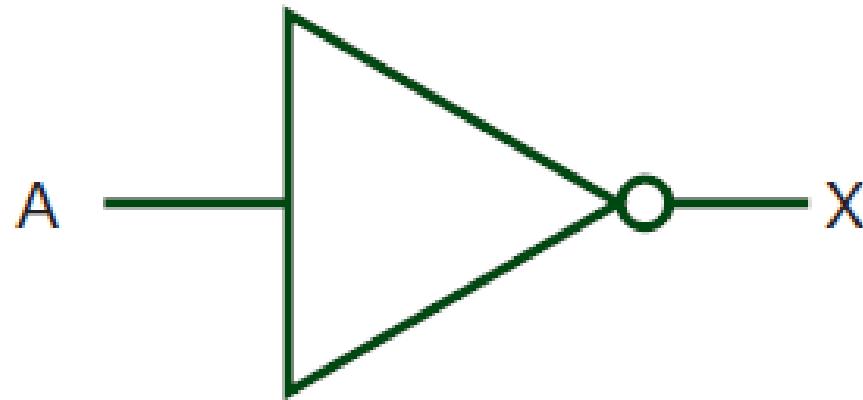


Cut-Off Voltage levels of Digital Signals



Basic Logic Gates : NOT Gate

④ NOT Gate

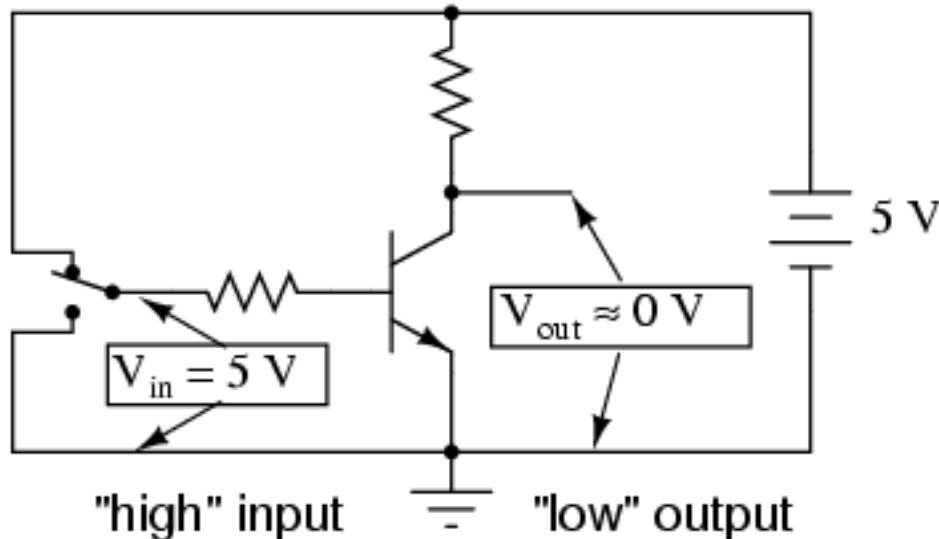


INPUT A	OUTPUT X
0	1
1	0

How digital logic gates are made?

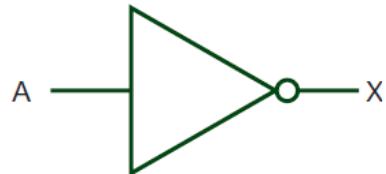
- Obviously, using the main building blocks as Transistors!

Transistor in saturation

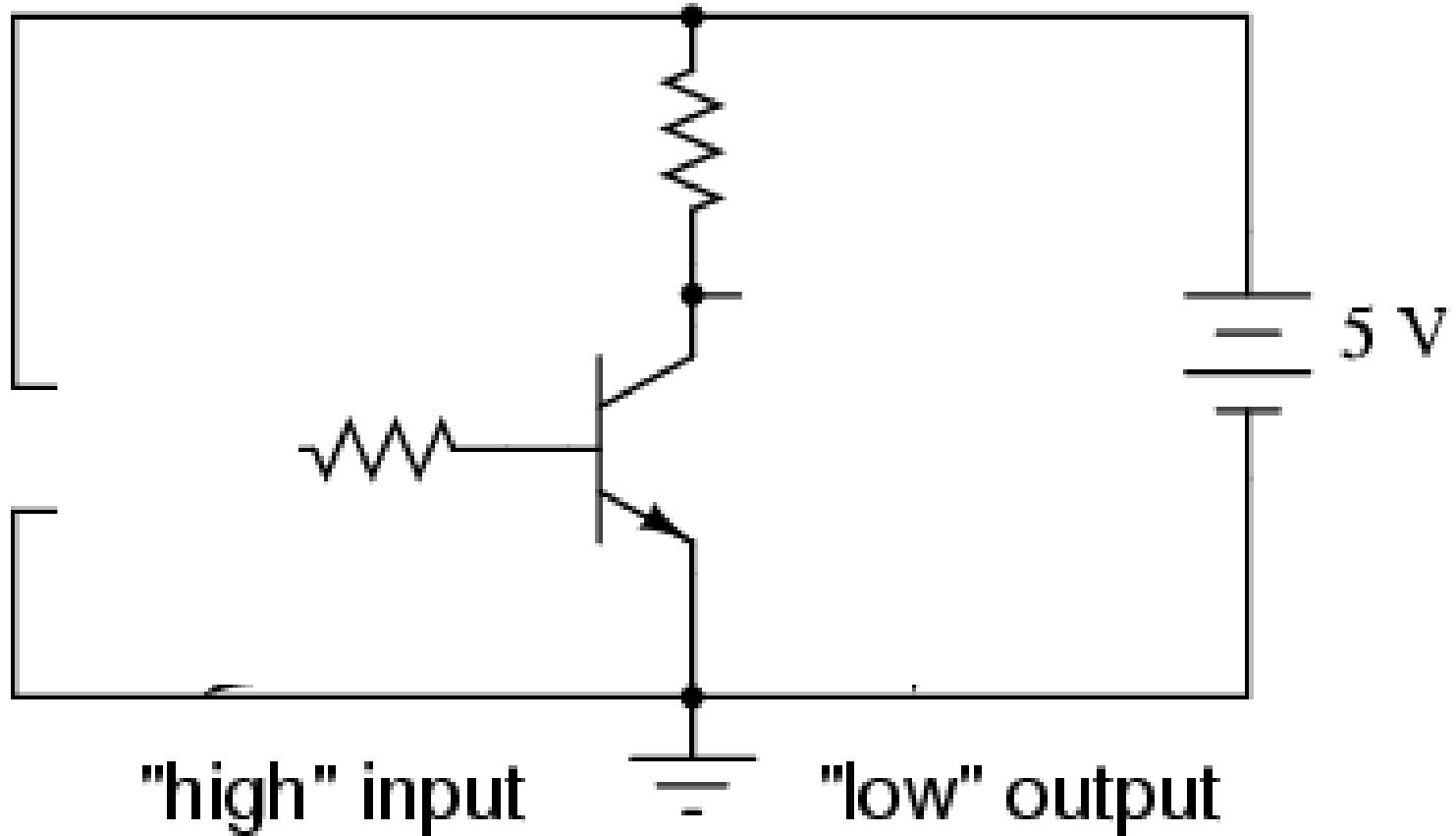


$0\text{ V} = \text{"low" logic level (0)}$

$5\text{ V} = \text{"high" logic level (1)}$

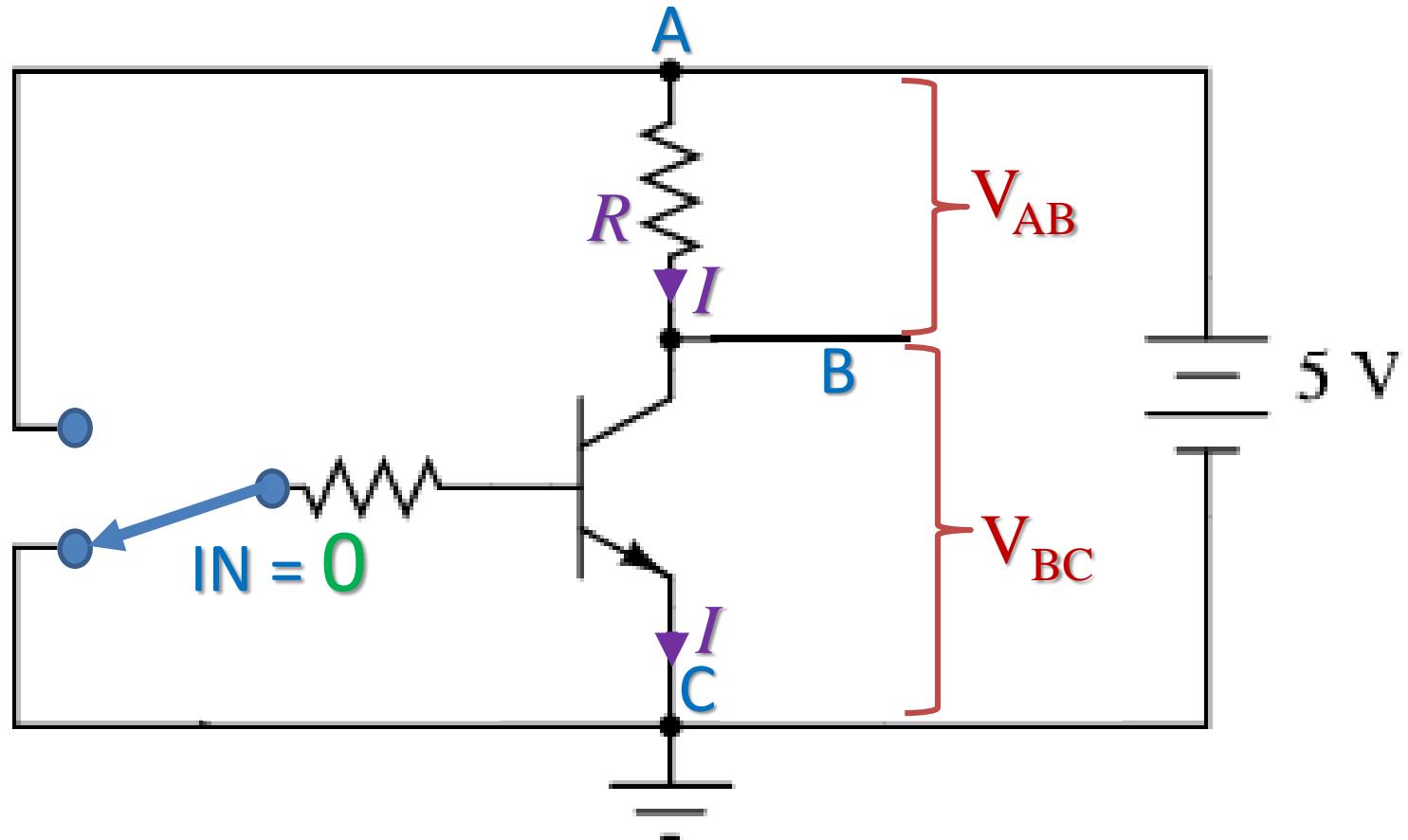
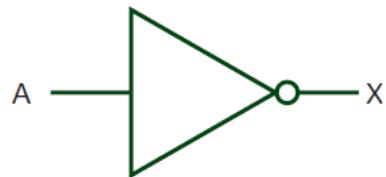


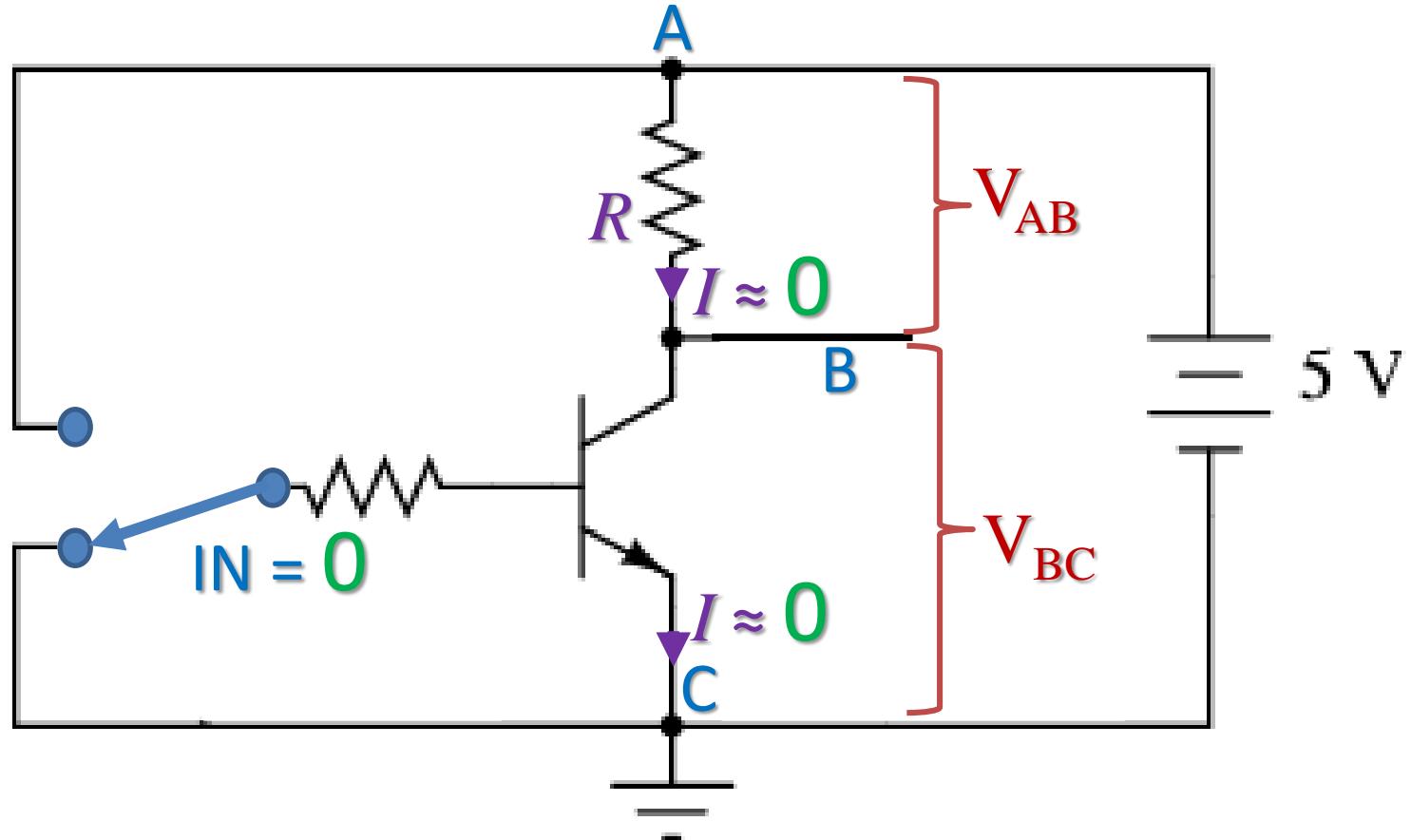
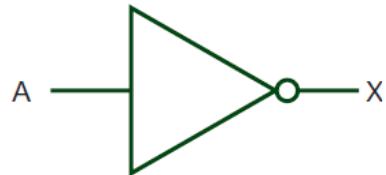
INPUT A	OUTPUT X
0	1
1	0

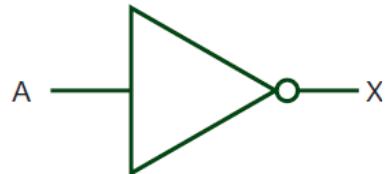


$0 \text{ V} = \text{"low" logic level (0)}$

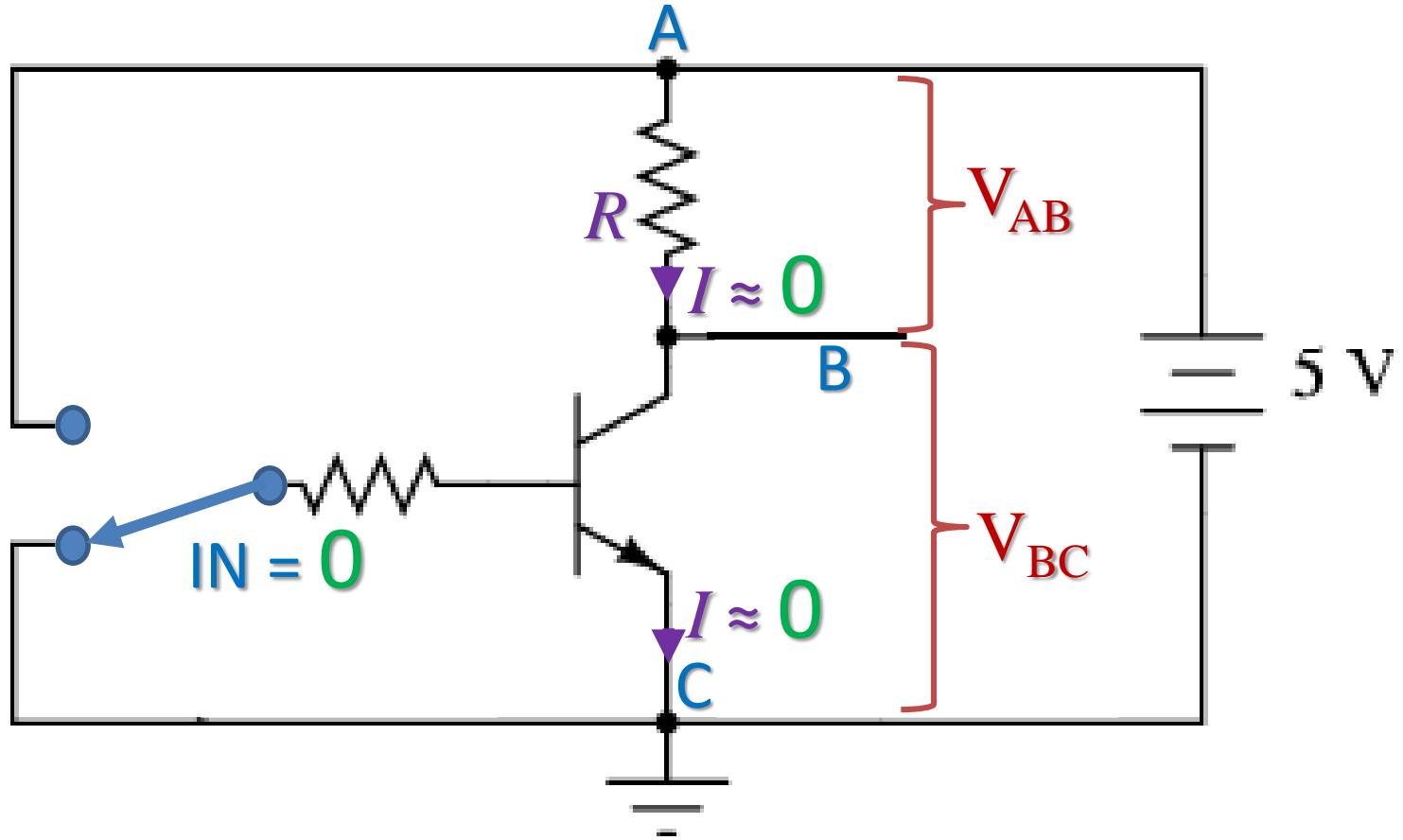
$5 \text{ V} = \text{"high" logic level (1)}$







INPUT A	OUTPUT X
0	1
1	0

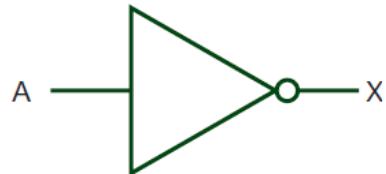


Voltage Drop across R :

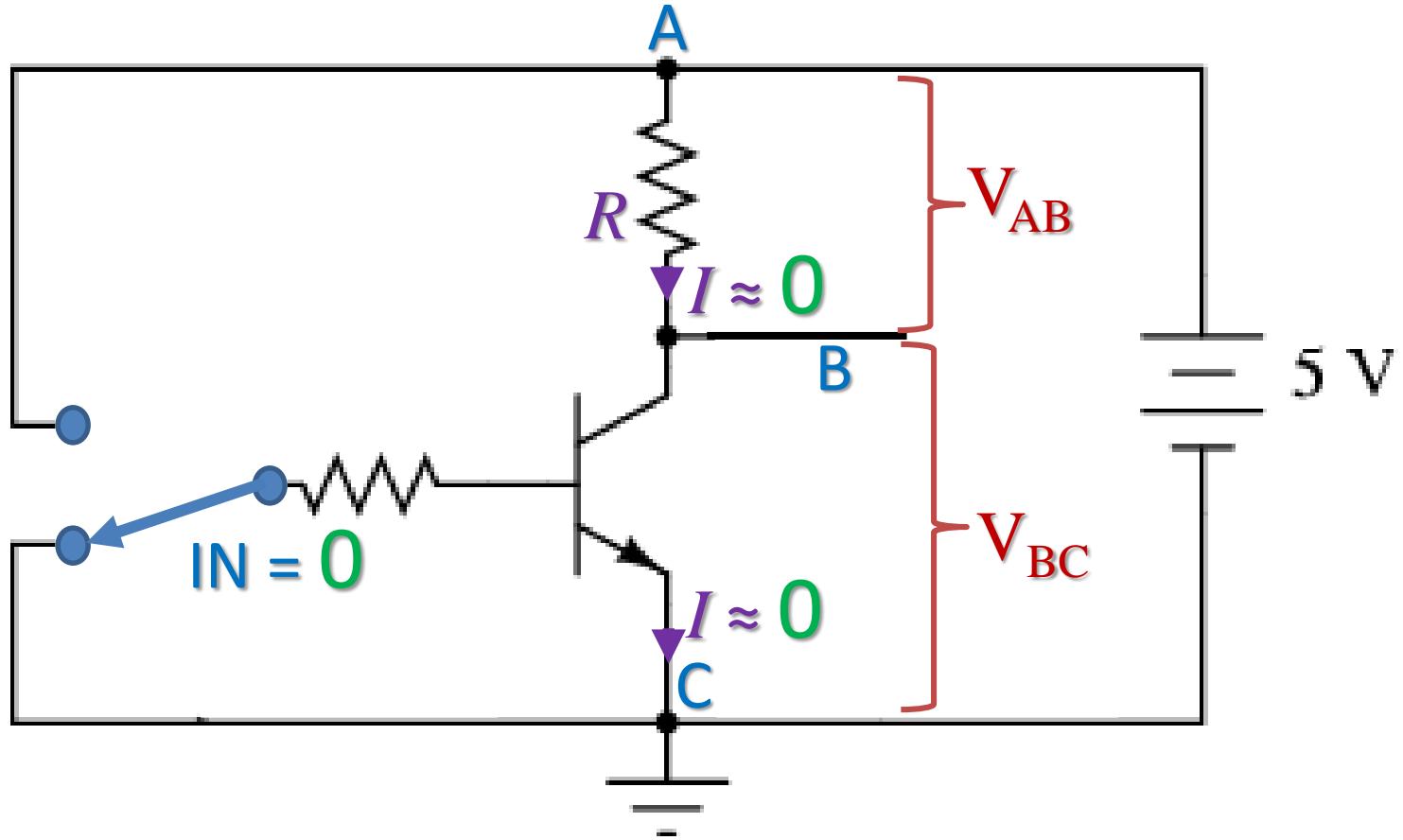
$$V = I * R$$

$$V_{AB} = 0 * R$$

$$V_{AB} \approx 0 \text{ V}$$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

$$V = I * R$$

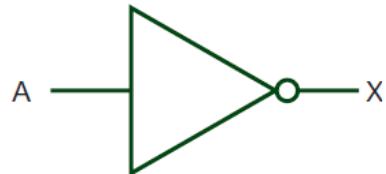
$$V_{AB} = 0 * R$$

$$V_{AB} \approx 0 \text{ V}$$

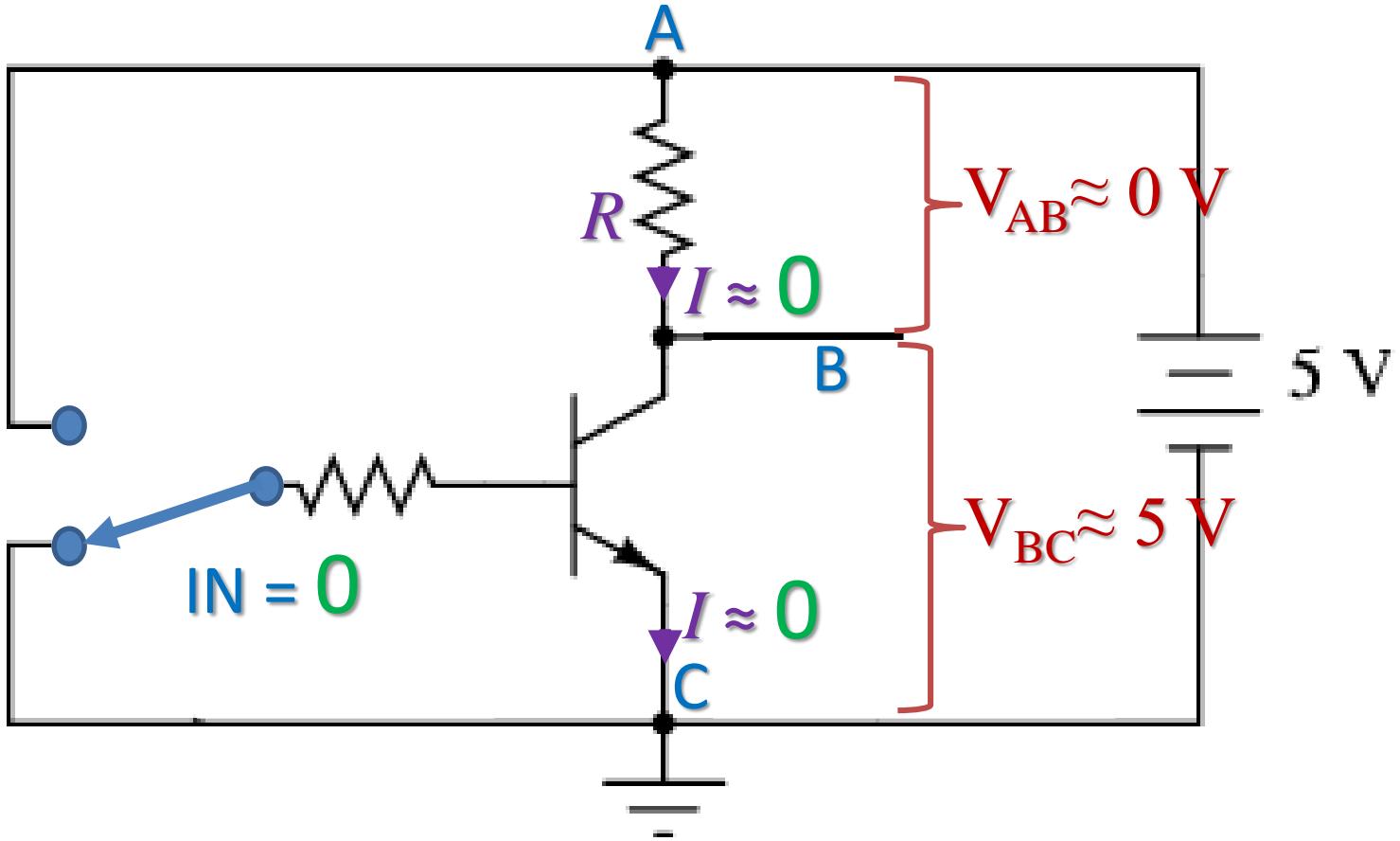
$$V_{AB} + V_{BC} = 5 \text{ V}$$

$$0 + V_{BC} = 5 \text{ V}$$

$$V_{BC} \approx 5 \text{ V}$$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

$$V = I * R$$

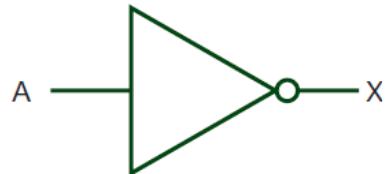
$$V_{AB} = 0 * R$$

$$V_{AB} \approx 0 \text{ V}$$

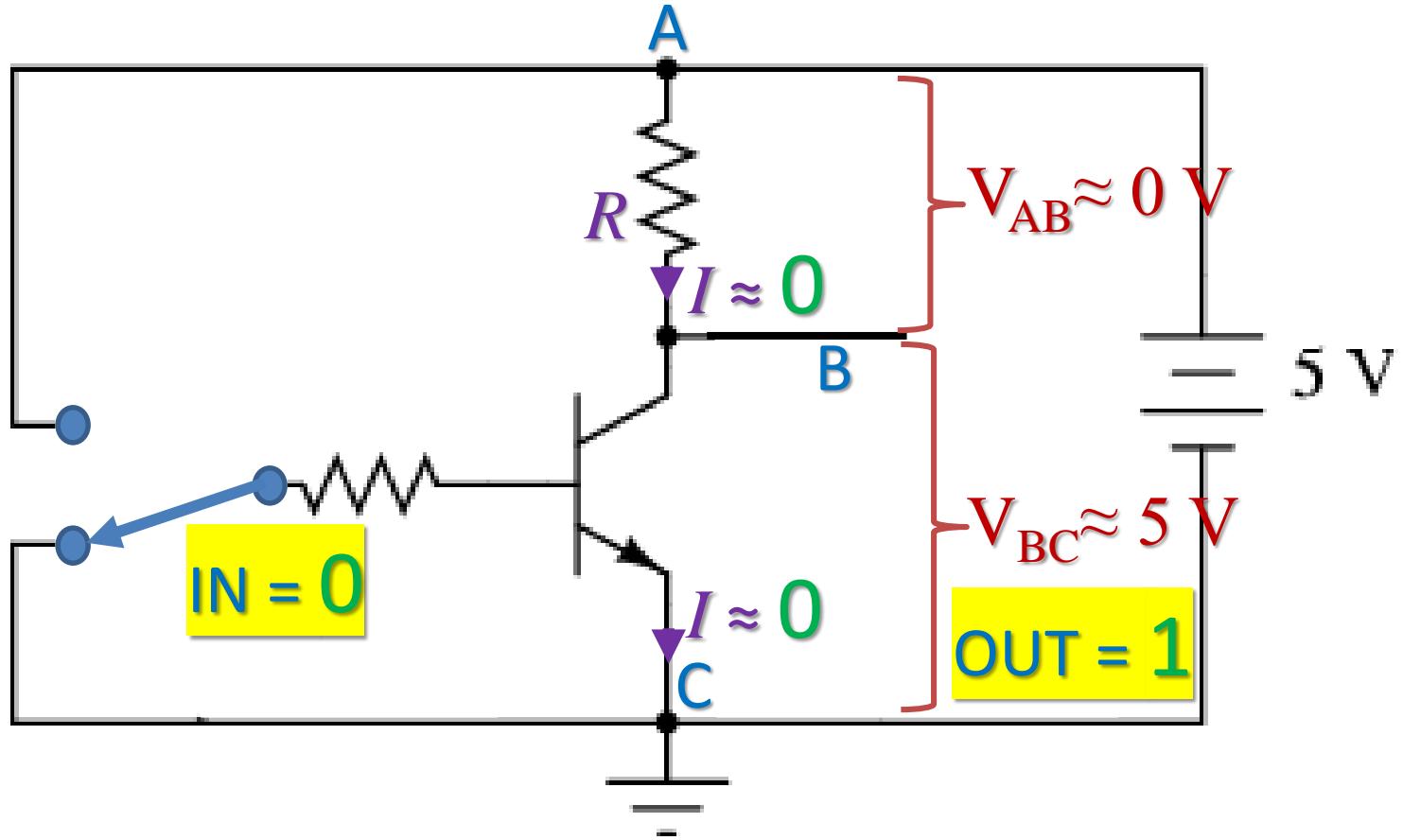
$$V_{AB} + V_{BC} = 5 \text{ V}$$

$$0 + V_{BC} = 5 \text{ V}$$

$$V_{BC} \approx 5 \text{ V}$$



INPUT A	OUTPUT X
0	1
1	0

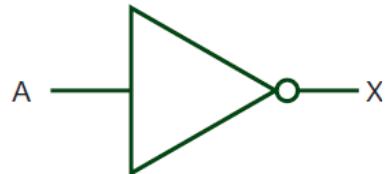


Voltage Drop across R :

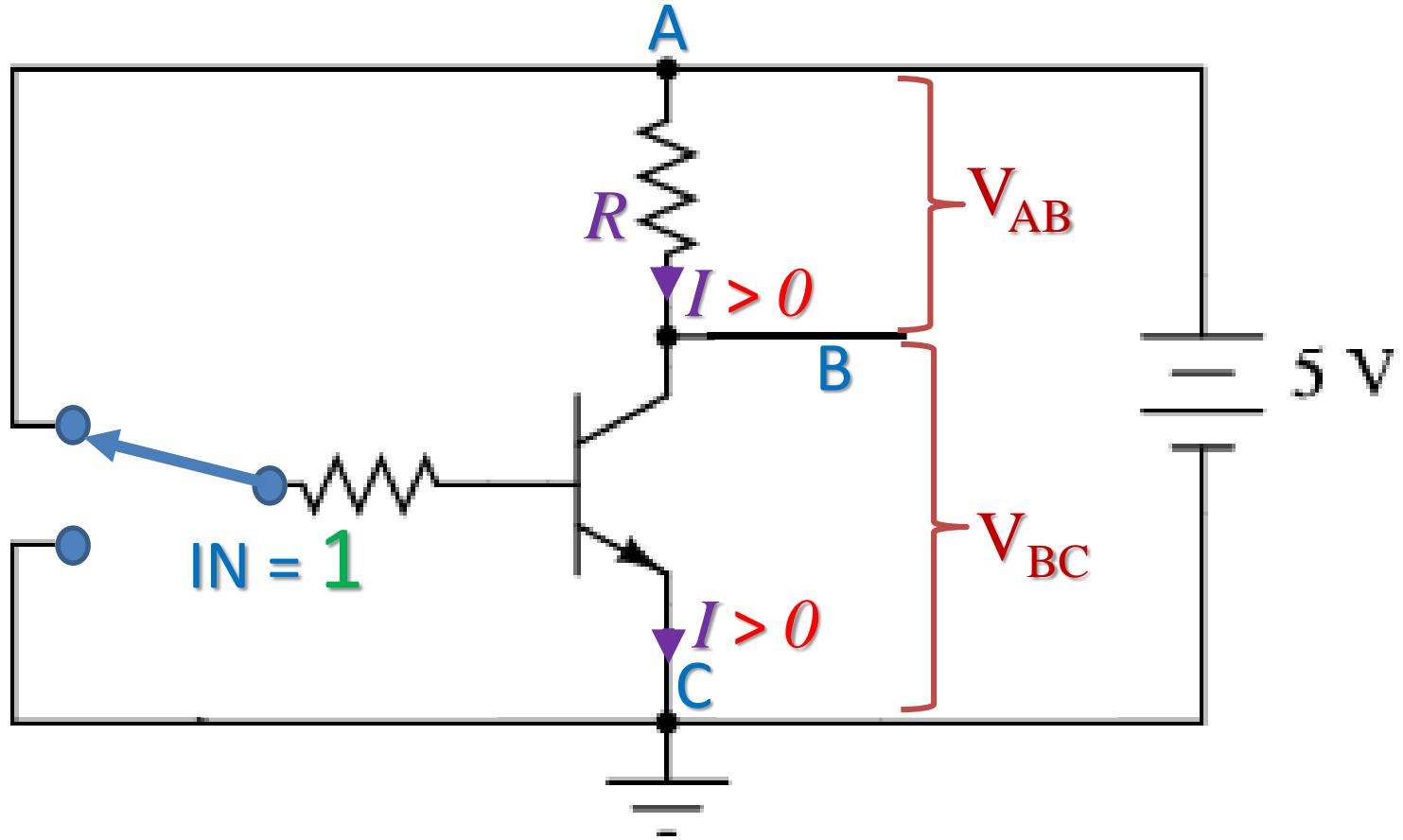
$$V = I * R$$

$$V_{AB} = 0 * R$$

$$V_{AB} \approx 0 \text{ V}$$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

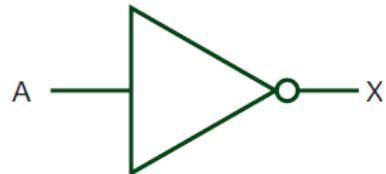
$$V = I * R$$

$$V_{AB} = I * R \text{ where } I > 0$$

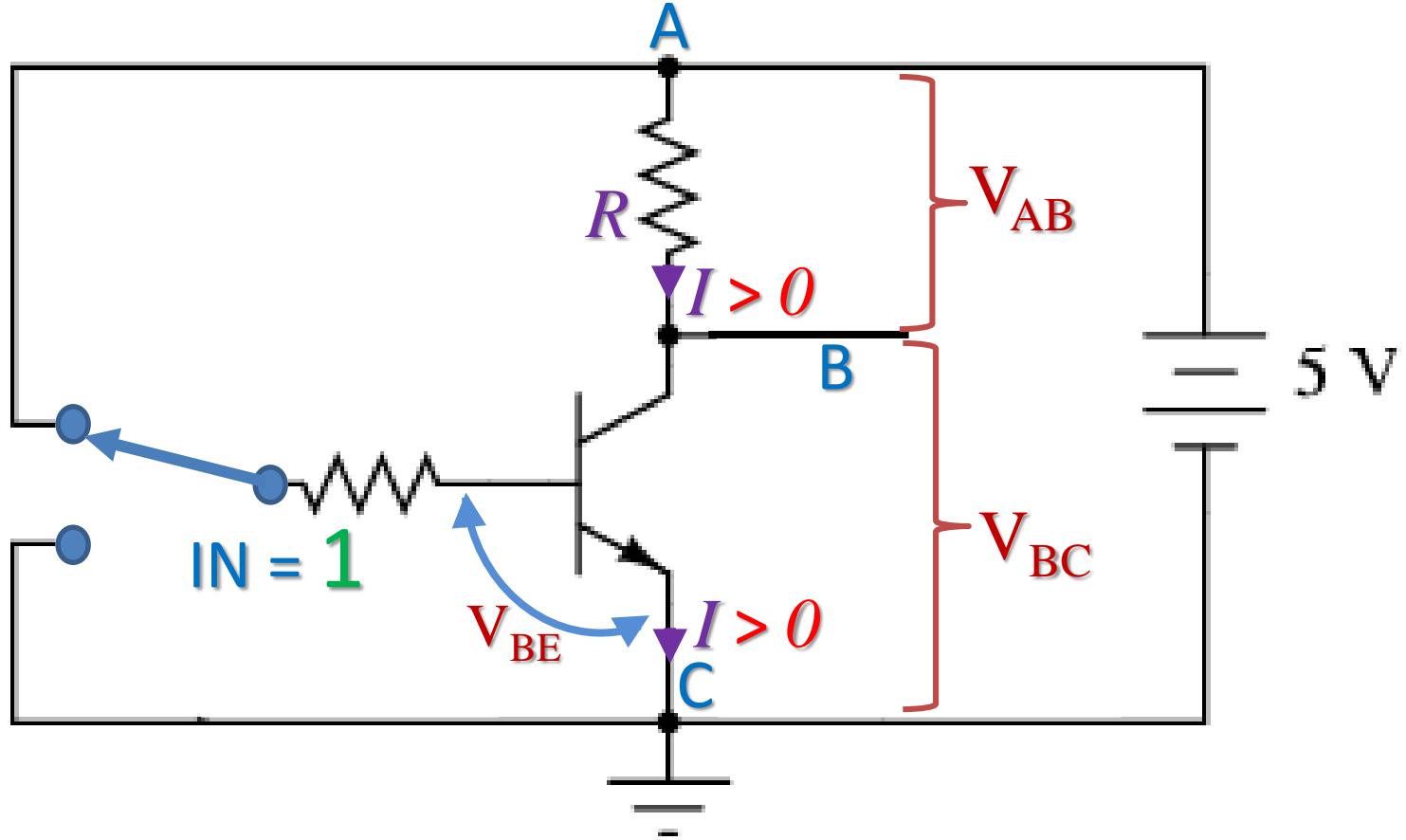
$$V_{AB} > 0$$

Requirement for $I > 0$

V_{BE} (of the transistor) $\gg 0.7 \text{ V}$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

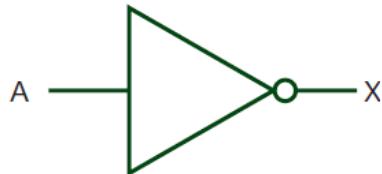
$$V = I \cdot R$$

$$V_{AB} = I \cdot R \text{ where } I > 0$$

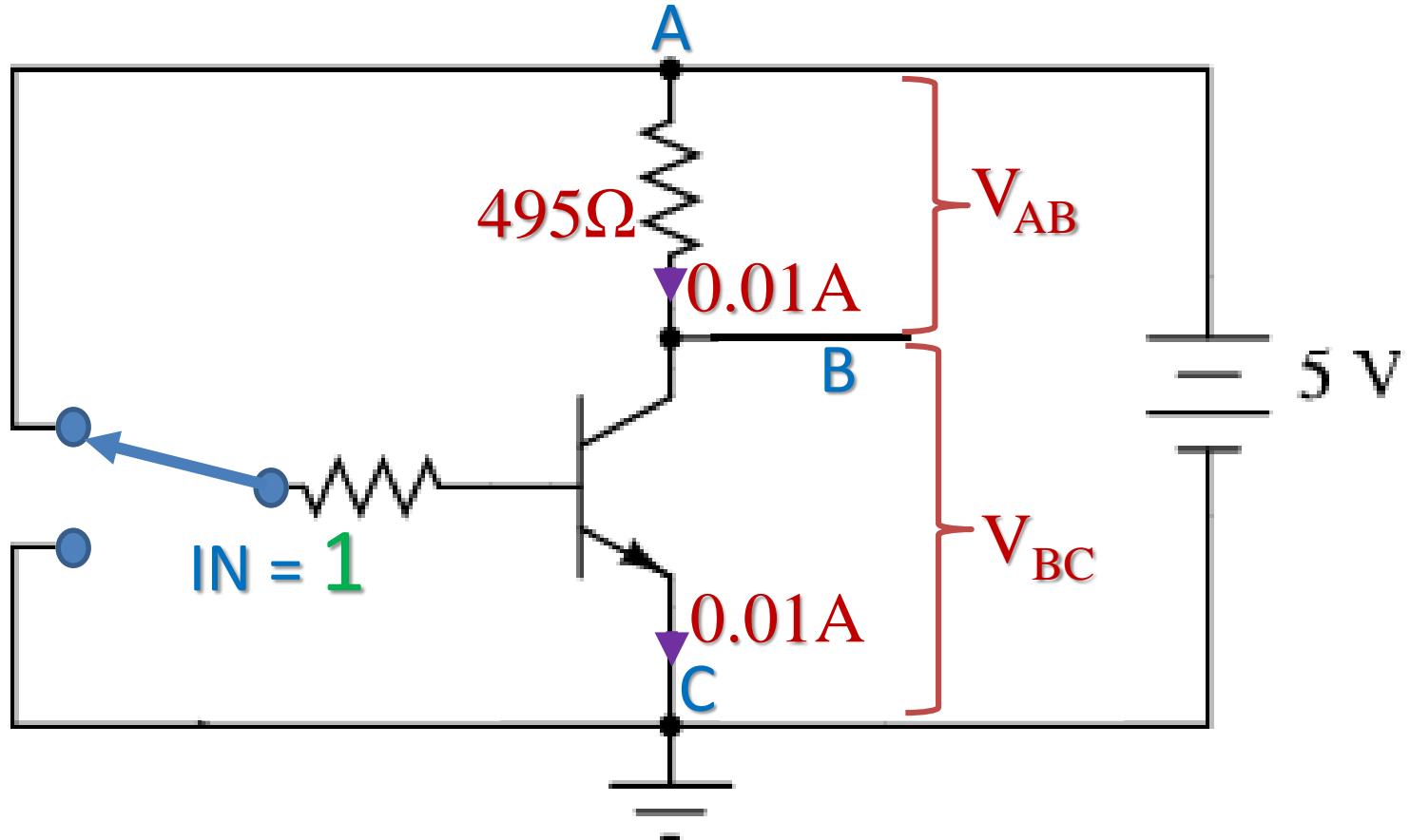
$$V_{AB} > 0$$

Requirement for $I > 0$

V_{BE} (of the transistor) $\gg 0.7 \text{ V}$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

$$V = I \cdot R$$

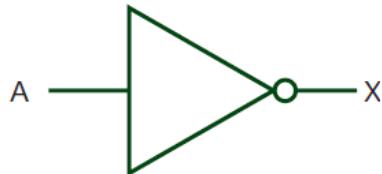
Let's assume $R = 495\Omega$, $I = 0.01A$

$$V_{AB} = 495 \cdot 0.01 = 4.95 V$$

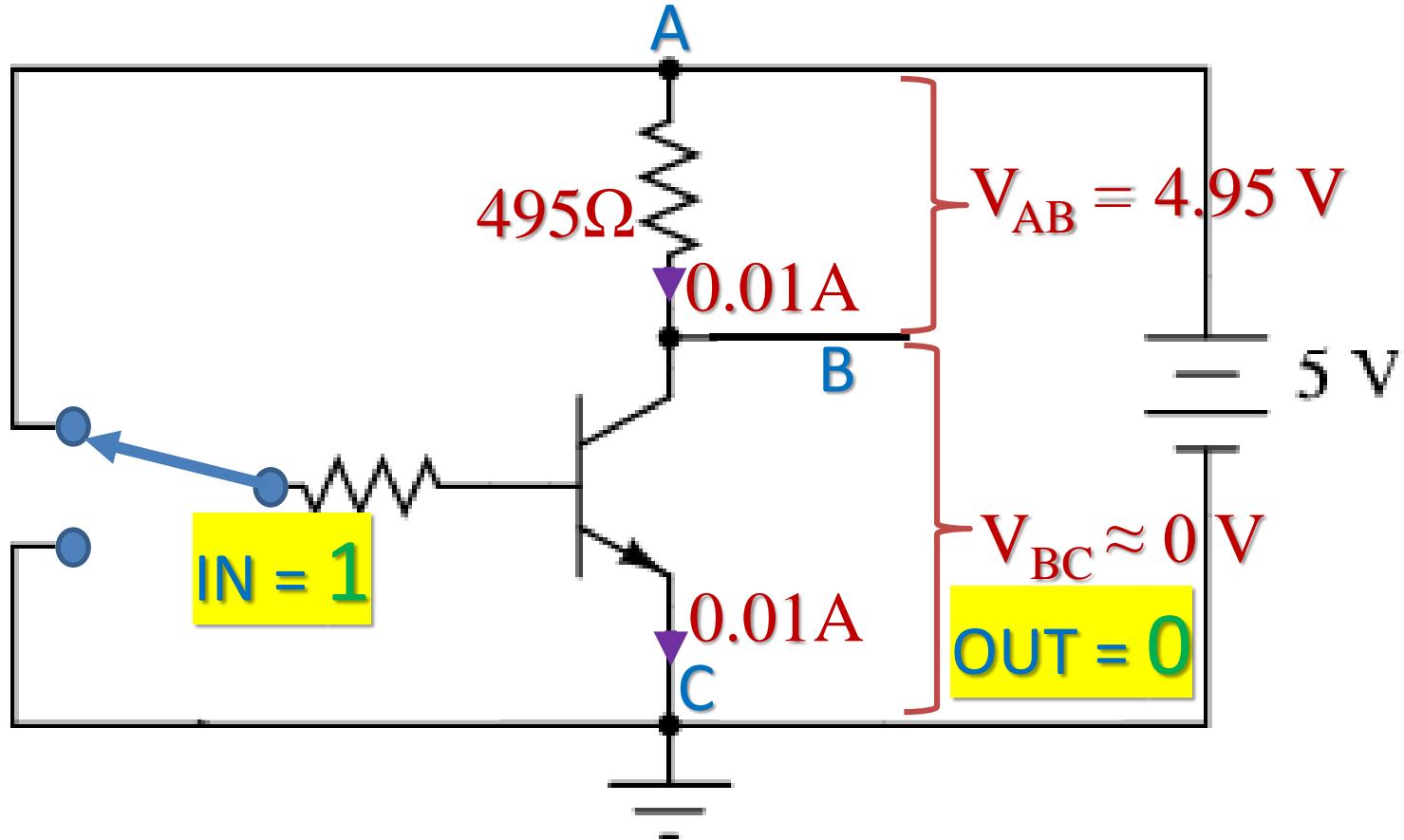
$$V_{AB} + V_{BC} = 5 V$$

$$4.95 V + V_{BC} = 5 V$$

$$V_{BC} = 0.05 V \approx 0 V$$



INPUT A	OUTPUT X
0	1
1	0



Voltage Drop across R :

$$V = I * R$$

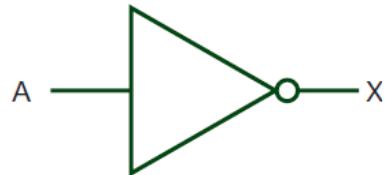
Let's assume $R = 495\Omega$, $I = 0.01\text{A}$

$$V_{AB} = 495 * 0.01 = 4.95 \text{ V}$$

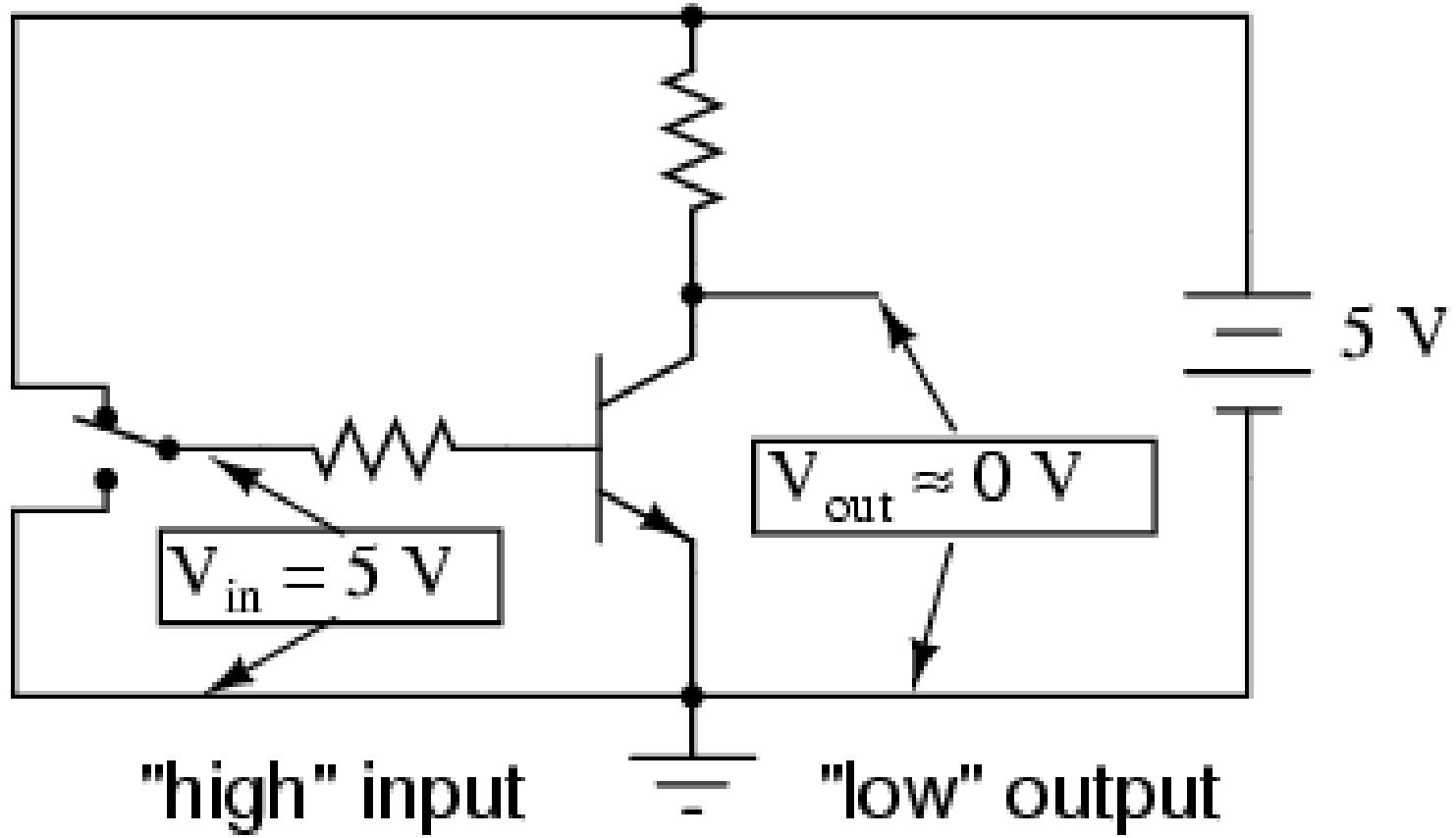
$$V_{AB} + V_{BC} = 5 \text{ V}$$

$$4.95 \text{ V} + V_{BC} = 5 \text{ V}$$

$$V_{BC} = 0.05 \text{ V} \approx 0 \text{ V}$$



INPUT A	OUTPUT X
0	1
1	0



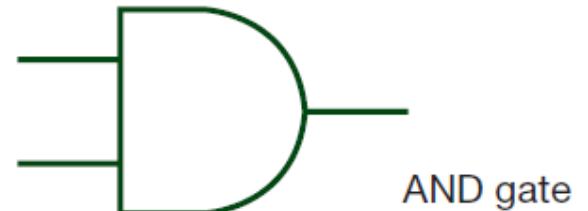
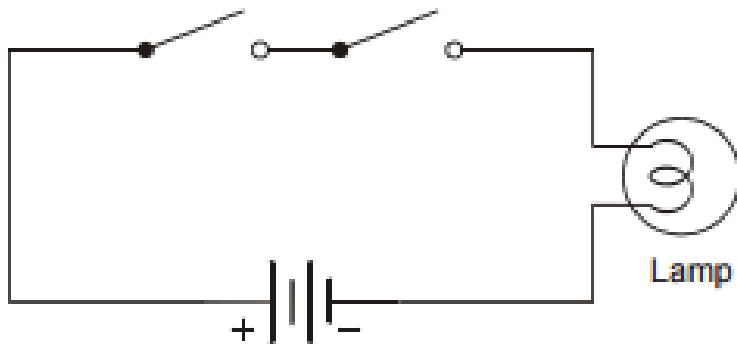
$0 \text{ V} = \text{"low" logic level (0)}$

$5 \text{ V} = \text{"high" logic level (1)}$

Transistor Characteristics Curve

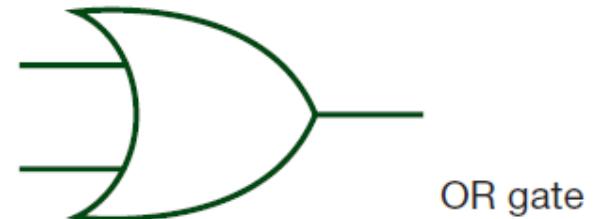
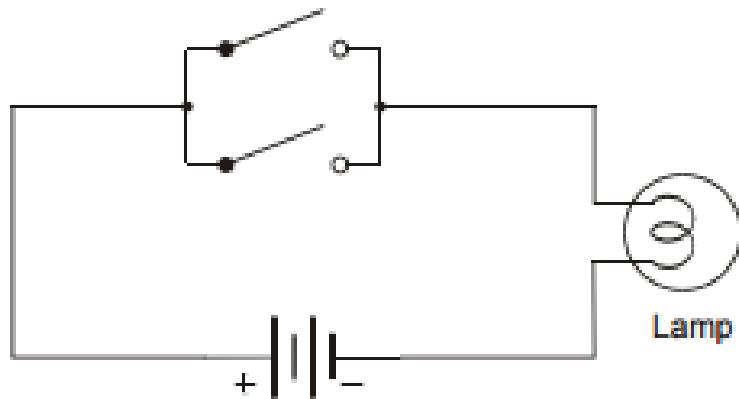
- ④ https://www.youtube.com/watch?v=Sod_5y7ZBlk
- ④ <https://www.youtube.com/watch?v=J4oO7PTnzQ>

Basic Logic Gates: AND Gate



INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	0
1	0	0
1	1	1

Basic Logic Gates: OR Gate

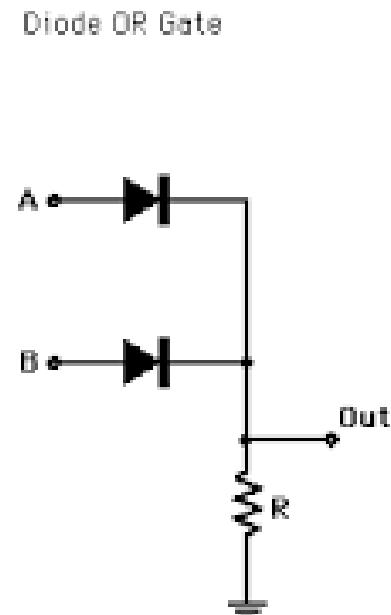
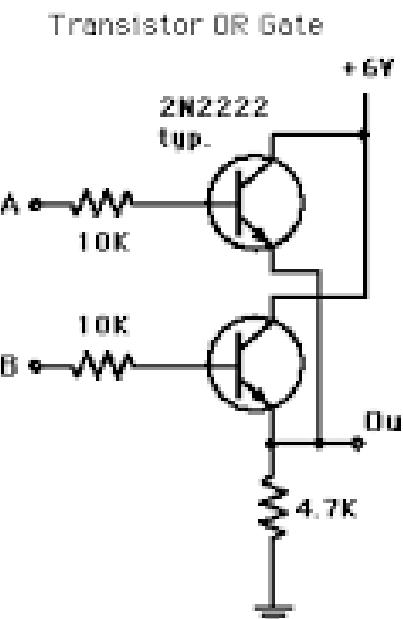
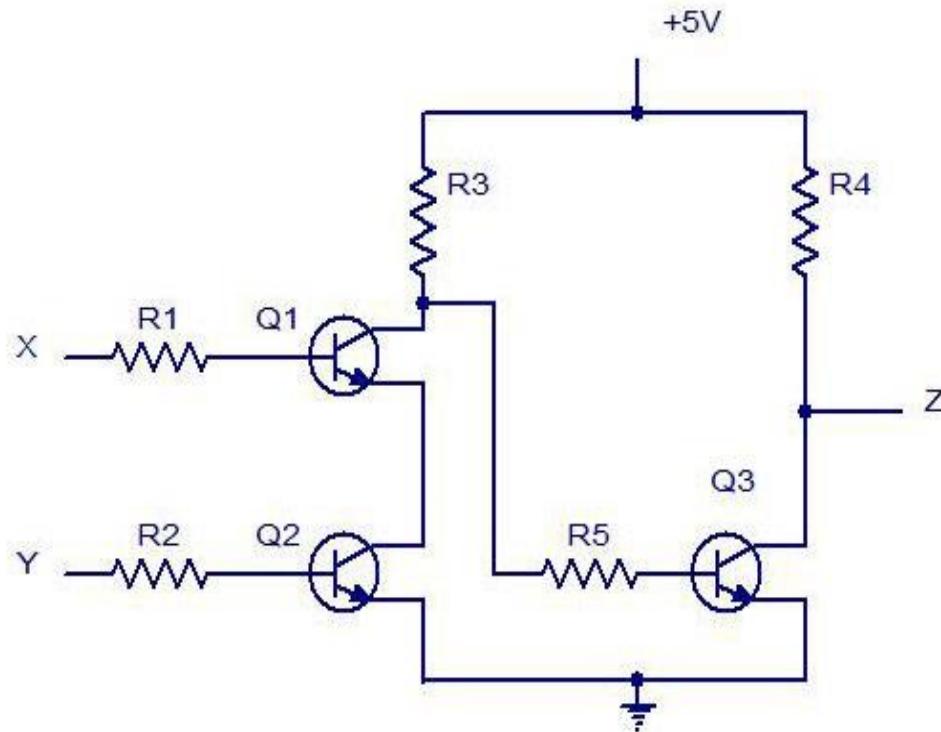


OR gate

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	1

Transistor Implementation: AND / OR

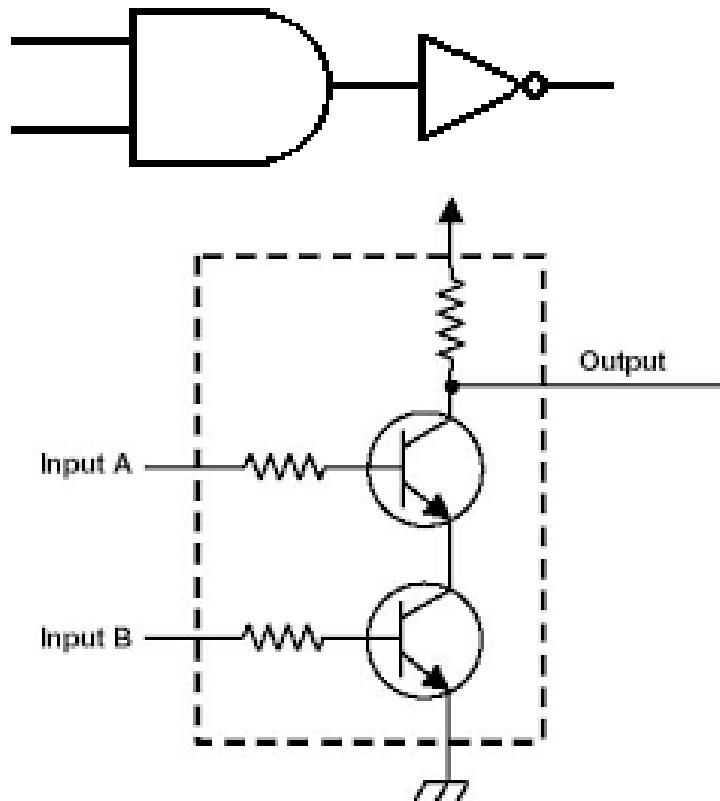
2 Input Transistor AND Gate



More Logic Gates!

④ NAND

④ NAND = NOT AND

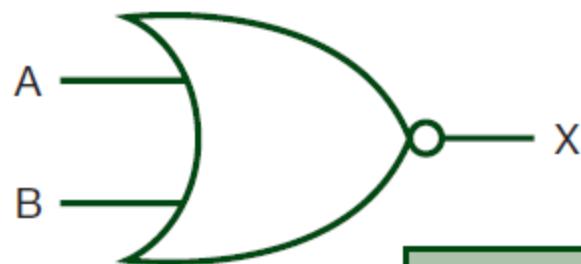


INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	1
1	0	1
1	1	0

More Logic Gates!

④ NOR

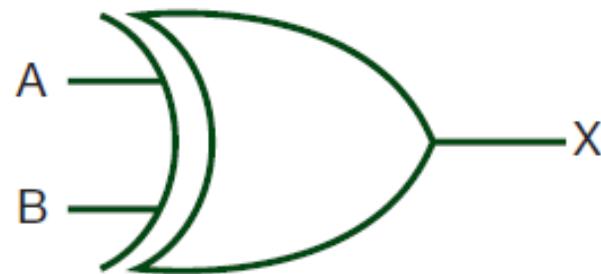
④ NOR = NOT OR



INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	0
1	0	0
1	1	0

XOR

④ Exclusive of OR



INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	0

Understanding with Real-World *Example*

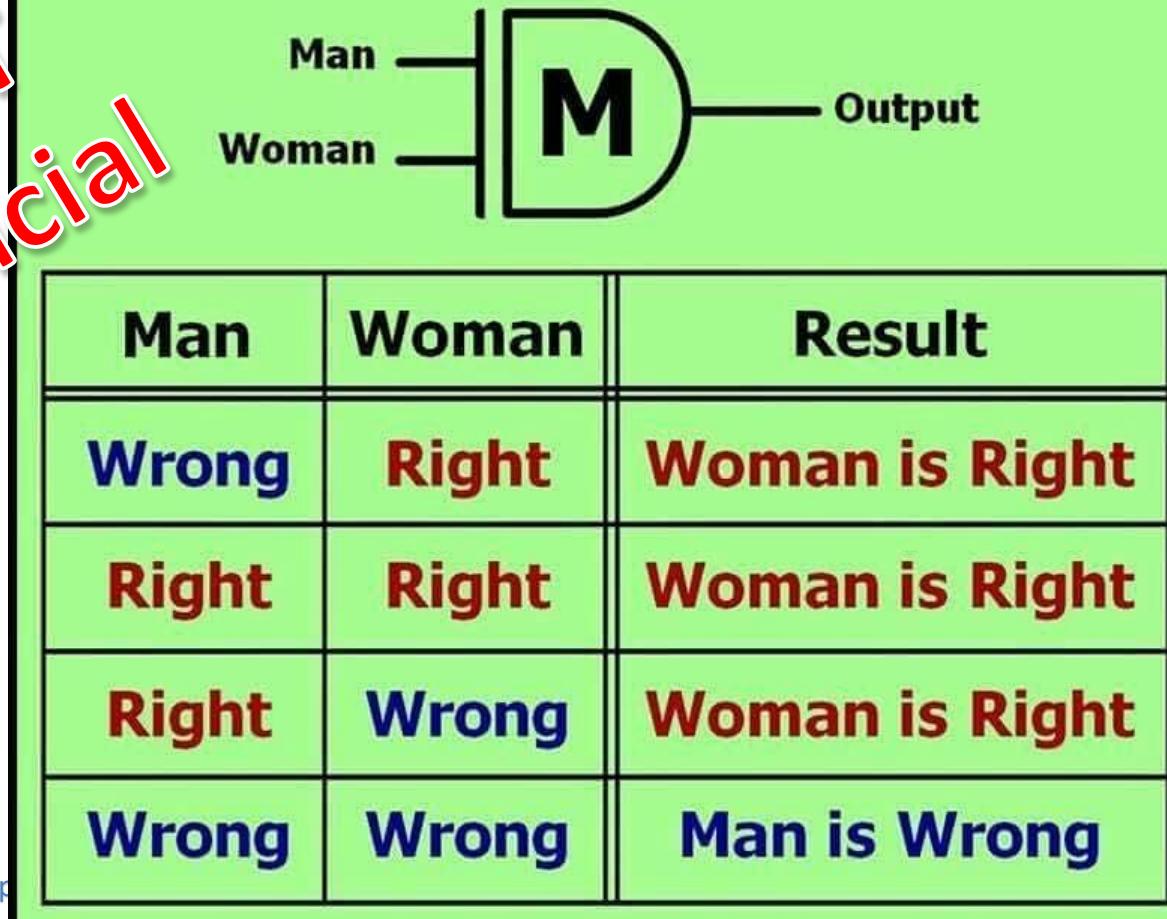
④ Making
Milk Tea
OR
Milk Coffee



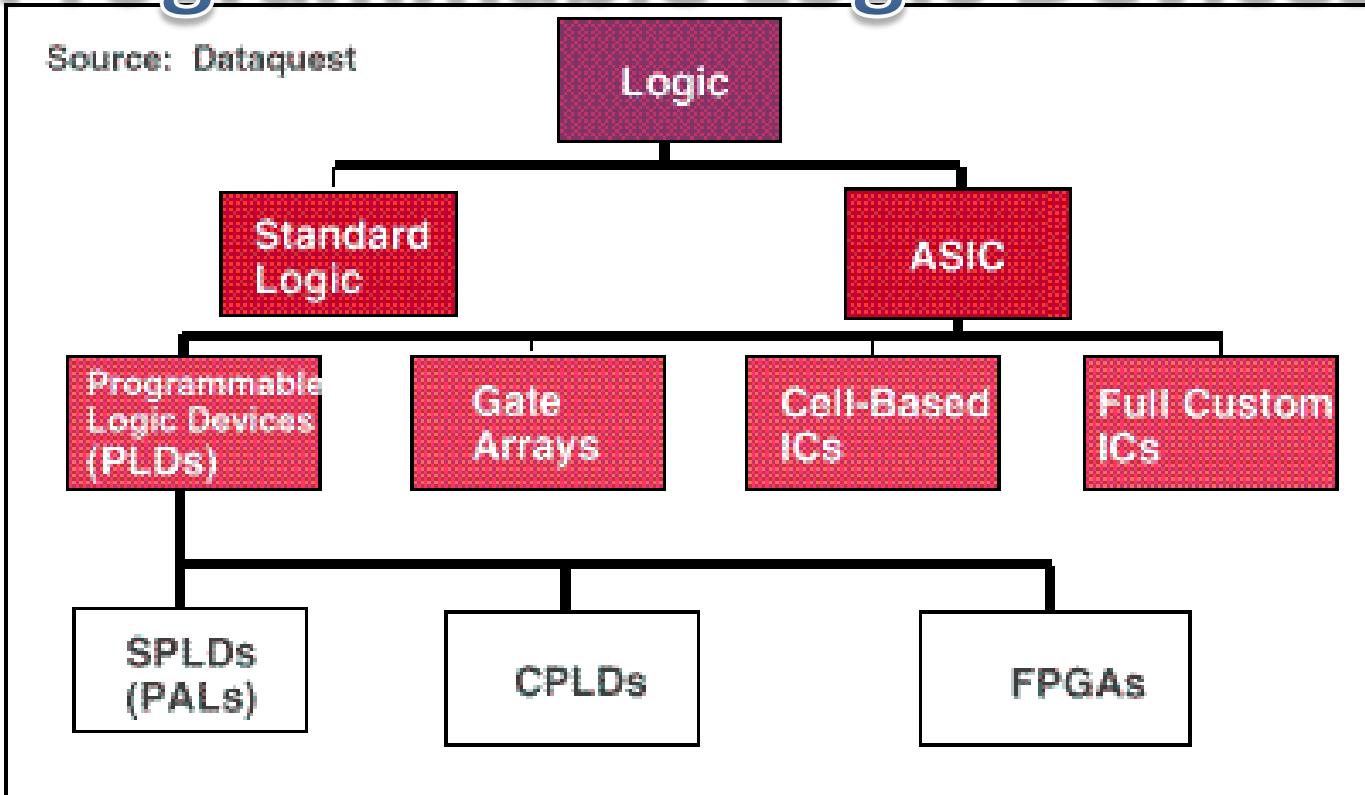
One more
Logic
Gate...

Marriage Logic Gate

NOT
Official



Programmable Logic Devices

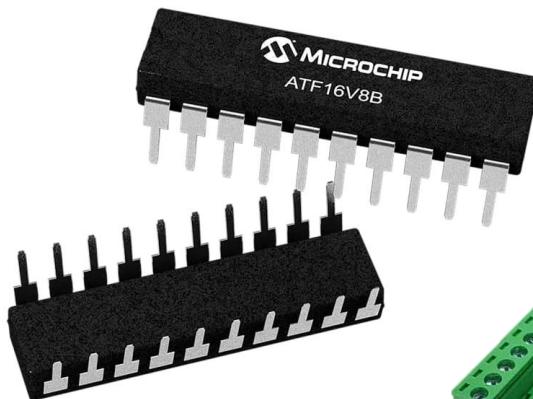


- ④ ASIC : Application-Specific Integrated Circuit
- ④ FPGA - Field Programmable Gate Arrays
- ④ PAL - Programmable Array Logic
- ④ SPLD - Simple Programmable Logic Device
- ④ CPLDs - Complex Programmable Logic Devices

Programmable Logic Devices

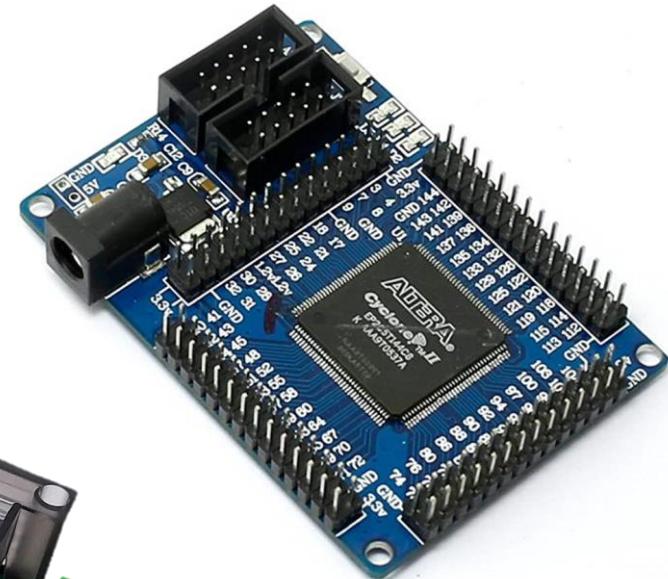
SPLD - Simple Programmable Logic Device

Example: Microchip ATF16V8B-15PU, SPLD Simple Programmable Logic Device ATF16V8B 150 Gates



FPGA - Field Programmable Gate Arrays

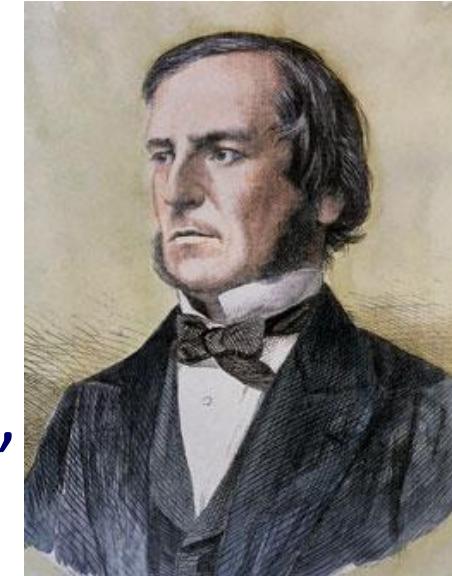
Example: ALTERA FPGA Cyclone II EP2C5T144 Minimum System Development Board



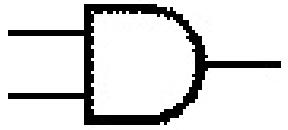
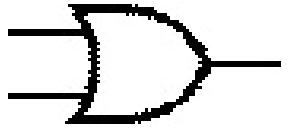
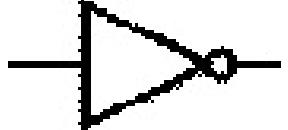
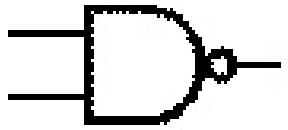
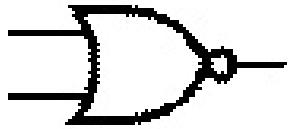
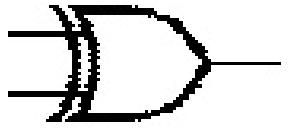
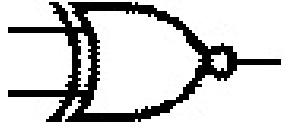
FX1N-20MR
programmable logic
controller

Boolean Algebra

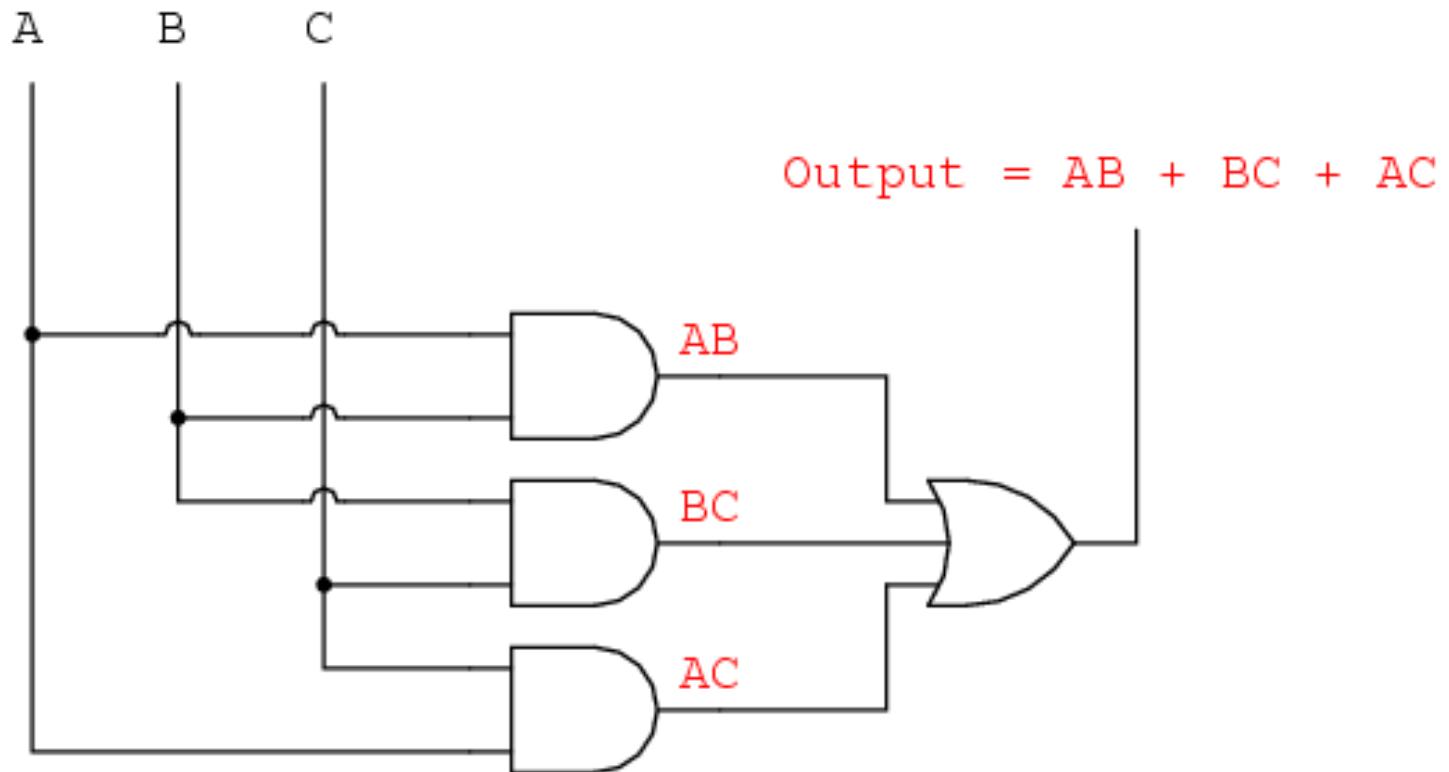
- ④ George Boole (November 1815 – 8 December 1864) was an English mathematician, philosopher and logician, the first professor in mathematics at Queen's College, Cork in Ireland
- ④ He worked in the fields of differential equations and algebraic logic, and is best known as the author of *The Laws of Thought* (1854) which contains Boolean algebra
- ④ Boolean logic is credited with laying the foundations for the information age



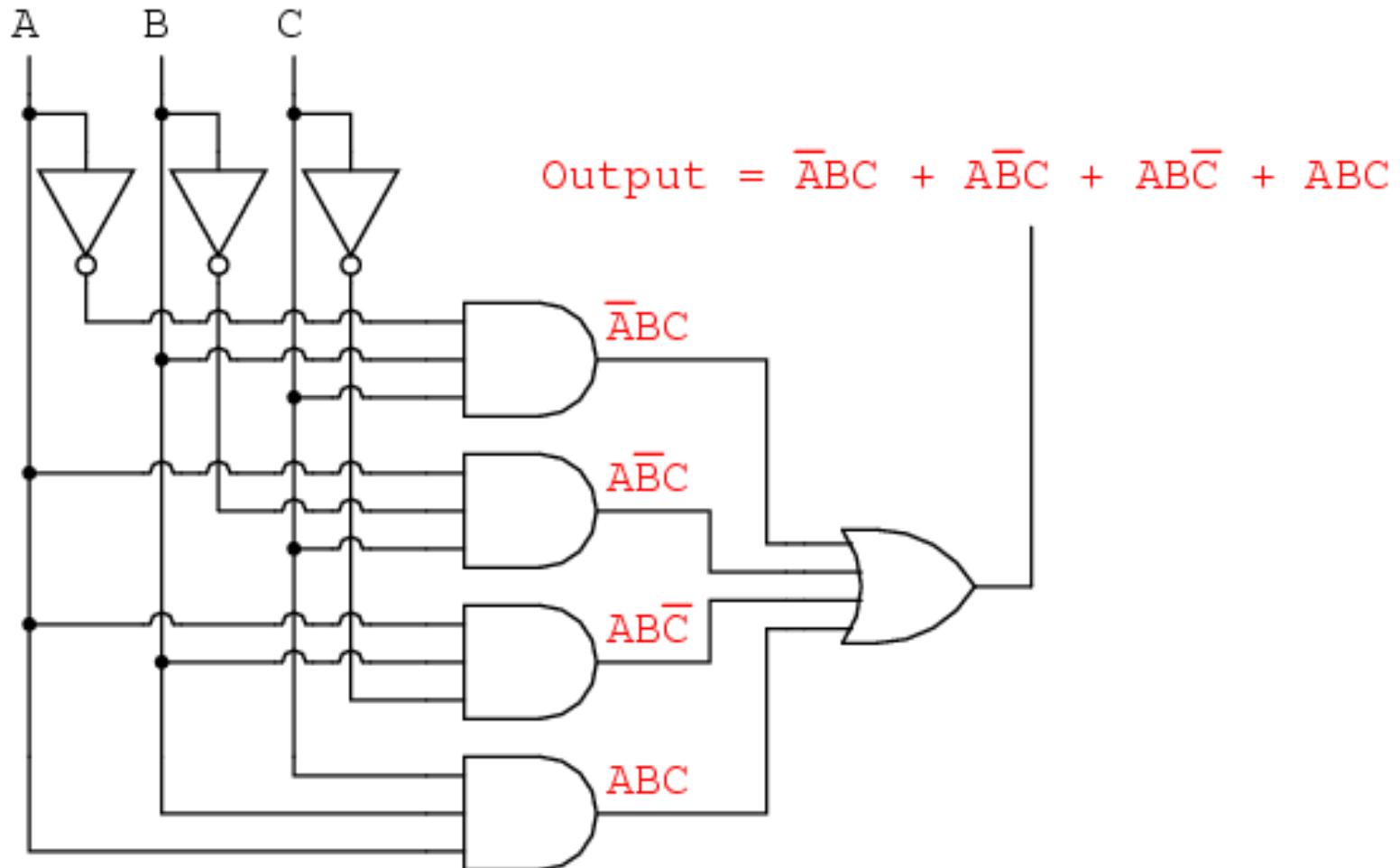
Boolean Algebra

AND		$A \cdot B$
OR		$A + B$
NOT		\bar{A}
NAND		$\overline{A \cdot B}$
NOR		$\overline{A + B}$
XOR		$A \oplus B$
XNOR		$A \odot B$ or $\overline{A \oplus B}$

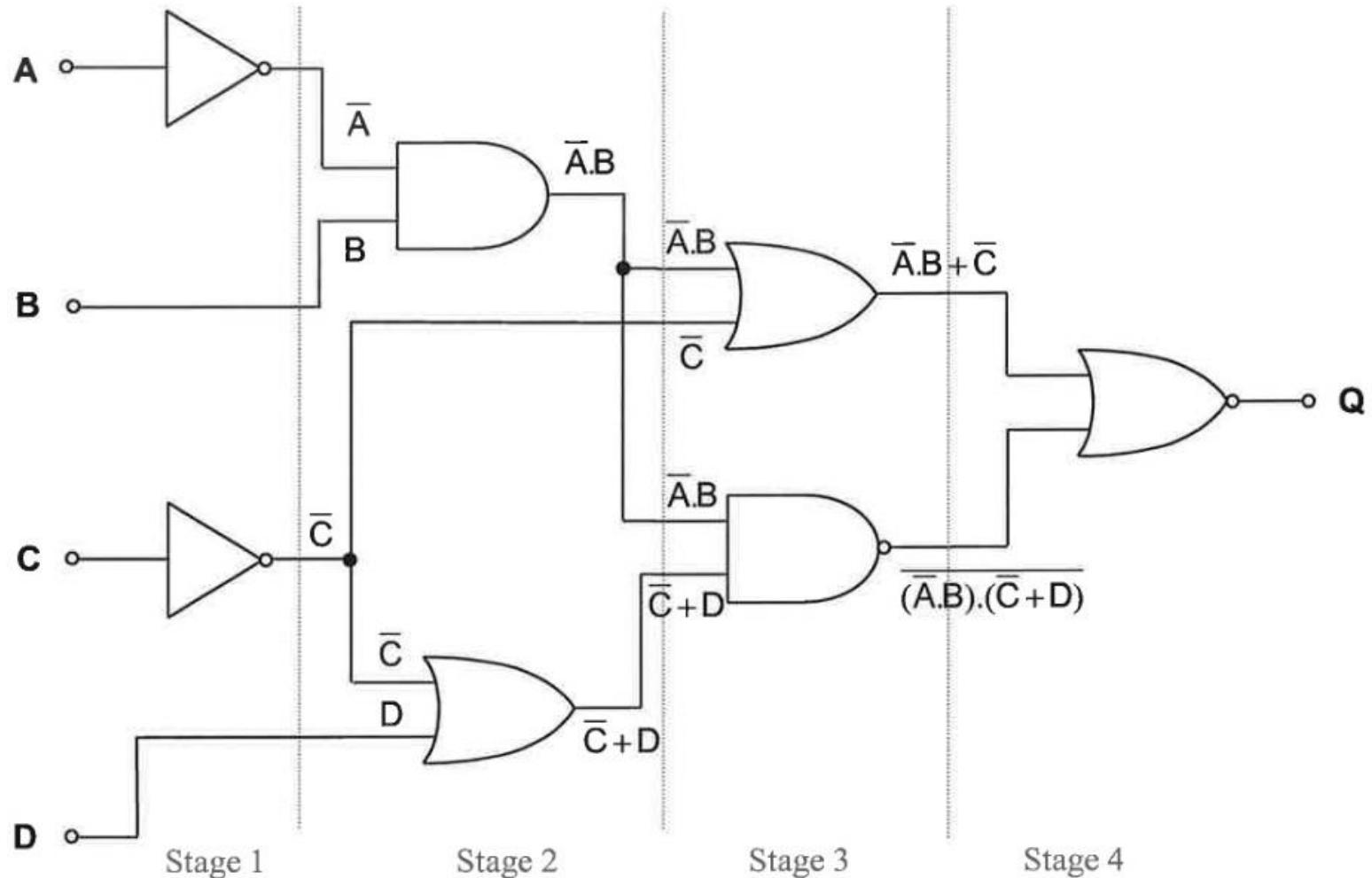
Examples



Examples



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Exercise

- ④ Construct XOR with only basic gates (AND, OR, NOT)

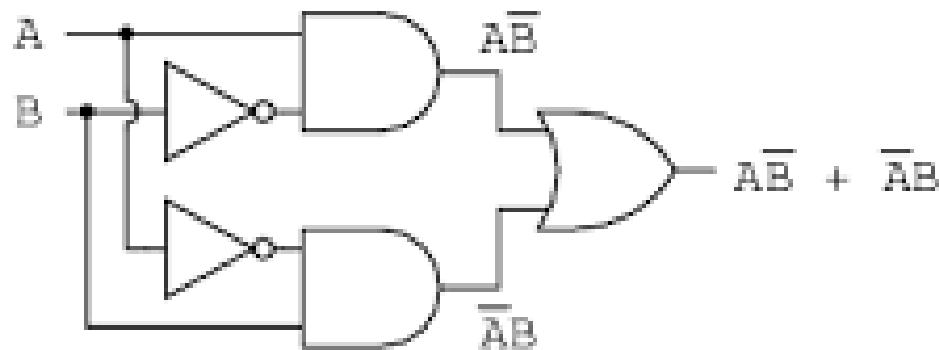
Exercise

- ④ Construct XOR with only basic gates (AND, OR, NOT)
- ④ Hint: **Construct a Boolean expression that simulates the functionality of XOR**

Answer



... is equivalent to ...



$$A \oplus B = \overline{AB} + \overline{\overline{A}}\overline{B}$$

Basic Rules for Boolean Algebra

Basic Rules of Boolean Algebra

1. $A + 0 = A$	7. $A \cdot A = A$
2. $A + 1 = 1$	8. $A \cdot \bar{A} = 0$
3. $A \cdot 0 = 0$	9. $\bar{\bar{A}} = A$
4. $A \cdot 1 = A$	10. $A + AB = A$
5. $A + A = A$	11. $A + \bar{A}B = A + B$
6. $A + \bar{A} = 1$	12. $(A + B)(A + C) = A + BC$

DeMorgan's Theorem

$$\overline{(AB)} = (\bar{A} + \bar{B})$$

$$\overline{(A + B)} = (\bar{A} \bar{B})$$

Comprehensive Version Ahead!

1.	Law of Identity	$A = A$ $\overline{A} = \overline{A}$
2.	Commutative Law	$A \cdot B = B \cdot A$ $A + B = B + A$
3.	Associative Law	$A \cdot (B \cdot C) = A \cdot B \cdot C$ $A + (B + C) = A + B + C$
4.	Idempotent Law	$A \cdot A = A$ $A + A = A$
5.	Double Negative Law	$\overline{\overline{A}} = A$
6.	Complementary Law	$A \cdot \overline{A} = 0$ $A + \overline{A} = 1$
7.	Law of Intersection	$A \cdot 1 = A$ $A \cdot 0 = 0$
8.	Law of Union	$A + 1 = 1$ $A + 0 = A$
9.	DeMorgan's Theorem	$\overline{AB} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A} \cdot \overline{B}$
10.	Distributive Law	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ $A + (BC) = (A + B) \cdot (A + C)$
11.	Law of Absorption	$A \cdot (A + B) = A$ $A + (AB) = A$
12.	Law of Common Identities	$A \cdot (\overline{A} + B) = AB$ $A + (\overline{AB}) = A + B$