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## Core Subjects

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### **COMPUTER SYSTEM ARCHITECTURE**

#### **1.1 Course Description**

The course provide students with a fundamental understanding of the functional components of a computer system, and how they are organized. The emphasis of the module is on the hardware aspects of a system, and how hardware is used during the execution of software. This is a core component of all computer science related degree courses. Practical skills will also be developed in the use and construction of computer components, and their interfacing to microprocessors.

#### **1.2 Learning Targets/Outcomes**

**By learning this course Student will able to**

- Draw the functional block diagram of a single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.
- Write assembly language program for specified microprocessor for computing  
16 bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).
- Write a flowchart for Concurrent access to memory and cache coherency in Parallel Processors and describe the process.
- Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.
- Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology

#### **1.3 Course Organization**

There will be 3-hours lecture and 2 hours Laboratory session each week. Students are expected to attend all lectures and to participate in class actively.

#### **2.1 Text Book**

1. “Computer Organization and Design: The Hardware/Software Interface”, 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.
2. M. Mano, Computer System Architecture, Pearson Education

#### **2.2 Reference Text Books**

- 1 A. J. Dos Reis, Assembly Language and Computer Architecture using C++ and JAVA, Course Technology, 2004

- 2 W. Stallings, Computer Organization and Architecture Designing for Performance, 8th Edition, Prentice Hall of India ,2009
- 3“Computer Architecture and Organization”, 3rd Edition by John P. Hayes, WCB/McGraw-Hill
- 4 Fundamentals of Digital Circuits (3rd Ed). A. Anand Kumar. (2014). PHI Learning Private Limited, Delhi

### **3. Course Content**

#### **3.1 Introduction**

- 3.1.1 Logic gates
- 3.1.2 Boolean algebra
- 3.1.3 Combinational circuits,Circuit simplification

#### **3.2 Introduction**

- 3.2.1 Flip-flops
- 3.2.2 Sequential circuits
- 3.2.3 Decoders,Multiplexers

#### **3.3 Introduction**

- 3.3.1 Registers
- 3.3.2 Counters
- 3.3.3 Memory

#### **3.4 Data Representation and basic Computer Arithmetic**

- 3.4.1 Number systems,Complements
- 3.4.2 fixed and floating point representation
- 3.4.3 character representation

#### **3.5 Data Representation and Basic Computer Arithmetic**

- 3.5.1 Addition
- 3.5.2 Subtraction
- 3.5.3 Magnitude comparison

#### **3.6 Basic Computer Organization and Design**

- 3.6.1 Computer Registers
- 3.6.2 Bus system
- 3.6.3 Instruction Set

#### **3.7 Basic Computer Organization and Design**

- 3.7.1 Timing and control
- 3.7.2 Instruction cycle
- 3.7.3 Memory Reference,Input-output and Interrupt

#### **3.8 Central Processing Unit**

- 3.8.1 Register organization
- 3.8.2 Arithmetic and Logical Micro-operations

3.8.3 Stack Organization, Micro programmed control

### **3.9 Programming the Basic Computer**

3.9.1 Instruction formats, Addressing modes

3.9.2 Instruction codes, Machine language

3.9.3 Assembly language and Input output programming

### **3.10 Input-output Organization**

3.10.1 Peripheral devices

3.10.2 I/O interface

3.10.3 File System Structure: Modes of data transfer

### **3.11 Pipelining:**

3.11.1 Basic concepts of pipelining, throughput and speedup

3.11.2 Pipeline hazards.

3.11.3 Parallel Processors: Introduction to parallel processors, Concurrent access to memory and cache coherency.

### **3.12 Memory organization:**

3.12.1 Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size

3.12.2 Mapping functions, replacement algorithms, write policies.

3.12.3 Overview of I/O Systems: Direct memory access

## **4. Plagiarism**

The University intends to develop and promote original work. Taking another person's words or ideas and using them as if they were your own or Plagiarism, as it is called, is taken very seriously at the University. Plagiarism may be deliberate or accidental.

## Computer System Architecture Lab

### **A list of potential Laboratory Practical's**

1. To design a combinational logic system for a specified Truth Table and design it using logic gate ICs.
2. Implement Half Adder and Full Adder using logic gate ICs.
3. Implement Half Subtractor and Full Subtractor using logic gate ICs.
4. To build JK Master-slave flip-flop using Flip-Flop ICs
5. To build a Counter using D-type/JK Flip-Flop ICs and study timing diagram
6. Write a program in assembly language to add two 8-bit numbers
7. Write a program in assembly language to perform multiplication for unsigned positive numbers
8. Write a program in assembly language to print input string and print it.
9. Simulate the machine to determine the contents of AC, E, PC, AR and IR registers in hexadecimal after the execution of each of following register reference instructions:

a. CLA	e. CIR	i. SNA
b. CLE	f. CIL	j. SZA
c. CMA	g. INC	k. SZE
d. CME	h. SPA	l. HLT

10. Simulate the machine for the following memory-reference instructions with I= 0 and address part = 082. The instruction to be stored at address 022 in RAM. Initialize the memory word at address 082 with the operand B8F2 and AC with A937. Determine the contents of AC, DR, PC, AR and IR in hexadecimal after the execution.

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|--------|--------|
| a. ADD | f. BSA |
| b. AND | g. ISZ |
| c. LDA |        |
| d. STA |        |
| e. BUN |        |