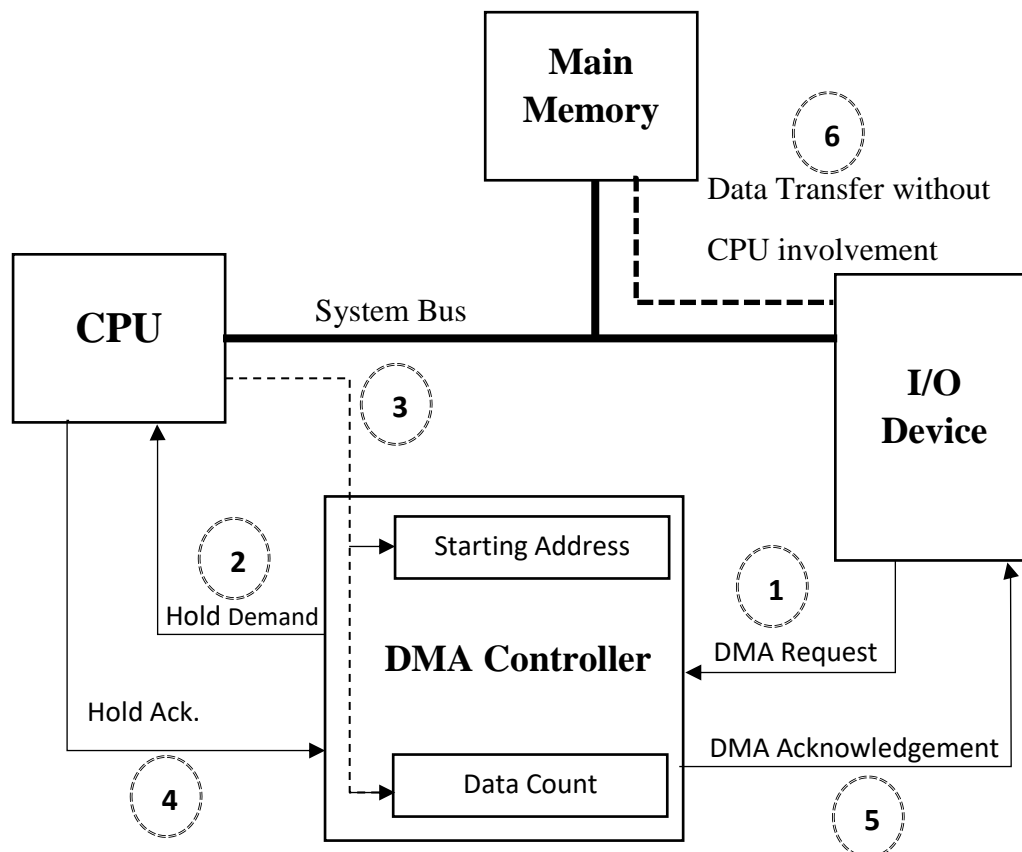


## DMA (Direct Memory Access)

Direct Memory Access (DMA) enables hardware devices to transfer data directly to or from main memory without involving the CPU, improving system performance by offloading data transfer tasks. DMA controller is a capability that allows certain hardware subsystems to access main system memory independently of the CPU. Here The DMA controller is a hardware device that manages the DMA process, facilitating data transfers between memory and devices. DMA can transfer data in different modes, including burst mode, cycle stealing mode, and transparent mode.



**Figure: Direct Memory Access (DMA))**

Initially System bus is under controlled by the CPU, I/O device request to DMA controller for system bus, sequentially, DMA controller send Hold request to CPU.

CPU check the starting address and Data count for the assigning the system bus to the I/O device. After these, CPU gives the Acknowledgement to the DMA controller, and same way DMA Controller send Acknowledgement to the I/O device for acquiring command to system bus for Memory Access. In Between CPU do only those operations which do not require system bus, otherwise mostly system CPU will be blocked.

But, *how many time system bus under control to DMA controller?* This will identify by the mode of DMA transfer, here 3 modes are there for identification. **(1). Burst Mode (2). Cycle Stealing and (3). Interleaving DMA.**

Here, example for how to initiate starting address and count the data by counting reducing of data up to 0, for stop data transfer in between I/o and Memory.

	<b>Initially</b>	<b>After 1B</b>	<b>After 2B</b>	<b>After 3B</b>
<b>Starting Address</b>	1001	1010	1011	1100
<b>Data Count</b>	50	49	48	47.....

Here data count read continue up to 0, then stop data transfer, from I/O device to Memory and system bus again under control to CPU.

In short, DMA plays the pivotal role in optimizing data flow within computers and enhancing their operational capabilities by minimizing unnecessary processing overheads.

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