Q-1 What is the function of ALE signal in 8085 microprocessor

→ the function of ALE signal is It is demultiplexed Multiplexed Address/Data Bus.

→ When ALE = '1' AD0 - AD7 work as a lower order address Bus. (A0 - A7)

→ When ALE = '0' AD0 - AD7 work as a Data Bus which is carries the 8 Bit Data.

Q=2 Give the symbolic Representation of Instruction ADC R and 'DAD RP.

ADCR = (A) ← (A) + (R) + (CY)

DAD RP = (H)(L) ← (H)(L) + (Rh)(Rl)

Q=3 Write 8085 ALP to find out 2's complement of 8 Bit NO. stored in Register 'C' save the Result in C

NOTE: 8 Bit data not given in Reg-C so, You can Assumme 8 Bit data.

```
MVI C, 45H  ; load 45H data Immediately into Register C
MOV A, C    ; copy the content of Reg C into Reg A
CMA         ; Complement of Accumulator
ADI 01H     ; ADD Immediate 01H with Reg. A
MOV C, A    ; copy the content of Reg A into Reg 'C'
RST 5       ; STOP
```

Result:- Input Output

C = 45H C = BBH (10111011)

Q=4 What is the function of Instruction Register and Decoder in 8085 μP.

→ When ever opcode fetch cycle is Perform that time opcode of Instruction stored into Instruction Register.

→ the Instruction Decoder is used to decode the

OPcode. mean is that It is taken out the meaning of that OPcode.

Q=5 What do you mean By Interuppt ? Enlist Hardware Interuppt and software Interrupt of 8085uP.

→ Interrupt is a process to Read the Data from external I/o Device.

→ there are two types of Interrupt

Hard ward Interrupt	Software Interrupt
1) TRAP	1) RST
2) RST7.5	
3) RST6.5	
4) RST5.5	
5) INTR	

Q=8 Give the full form of

PC = Program Counter
ALU = Arithmetic Logic Unit
PSW = Program status word.
RIM = Read Interrupt mask
ALE - Address latch Enable

DMA - Direct memory Acess.
RAM = Radom Access memory
Rom - Read only memory
EI - Enable Interrupt
DI - Disable Interrupt
ISR: Interrupt service Routine

Q=9 What will Be Result of XRA Bif A = 23H and B = 23H?

```
MVI A, 23H ; load 23H data Immediately in Reg.A
MVI B, 23H ; load 23H data Immediately in Reg B
XRA B      ; EX-OR operation perform Betn content of Reg B and Reg A
RST 5      ; STOP.
```

EX-OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A = 23 → ~~0100~~ 0010 0011

B = 23 → 0010 0011

0000 0000

→ after execute ~~above~~ XRA B the Result is 00H. **A = 00H**

Q=10 Enlist the steps during memory write cycle in 8085 µP.

step1: Microprocessor send signal to memory for Activate the memory chip.

step2: Identify the memory location.

step3: the data is write at specific memory location.

Q=11 List the 16 Bit Register of 8085 µP.

1) Stack Point Register (SP)
2) Program Counter (PC)
3) Register HL pair
4) Register DE Pair
5) Register BC Pair

Q=12 Define Tstate, machine cycle and Instruction cycle.

Tstate:- Microprocessor Required the clock to Perform operation like Memory Read, Memory write, I/o Read and I/o write.

→ one clock plwse is called T state.

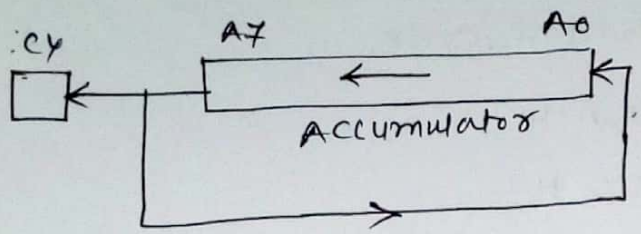
Machine cycle:- Itis defined as time Required to Perform Memory or I/o operation.

Instruction cycle: Itis defined as time Required to Perform or execute an Instruction.

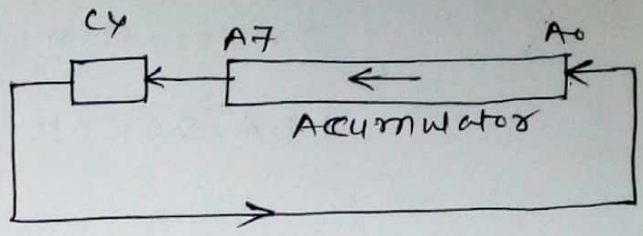
Q=13 Give the difference Betn RLC and RAL

RLC	RAL
1) RLC - Rotate left	1) RAL - Rotate left through carry.
2) This Instruction Rotates the contents of the Accumulator one Position left.	2) The Instruction Rotates the contents of Accumulator one Position left through carry
→ The MSB of Accumulator is transferred in to Both CY flag and LSB Bit of Accumulator.	→ The MSB Bit of Accumulator Transferred into the CY flag and the CY flag into LSB of the Accumulator.

RLC



RAL



Q=15 The 8085 µP has 8 Bit data Bus and 16 Bit Address Bus

Q=16 The 8085 µP supported maximum memory 64 kB.

Q=17 Give example of sing Byte, two Byte and three Byte Instruction.

① single Byte:-

Instruction	machine code
MOV A, B	78H
ADD C	89H
CMA	2FH

It Required single memory location to stored opcode.

② two Byte:-

Instruction	machine code.
MVI A, 32H	3E 32H
ADI 65H	C6H 65H

It is Required two memory location to stored opcode.

Three Byte Instruction.

Instruction	machine code
LDA 2050H	3A H
	50 H
	20 H
STA 3050H	32H
	50H
	30H

Q=18 what is function of ORA B Instruction.

~~MVI A~~

→ the function of ORA B mean 'OR' operation is perform Bet^n the content of Register B and Accumulator content.

OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Ex

```
MVI A, 32H
MVI B, 45H
ORA B
RST 5
```

Input
A = 32H
B = 45H

Output
A = 77H

```
0011 0010 (32)
0100 0101 (45)
0111 0111
 7    7
```

Q=19 Define stack and stack Related Instruction.

→ stack is a LIFO memory

→ Any memory location used as stack

→ To Initiaze memory location using SP Register with Instruction LXI SP, 2050H.

→ the PUSH and POP Instructions are used in stack operation.

→ PUSH Instruction is used for to load the data into stack. ~~from~~ ~~Register Pair~~

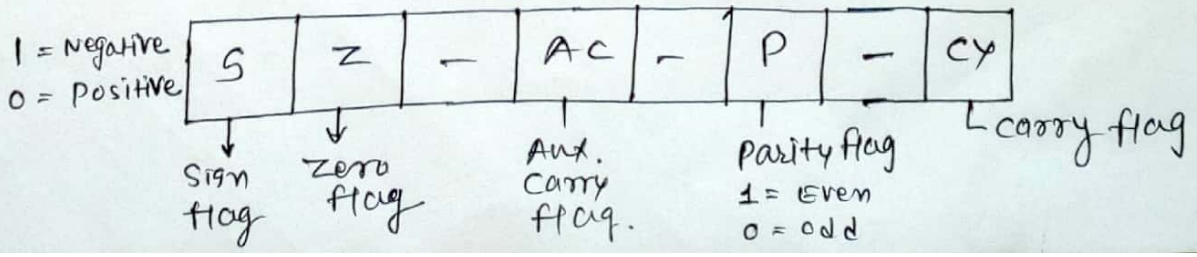
→ POP Instruction is used for to fetch the data from Memory location. and stored at Register pair

Q-21 Which Instruction is used to Read data from Port address 05H?

IN 05H

Read the data from Port address 05H put in to Accumulator.

Q-22 Draw the format of 8085 flag Reg.



Q-23 What is mean By multiplexed address / Data Bus?

→ In 8085 µP lower order Address Bus (A0-A7) and Data Bus are combined.

→ Bath are perform alternate operation Base on condition of ALE pin. when ALE='1' lower order Address Bus work's and when ALE='0' Data Bus work's.

Q-24 Define opcode and operand and Instruction.

(1) Instruction:- Instruction is a command which is given to the microprocessor to perform Particular task or operation.

→ Instruction made of opcode and operand's.

(2) opcode: opcode is operational code that Indicate that which operation to Be perform.

(3) Operand's:- The operands for an Instruction can Be specified in different way knows as Addressing mode.

→ the data operated an Instruction is called operands.

Ex MOV A, B - opcode is 78H
Operand's - A, B

MVI A, 32H - opcode is 3E
Operands is 32H

Q=25 Difference Betⁿ Direct Addressing mode and Indirect Addressing mode

Direct Addressing mode	Indirect Addressing mode.
① In Direct Addressing mode Instructions the address of an operand is directly given with in the Instruction itself	① The Instruction that use the indirect Addressing specifies the address of an operand In directly into the Register Pair
② Ex LDA 2050H	② mov A, M

Q=26 what mean By vectored Interrupt in 8085.

→ The location at which control is transferred when any Interrupt occurs is called vector Interrupt.

→ the address is fixed for vectored Interrupt

	Interrupt	Address
①	TRAP	0024H
②	RST7.5	003CH
③	RST6.5	0034H
④	RST5.5	002CH

Q= 80 function of following pins of 8085 MP.

(1) ALE:- It stands for Address latch Enable It is used to Demultiplex ~~Multp~~ multiplexed address/ Data Bus (AD7 – AD0)

→ When It is High (AD7-AD0) carries lower Byte of an adress.

→ when It is low they are used as 8 Bit Data Bus. and It is carries 8 Bit data.

(2) X1 and X2 :- X1 and X2 are used to connect the crystal ~~for this Inter~~. for this Internal clock generator All operation perform By 8085 are synchronized to this clock.

(3) TRAP:- It is Non Maskable interrupt and used only in ~~emerg~~ emergency like power failure when It is occurs for once It can not Be stopped By Software and Hardware.

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4) HOLD and HLDA :-

These signals are used with DMA controller DMA controller used HOLD to send the Request for granting the control of Buses of microprocessor

→ HLDA is used By microprocessor to acknowledge the granting of Request.

5) READY :- It is used to synchronize the operation with slower Peripherals when It is high Device is Ready to Perform Read or write operation.

6) S_1 and S_0 :- They are status. It is Represent ~~used~~ with $IO/\overline{M}$ to show the different operation like memory Read memory write, opcode fetch, I/O Read and I/O write.

7) $\overline{\text{Reset In}}$:- When $\overline{\text{Reset In}}$ Is low microprocessor Reset- it self and Program counter Intializes from 0000H.

Q=3) Define Bytesize and Addressing mode of following ~~Instruction~~ Instructions

	Instruction	Bytesize	Addressing mode
(1)	MOV A, B	1	Register Addressing mode
(2)	MVI A, FFH	2	Immediate. Addressing mode.
(3)	ADI 05H	2	Immediate Addressing mode
(4)	ADD C	1	Register Addressing mode
(5)	CMA	1	Implied Addressing mode
(6)	DAD RP	1	Register
(7)	SPHL	1	Register
(8)	STAX B	1	Indirect Addressing mode
(9)	LDAX B	1	Indirect Addressing mode

	Instruction	Byte size	Addressing mode.
10)	XTHL	01	Indirect Addressing mode.
11)	ANI 03H	02	Immediate.
12)	ACI 05H	02	Immediate
13)	PCHL	01	Register
14)	LXI SP, 3050H	03	Immediate
15)	XCHG	01	Register
16)	LHLD 2060H	03	direct-
17)	PUSH B	01	Indirect
18)	POP PSW	01	Indirect-
19)	XOR A	01	Register
20)	JC 2050H	03	Immediate Addressing mode.