ch - 1
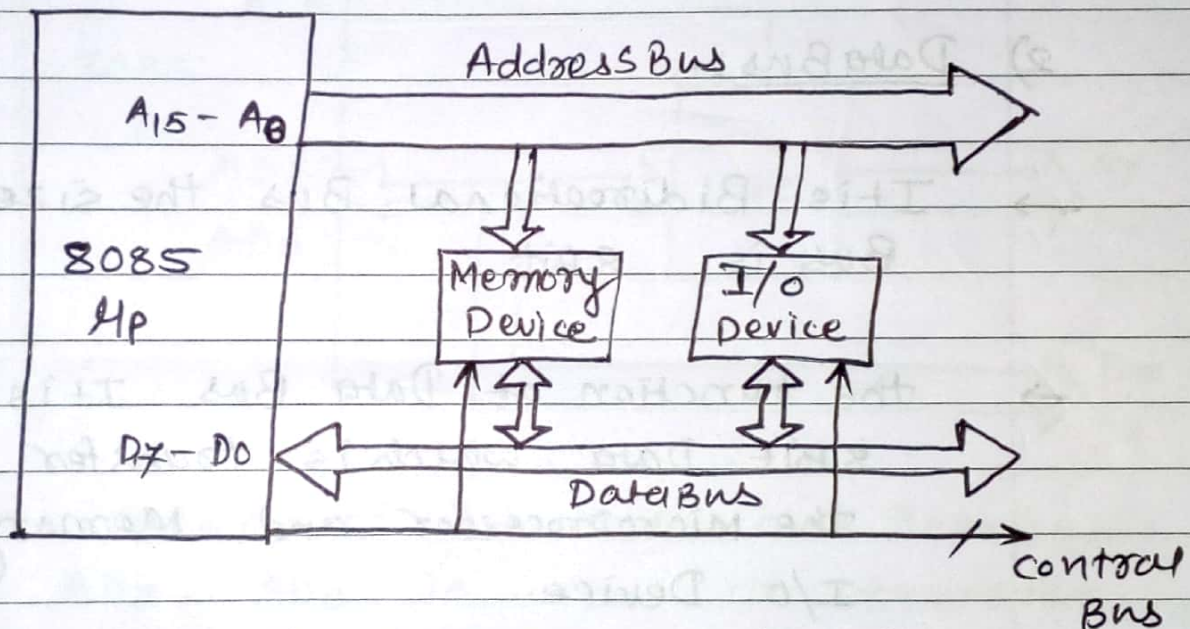
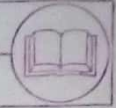* Explain Bus organization of 8085 µp !

or

* Explain Bus structure of 8085 µp!

→ The 8085 Microprocessor consist three
   types of Bues as given Below.

① Address Bus
② Data Bus
③ Control Bus.

① Address Bus :-
→ Address Bus is Unidirectional which is
carries ~~easy~~ 16 Bit ad Memory address or
I/o Port address.

→ The address Bus also determines the total Amount of Memory accessed By the Microprocessor

∴ 8085 u/p consist 16 Bit Address Bus.
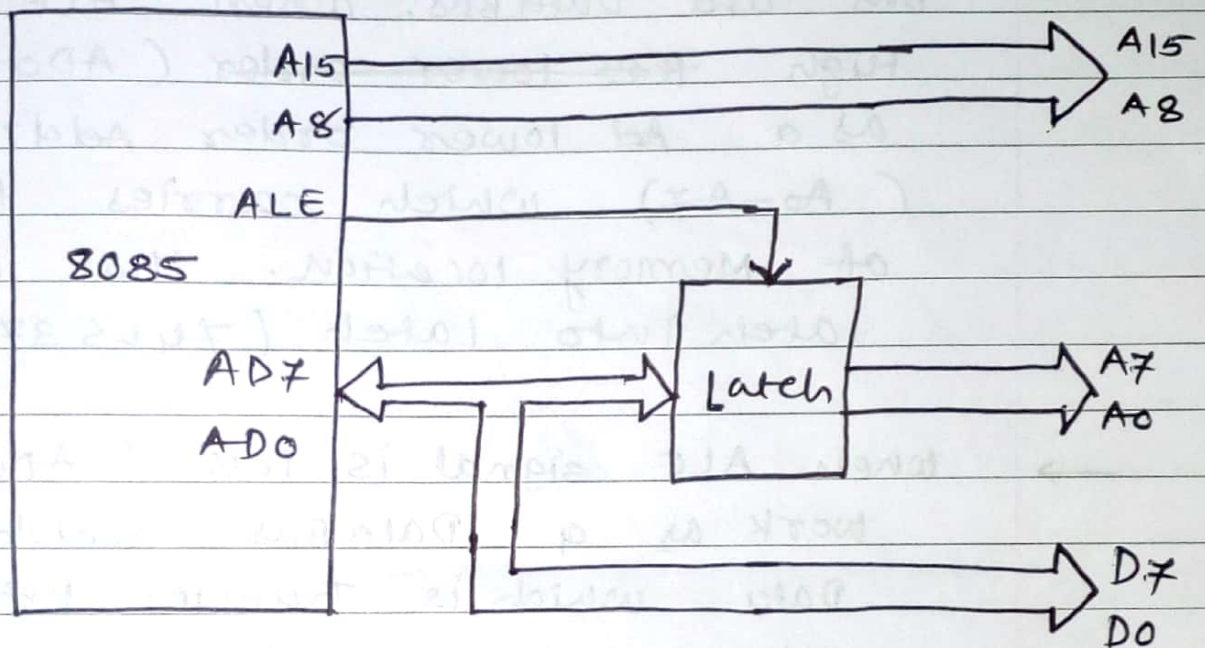
$$2^{16} = 64 KB.$$

2) **Data Bus :-**

→ It is Bidirectional Bus the size of Data Bus is 8 Bit.

→ the function of Data Bus It is carries 8 Bit Data which is transfer Between the Microprocessor and Memory or I/o Device.

3) **Control Bus:-**

→ Control Bus consist various signals like Synchronization signals which is acts as an Hand shake signals Between the Microproceessor and I/o Device.

* De. Explain Demultiplexing Multiplexed
  Address Bus and DataBus.

```
        ┌──────────────┐                          ──────────►  A15
        │          A15 ├──────────────────────────────────►   A8
        │          A8 ←┤
        │              │
        │          ALE ├──────────┐
        │   8085       │          │
        │              │          ▼
        │              │      ┌────────┐
        │          AD7 ←──────┤        ├──────────────────►  A7
        │              ├──────►  Latch ├──────────────────►  A0
        │          AD0 │      └────────┘
        │              │   │
        └──────────────┘   └──────────────────────────────►  D7
                                                              D0
```

→ The Multiplexed Address Bus and DataBus
  AD7 - AD0 is used to transfer
  Data and Address Both.

→ When ever Microprocessor Perform the
  Memory Read or Write operation
  we Required memory location which is
  specified By 16 Bit address. this
  address carries Address Bus.

→ The Higher Byte of Address available
  through Higher order Address Bus
  (A15 - A8), and lower Byte of address
  available through lower order Address Bus
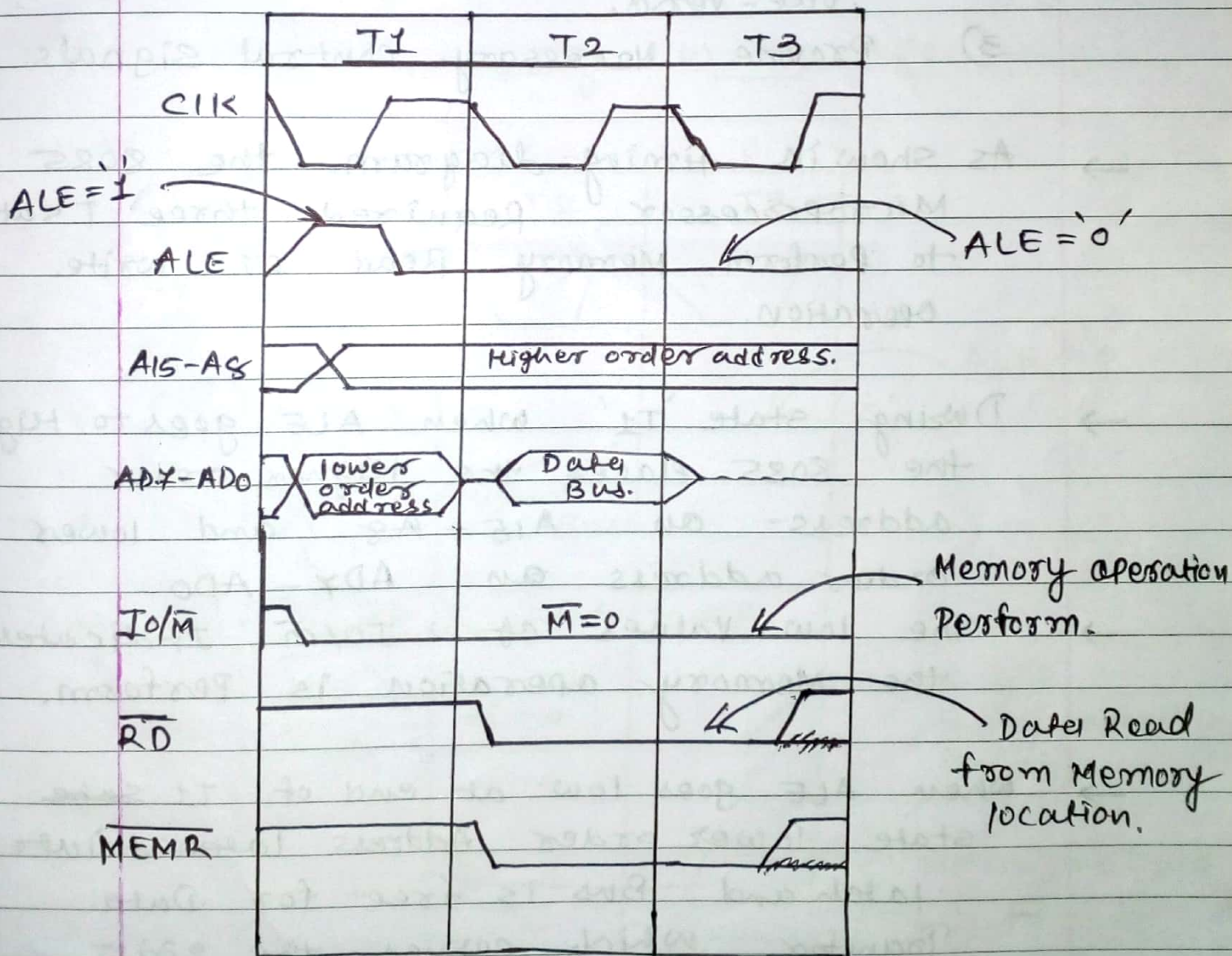 (AD7 - AD0)   (A8 - A0)
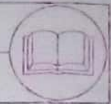
→ But lower order Address Bus and DataBus Multiplexed. (~~AD7-AD0~~) (AD7 — AD0)

→ We need demultiplexed lower order Address Bus and Data Bus. When ALE signal is High ~~the lower order~~ (AD0 — AD7) work as a ~~Ad~~ lower order Address Bus (A0 — A7) which carries lower Byte of Memory location. that address latch into latch (74LS373)

→ When ALE signal is low (AD0 — AD7) work as a Data Bus which carries Data which is Transfer Between Microprocessor and Memory Device.
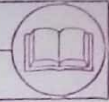
* Explain Memory Read and write cycle operation.

or

* Draw and Explain timing diagram of Memory Read and Memory write cycle.

	T1	T2	T3
CIK			
ALE			
A15-A8		Higher order address.	
AD7-AD0	lower order address	Data Bus.	
IO/$\overline{M}$		$\overline{M}=0$	
$\overline{RD}$			
$\overline{MEMR}$			

ALE = 1

ALE = 0

Memory operation Perform.

Data Read from Memory location.

→ The 8085 Microprocessor Perform the operation in three steps.

1) To identify the Memory location or I/o Port address of I/o Device.

2) Transfer the Data Bet^n, Microprocessor and I/o Device or Memory Device vice-versa.

3) Provide Necessary control signals.

→ As show in timing diagram. the 8085 Microprocessor Required three T sates to Perform Memory Read or write. operation.

→ During state 'T1' when ALE goes to High the 8085 places the Higher order address on $A_{15} - A_8$ and lower order address on $AD_7 - AD_0$.

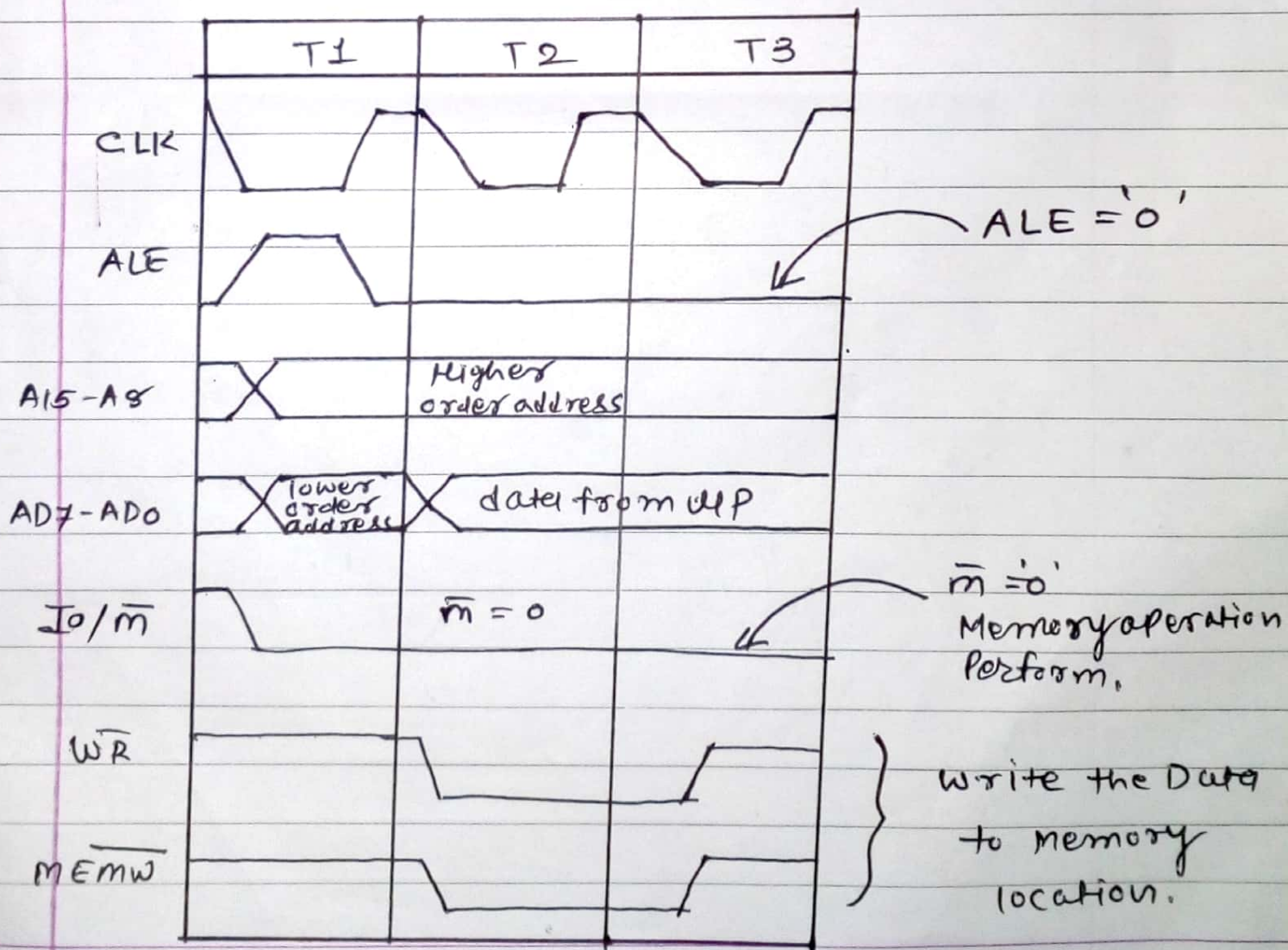→ The low values of $IO/\overline{M}$ Indicates the Memory operation is Perform.

→ when ALE goes low at end of T1 state lower order Address latched into latch and Bus is free for Data Transfer. which carries the 8 Bit Data.

→ During T2 state, $\overline{RD}$ goes to low and the control signal $\overline{MEMR}$ is also goes to low so, the Data is Read from Memory location.

→ During T3 state $\overline{RD}$ and $\overline{MEMR}$ signals are goes to High.

* Explain Memory Write operation:-

	T1	T2	T3
CLK			
ALE			
A15-A8		Higher order address	
AD7-AD0	lower order address	data from µP	
Io/$\overline{m}$		$\overline{m} = 0$	
$\overline{WR}$			
$\overline{MEMW}$			

ALE = '0'

$\overline{m}$ = '0'
Memory operation Perform.

} Write the Data to memory location.

→ During state `T2` $\overline{WR}$ and the control signal $\overline{MEMW}$ are goes to low so, the Data write to Memory location.

→ During state `T3` $\overline{WR}$ and $\overline{MEMW}$ signal goes to High.