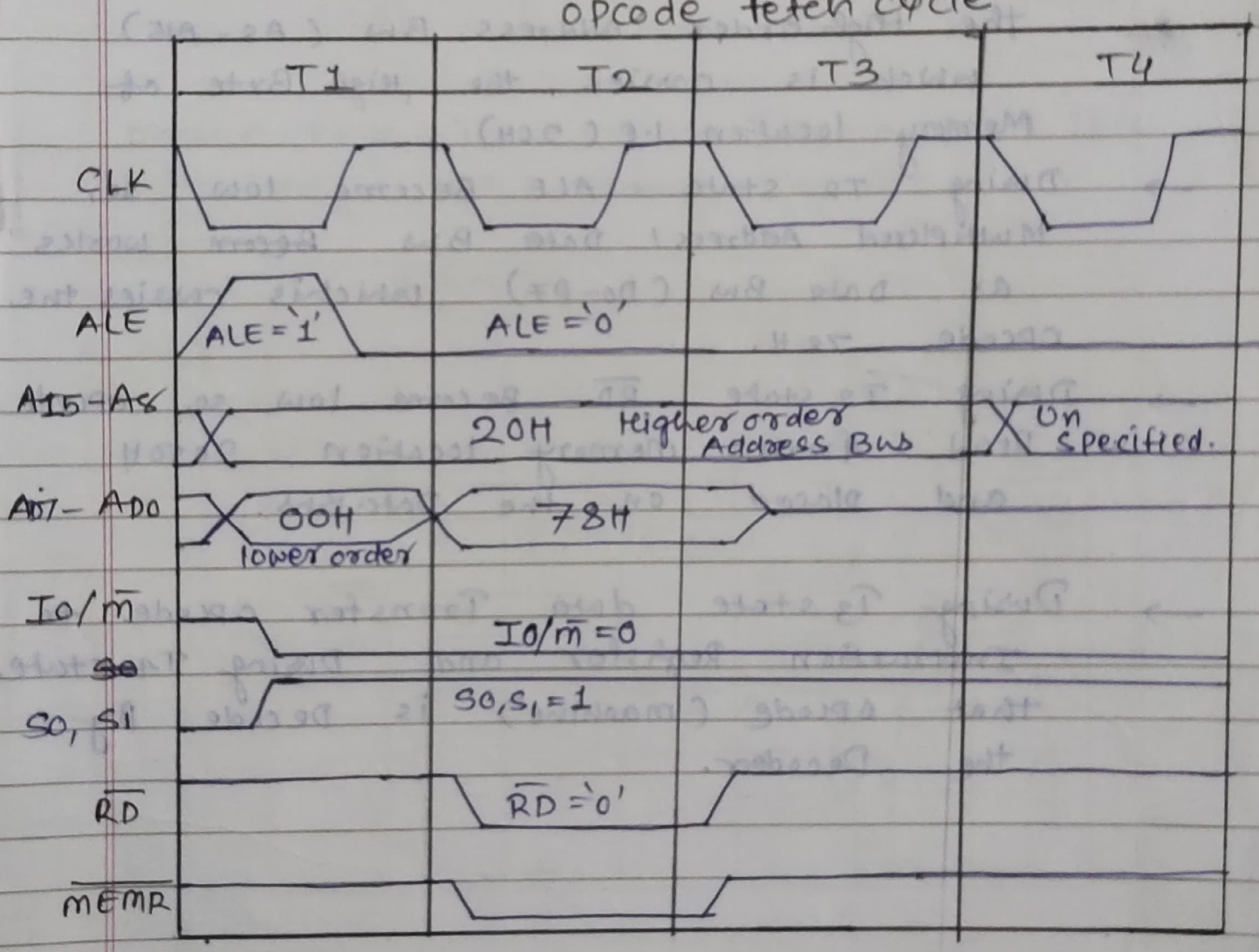
Ch-2

* Draw and Explain timing diagram of MOV A, B.

Memory location	Instruction	Machine code
2000H	MOV A, B	78H



→ The Instruction MOV A, B is Required '4' T state to fetch opcode.

→ During the 'T1' state when ALE = '1' so, Multiplexed Address/ Data Bus (AD7 - AD0) work as lower order Address Bus which is carries lower Byte of memory location ie (00H) as show in timing diagram.

→ $IO/\overline{M}$ signal Become Low dueto Microprocesso * deal with Memory.

→ the status signal S_0 and S_1 Both are Become '1' Because opcode fetch opera perform.

→ the High order address Bus (A8 - A15) which is cassies the High Byte of Memory location i.e (20H)

→ During T2 state. ALE Become low so, Multiplexed Address/ Data Bus ~~Becom~~ works as Data Bus (D0 - D7) whichis cassies the opcode 78H.

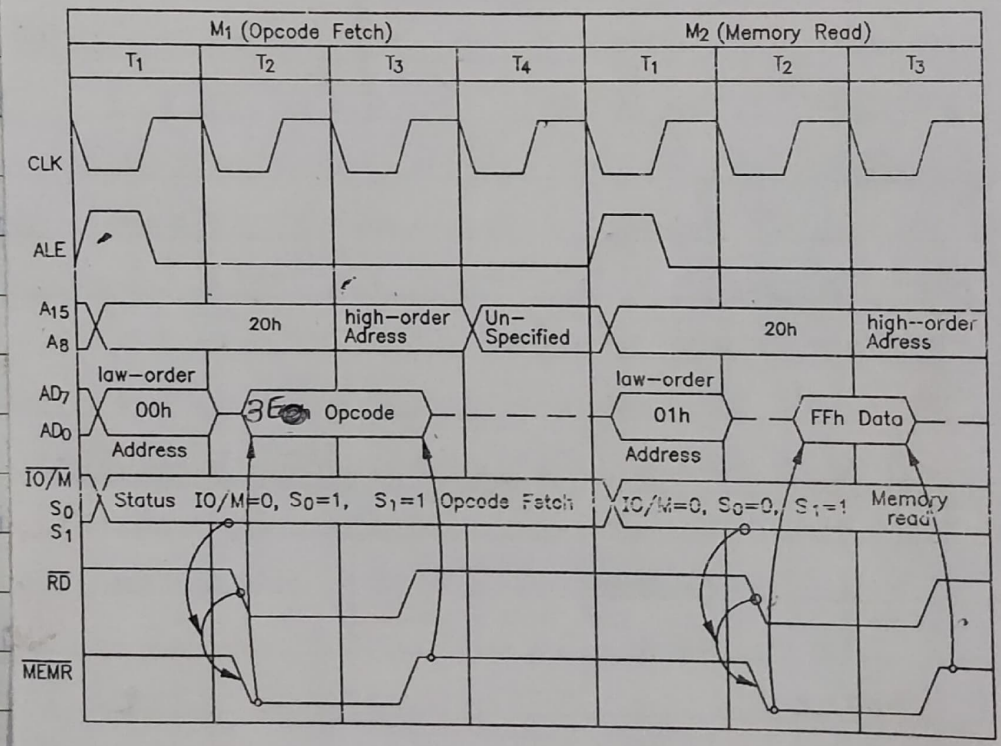
→ During T2 state $\overline{RD}$ Become low so, opcode Read from memory location 2050H and placed on the Data Bus.

→ During T3 state data Transfer opcode to Instruction Register and During T4 state that opcode (machine) is Decode By the Decoder.

* Draw and Explain timing digram of MVI A, FFH.

Memory location	Instruction	machine code
2000	MVI A, FFH	3EH
2001		FFH

MVI A, FFH is a 2 Byte Instruction It is Required two Memory location.



(FIG. 2.6 : TIMING AND EXECUTION OF MVI A, FFH INSTRUCTION)

→ The first machine cycle M1 (opcode fetch) has four T states and second machine cycle M2 has three T states.

→ The 8085 Identifies the first machine cycle M1 as opcode fetch cycle By control signals $IO/\overline{M} = '0'$ $S_1 = 1'$ and $S0 = 1'$.

→ During T2 state the 8085 send the control signal $\overline{RD}$ low which together with control signal IO/$\overline{m}$ generates $\overline{MEMR}$ to enable the memory device to place OPcode 3EH on Data Bus.

→ The 8085 Read that OPcode transfer to Instruction Register During T3 state and It is decode During T4 states.

→ The second machine cycle is M2 is Memory Read cycle identified By control signal IO/$\overline{m}$ = '1' and S_1 = '1', S_0 = '0'

→ In this cycle the 8085 places address 2050 on Address Bus and ALE makes High During T1 states.

→ the control signal $\overline{RD}$ goes low which together with IO/$\overline{m}$ generates $\overline{MEMR}$ to enable the memory Device to place Data 'FFH' on Data Bus During 'T2' states. the Instruction execute During T3 State.

→ So, MVI A, FFH Consist 4 states of OPcode fetch 3 states for memory Read total '7' states Required.