processor Project Status (12/29/2022 - 23:17:48)			
Project File:	Processor_ISE.xise	**Parser Errors:**	No Errors
Module Name:	processor	**Implementation State:**	Synthesized
Target Device:	xc7a100t-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.1	• **Warnings:**	117 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	607	126800	0%
Number of Slice LUTs	1863	63400	2%
Number of fully used LUT-FF pairs	309	2161	14%
Number of bonded IOBs	3	210	1%
Number of Block RAM/FIFO	3	135	2%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	16	240	6%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Thu 29. Dec 23:21:25 2022	0	117 Warnings (0 new)	18 Infos (0 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
ISIM Simulator Log	Out of Date	Thu 29. Dec 23:20:32 2022

Date Generated: 12/29/2022 - 23:32:35