Micro - Processor Assignment 1 146256 - SINGH SEHMI - ICS3C

Solotion: osing a 3-to-8 decoder:

Address Lines 7 (Ao, A1, A2)

Ootpots 7 (Yo, Y1, Y2, Y3, Y4, Y5, Y6, Y7)

	To get 1	ert Addresses:
D	Address	Port whore: Port 0)
0	000	o Port 1 Inpot
l	001	Port 2 Ports
2	010	2 Port 3
3	011	3 Post 4)
4	(00	4 Port 5 Ootpot
5	101	5 Port 6 Ports
6	110	6 Port 7
7	411	7

Connocting Outpot > Pont:

Yo > Port O (Inpot) YH + Pont 4 (Outpot)

Y, + Pont 1 (Inpot) Ys + Pont 5 (outpot)

Y2 + Pont 2 (Inpot) Y6 + Pont 6 (outpot)

Y3 + Pont 3 (Inpot) Y7 + Pont 7 (outpot)

Diagram !	76	> POSE O
	6	Port 1 (Input
	Y2	Port 2
A . B	2 05 Y3	Port 3
A B	60 4	Post 4)
A2 9	8 Ys	Port 5 Gotput
	Y _G	Port 6
	У ₇	> Port 7